DATA
BOOK

UMC

Computer ICs

1990
1991

1990-1991 DATA BOOK

Computer ICs

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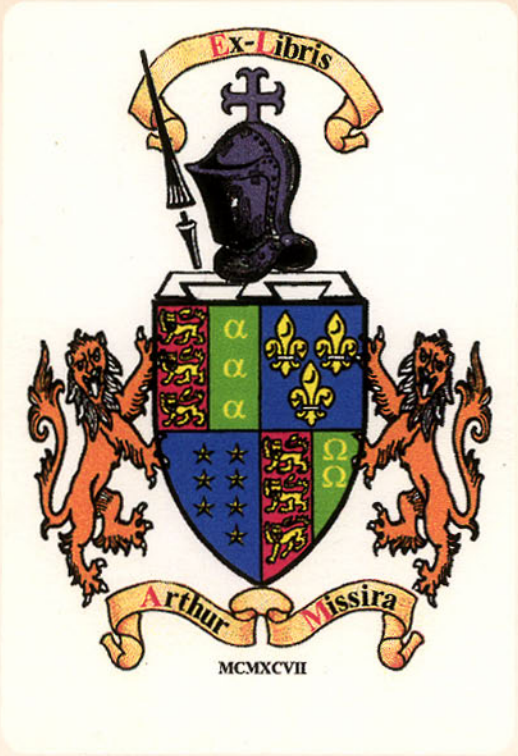
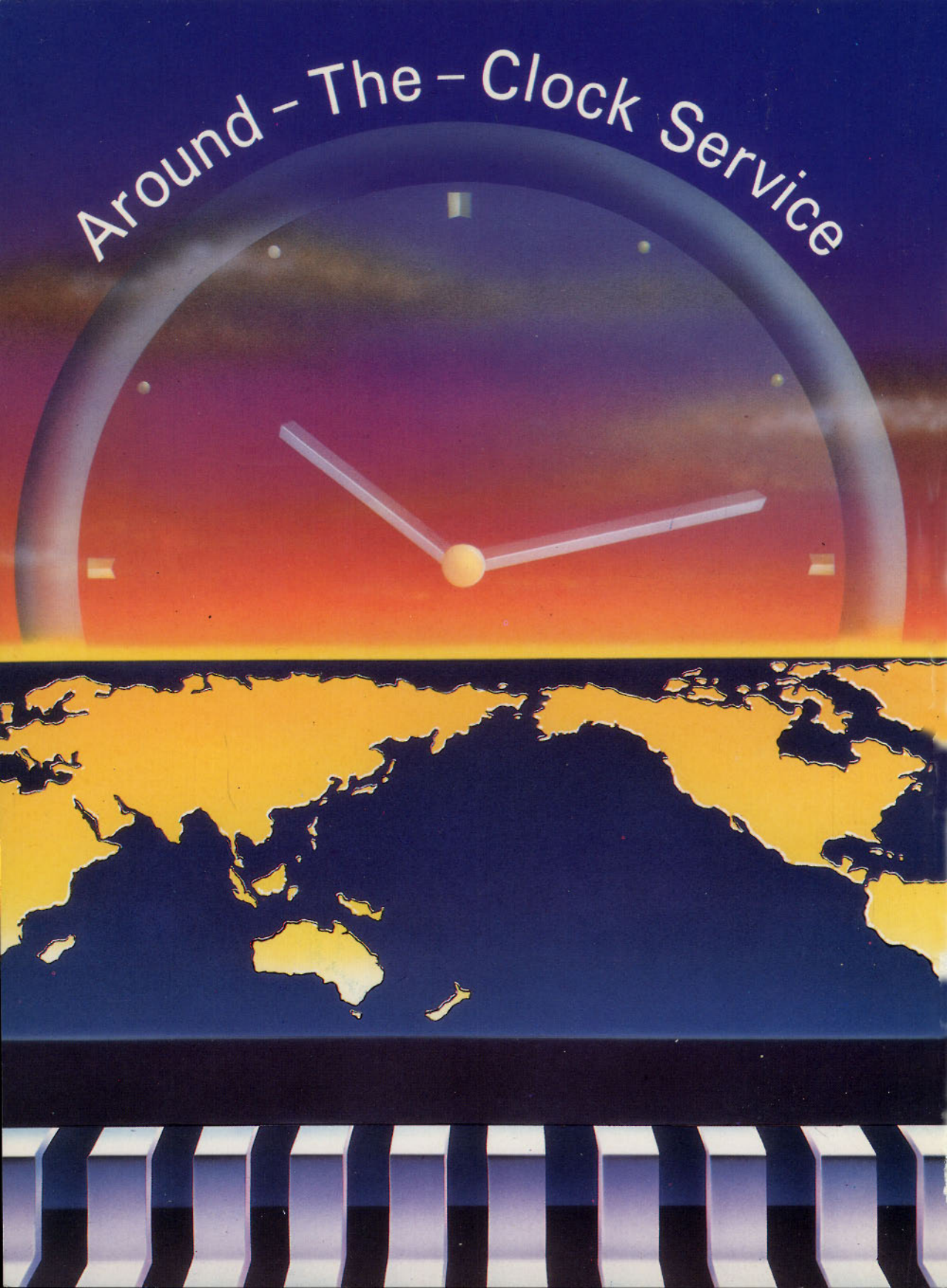
UNITED MICROELECTRONICS CORPORATION



Milestones in UMC's History

May 1980 -- Company formally established
Apr. 1982 -- Production began
Dec. 1983 -- Ranked first in profitability in Taiwan Top 500
Aug. 1984 -- Began VLSI process and product development
Nov. 1984 -- U.S. design facility established
Oct. 1985 -- Developed 1.5 micron 64K SRAM VLSI
Apr. 1986 -- Developed 1.25 micron VLSI process with TRW
June 1986 -- Contracted with SMC of U.S. on computer IC development
Jan. 1987 -- Dataquest listed UMC 32nd in worldwide MOS sales
Dec. 1987 -- Construction of US$260 million ULSI Plant began
Aug. 1988 -- Construction of new R&D office building began
Dec. 1988 -- Developed 1.0 micron 256K SRAM and 1M ROM
June 1989 -- ULSI Plant began production

Around-The-Clock Service



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Computer ICs

MEDICAL APPLICATIONS

UMC's products are not authorized for use in medical applications, including, but not limited to, use in life support devices without the written consent of the appropriate officer of UMC. Buyers of UMC products are requested to notify UMC sales offices when planning to use the products in the applications which involve medical applications.

NOTICE

The information in this document has been carefully checked. However, no responsibility is assumed for inaccuracies.

The example of an applied circuit or combination with other equipment shown herein indicates characteristics and performance of semiconductor-applied products. UMC shall assume no responsibility for any problem involving a patent caused when applying the descriptions in the example.

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TABLE OF CONTENTS

A. Contents
- ☐ Numerical
- ☐ Functional
- ☐ Cross-Reference

1. Microprocessor
2. PC Mainboard I
3. Display
4. Storage
5. I/O And Peripherals
6. PC Mainboard II

B. General Information
- ☐ MOS Handling
- ☐ Quality/Reliability
- ☐ Packaging Information
- ☐ Representatives/Distributors

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CONTENTS

Numerical Contents

Part No.	Description	Page
UM2661	Enhanced Programmable Communications Interface (EPCI)	5-3
UM487	HCGA Controller	3-3
UM587	VGA Controller	3-17
UM6502/07/12	8-bit Microprocessor	1-3
UM6502E	8-bit Microprocessor	1-14
UM6522/A	Versatile Interface Adapter (VIA)	5-18
UM6532/A	RAM, I/O; Timer Array	5-35
UM6551	Asynchronous Communication Interface Adapter (ACIA)	5-42
UM6845/A/B	CRT Controller	3-45
UM6845R/RA/RB	CRT Controller	3-68
UM6845E/EA/EB	CRT Controller	3-81
UM70C171/-50/-65	Color Palette with Triple 6-Bit DAC	3-98
UM74HCT590	8 bit Binary Counter with Output Registers	2-3
UM74HCT612	Memory Mapper	2-7
UM74HCT646	Octal Bus Transceiver and Register	2-13
UM82C01	Capacitance Keyboard Encoder (CKE)	5-51
UM82C088	PC/XT Integration Chip	2-19
UM82C11-C	Printer Adapter Interface (PAI)	5-62
UM82C206	Integrated Peripheral Controller	6-3
UM82C210 Series	386SX/286 AT Chip Set	6-67
UM82C211	System Controller	6-69
UM82C212	Memory Controller	6-74
UM82C215	Data/Address Buffer	6-85
UM82C230 Series	286 PC/AT Chip Set	6-87
UM82C231	System/Memory Controller	6-90
UM82C232	Data Buffer	6-116
UM82C380 Series	386 PC/AT Chip Set	6-130
UM82C381	System Controller	6-136
UM82C382	Address Buffer	6-145
UM82C383	Data Buffer	6-149
UM82C384	Memory Controller	6-154
UM82C388	INTEL Cache Interface	6-165
UM82C389	AUSTEK Cache Interface	6-177
UM82C284-10/-12	Clock Generator and Ready Interface	2-41
UM82C288-10/-12	Bus Controller	2-48

CONTENTS

Part No.	Description	Page
UM82C450	Asynchronous Communication Element (ACE)	5-71
UM82C451	Parallel/Asynchronous Communication Element	5-86
UM82C452	Single Chip Multi-I/O	5-111
UM82C54/-2	CMOS Programmable Interval Timer	2-63
UM82C550	Asynchronous Communication Element with 16-bit FIFO	5-135
UM82C55A	CMOS Programmable Peripheral Interface	2-79
UM82C59A-2	CMOS Programmable Interrupt Controller	2-98
UM82C8167	Real-Time Clock (RTC)	5-158
UM82C84AE	CMOS Clock Generator and Driver	2-115
UM82C852	Multi I/O For XT	5-165
UM82152	Cache Controller	2-122
UM8237AE/-4/-5	Programmable DMA Controller (DMAC)	2-126
UM82450	Asynchronous Communication Element (ACE)	5-188
UM8250A	Asynchronouc Communication Element (ACE)	5-204
UM8250B	Asynchronous Communication Element	5-219
UM8253/-5	Programmable Interval Timer	2-142
UM8259A-2	Programmable Interrupt Controller	2-153
UM8272A/A-4	Floppy Disk Controller	4-3
UM83C001	Hard Disk Controller	4-24
UM83C002	RAM Buffer Controller	4-44
UM83C003	Hard Disk Controller Interface	4-53
UM83C004	Hard Disk Controller Interface	4-57
UM83C021	Hard Disk Controller	4-61
UM83C022	AT HDC Interface	4-80
UM8326/B	Floppy Disk Data Separator (FDDS)	4-96
UM8388	Single-Chip Floppy Disk Controller	4-101
UM8397	Single-Chip Floppy Disk Controller	4-113
UM8398	Single-Chip Floppy Disk Controller	4-130

Functional Contents

Part No.	Description	Remarks	Page
MICROPROCESSOR			
UM6502/07/12	8-bit Microprocessor	1, 2, 3, 4 MHz Versions	1-3
UM6502E	8-bit Microprocessor	1, 2, 3, 4 MHz Versions	1-14
PC MAINBOARD I			
UM74HCT590	8 bit Binary Counter with Output Registers	–	2-3
UM74HCT612	Memory Mapper	–	2-7
UM74HCT646	Octal Bus Transceiver and Register	–	2-13
UM82C088	PC/XT Integration-Chip	10 MHz Version	2-19
UM82C284-10/-12	Clock Generator and Ready Interface	–	2-41
UM82C288-10/-12	Bus Controller	–	2-48
UM82C54/-2	CMOS Programmable Interval Timer	–	2-63
UM82C55A	CMOS Programmable Peripheral Interface	–	2-79
UM82C59A-2	CMOS Programmable Interrupt Controller	–	2-98
UM82C84AE	CMOS Clock Generator and Driver	–	2-115
UM82152	Cache Controller	–	2-122
UM8237AE/-4/-5	Programmable DMA Controller (DMAC)	–	2-126
UM8253/-5	Programmable Interval Timer	–	2-142
UM8259A-2	Programmable Interrupt Controller	–	2-153
PC MAINBOARD II			
UM82C206	Integrated Peripheral Controller	16, 20 MHz Versions	6-3
UM82C210 Series	386SX/286 AT Chip Set	16, 20 MHz Versions	6-67
UM82C211	System Controller	16, 20 MHz Versions	6-69
UM82C212	Memory Controller	16, 20 MHz Versions	6-74
UM82C215	Data/Address Buffer	16, 20 MHz Versions	6-85
UM82C230 Series	286 PC/AT Chip Set	12 MHz Version	6-87
UM82C231	System/Memory Controller	12 MHz Version	6-90
UM82C232	Data Buffer	12 MHz Version	6-116
UM82C380 Series	386 PC/AT Chip Set	20, 25 MHz Versions	6-130
UM82C381	System Controller	20, 25 MHz Versions	6-136
UM82C382	Address Buffer	20, 25 MHz Versions	6-145
UM82C383	Data Buffer	20, 25 MHz Versions	6-149
UM82C384	Memory Controller	20, 25 MHz Versions	6-154
UM82C388	INTEL Cache Interface	20, 25 MHz Versions	6-165
UM82C389	AUSTEK Cache Interface	20, 25 MHz Versions	6-177
DISPLAY			
UM487	HCGA Controller	–	3-3
UM587	VGA Controller	–	3-17
UM6845/A/B	CRT Controller	1, 1.5, 2 MHz Versions	3-45
UM6845R/RA/RB	CRT Controller	1, 2, 3 MHz Versions	3-68
UM6845E/EA/EB	CRT Controller	1, 2, 3 MHz Versions	3-81
UM70C171/-50/-65	Color Palette with Triple 6-Bit DAC	35, 50, 65 MHz Versions	3-98

Part No.	Description	Remarks	Page
STORAGE			
UM8272A/A-4	Floppy Disk Controller	4, 8 MHz Versions	4-3
UM83C001	Hard Disk Controller	For PC/XT H. D. C	4-24
UM83C002	RAM Buffer Controller	–	4-44
UM83C003	Hard Disk Controller Interface	For PC/XT MFM H. D. C.	4-53
UM83C004	Hard Disk Controller Interface	For PC/XT MFM/RLL H. D. C.	4-57
UM83C021	Hard Disk Controller	For PC/AT H. D. C.	4-61
UM83C022	AT HDC Interface	For PC/AT H. D. C.	4-80
UM8326/B	Floppy Disk Data Separator (FDDS)	4, 8 MHz Versions	4-96
UM8388	Single-Chip Floppy Disk Controller	Special Design For IBM PC	4-101
UM8397	Single-Chip Floppy Disk Controller	Design For IBM PC XT	4-113
UM8398	Single-Chip Floppy Disk Controller	Special Design For IBM PC	4-130
I/O AND PERIPHERALS			
UM2661	Enhanced Programmable Communications Interface (EPCI)	Three Baud Rates	5-3
UM6522/A	Versatile Interface Adapter (VIA)	1, 2 MHz Versions	5-18
UM6532/A	RAM, I/O, Timer Array	1, 2 MHz Versions	5-35
UM6551	Asynchronous Communication Interface Adapter (ACIA)	1, 2 MHz Versions	5-42
UM82C01	Capacitance Keyboard Encoder (CKE)	–	5-51
UM82C11-C	Printer Adapter Interface (PAI)	–	5-62
UM82C450	Asynchronous Communication Element (ACE)	–	5-71
UM82C451	Parallel/Asynchronous Communication Element	–	5-86
UM82C452	Single Chip Multi-I/O	–	5-111
UM82C550	Asynchronous Communications Element with FIFOs	–	5-135
UM82C8167	Real-Time Clock (RTC)	–	5-158
UM82C852	Multi I/O For XT	–	5-165
UM82450	Asynchronous Communication Element (ACE)	–	5-188
UM8250A	Asynchronous Communication Element (ACE)	–	5-204
UM8250B	Asynchronous Communication Element (ACE)	–	5-219

CROSS REFERENCE GUIDE

MICROPROCESSOR

UMC	ROCKWELL
UM6502	R6502

PC MAINBOARD

UMC	CHIPS	ACER	INTEL	HARRIS	AUSTEK
UM82C088		M1101			
UM82C206	CS82C206				
UM82C211	CS82C211				
UM82C212	CS82C212				
UM82C215	CS82C215				
UM82C284			iP82284		
UM82C288			i82288		
UM82C54				HD82C54	
UM82C55A				HD82C55	
UM8259A-2			iP8259A-2		
UM82C88				HD82C88	
UM82152					A38152
UM8237AE-5			iP8237A-5		
UM8253/-5			iP8253-5		
UM8259A-2			iP8259A-2		

DISPLAY

UMC	HITACHI	INMOS	OAK
UM587			OTI ϕ37–C
UM6845/A/B	HD6845S/68A45S/68B45S		
UM70C171/-50/-65		IMS G171S	

STORAGE

UMC	NEC	ZILOG	INTEL	SMC
UM8272A	μPD 765	Z765A	iP8272A	
UM8326				SMC FDC 9216

I/O AND PERIPHERALS

UMC	VTI	NS	SIS
UM82C11-C			SIS82C11
UM82C450			SIS82450
UM82C451	VTI16451		
UM82C452	VTI16452		
UM82C550		NS16550	
UM82C8167		NS58167	
UM82450		NS16450	
UM8250B		NS8250B	

Microprocessor

Part No.	Description	Page
UM6502/07/12	8-bit Microprocessor	1-3
UM6502E	8-bit Microprocessor	1-14

UM6502/07/12

8-bit Microprocessor

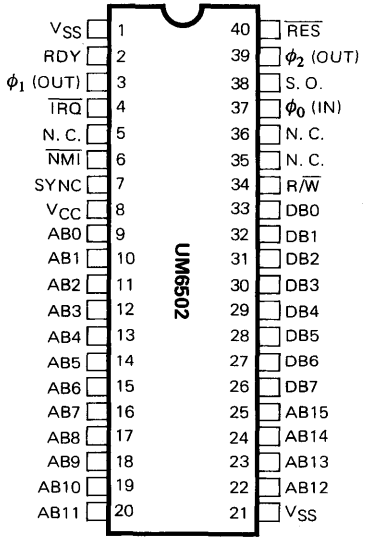
Features

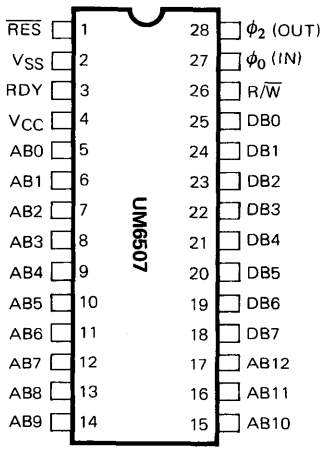
- Single 5V ± 5% power supply
- N channel, silicon gate, depletion load technology
- 56 instructions
- Decimal and binary arithmetic
- Thirteen addressing modes
- True indexing capability
- Programmable stack pointer
- Variable length stack
- Interrupt capability
- Non-maskable interrupt
- Bi-directional data bus
- Addressable memory range of up to 64K bytes
- "Ready" input
- Direct memory access capability
- Bus compatible with MC6800
- Choice of external or on-board clocks
- 1MHz, 2MHz, 3MHz and 4MHz versions
- On-chip clock options
  - –External single clock input
  - –Crystal time base input
- Pipeline architecture

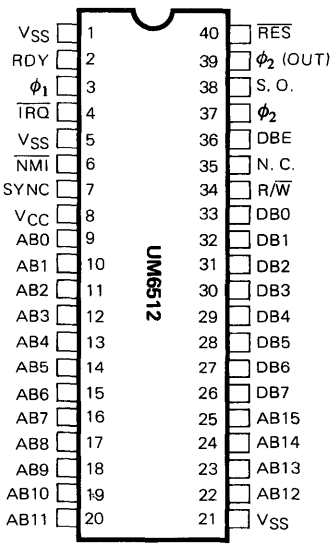
General Description

The UM6502/07/12 microprocessors are totally software compatible with one another. These products provide a wide selection of addressable memory range, interrupt input options and on-chip clock oscillators and drivers. The UM6502/07 on-chip clock versions are aimed at high performance, low cost applications where single phase inputs or crystals provide the time base. The UM6512 external clock version is geared to multiprocessor system applications where maximum timing control is mandatory. These products are bus compatible with the MC6800.

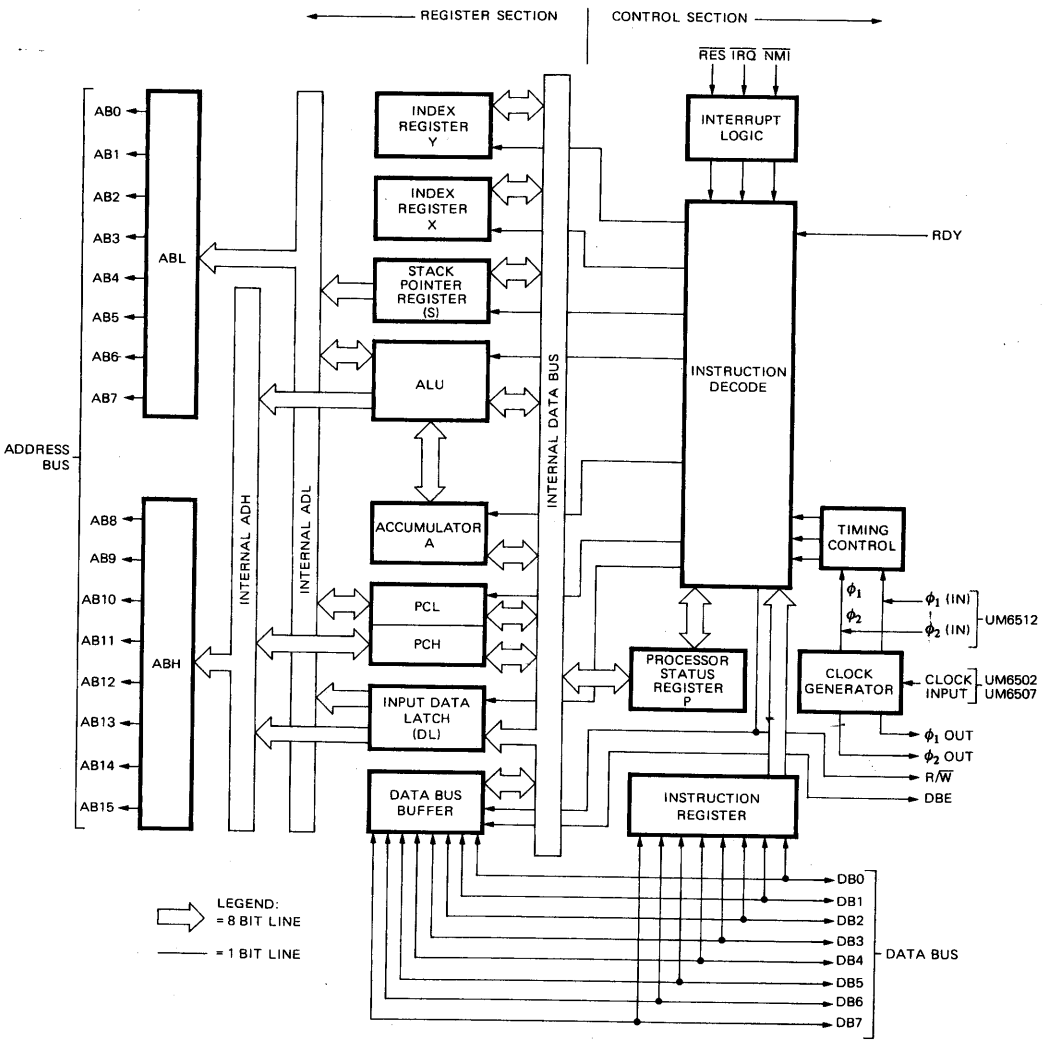
Pin Configurations







Block Diagram



Notes:

1. CLOCK GENERATOR IS NOT INCLUDED ON UM6512
2. ADDRESSING CAPABILITY AND CONTROL OPTIONS VARY WITH EACH PRODUCT.

Absolute Maximum Ratings*

Supply Voltage V_{CC}	−0.3 to +7.0V
Input Voltage V_{IN}	−0.3 to +7.0V
Operating Temperature T_A	0 to 70°C
Storage Temperature T_{STG}	−55 to +150°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

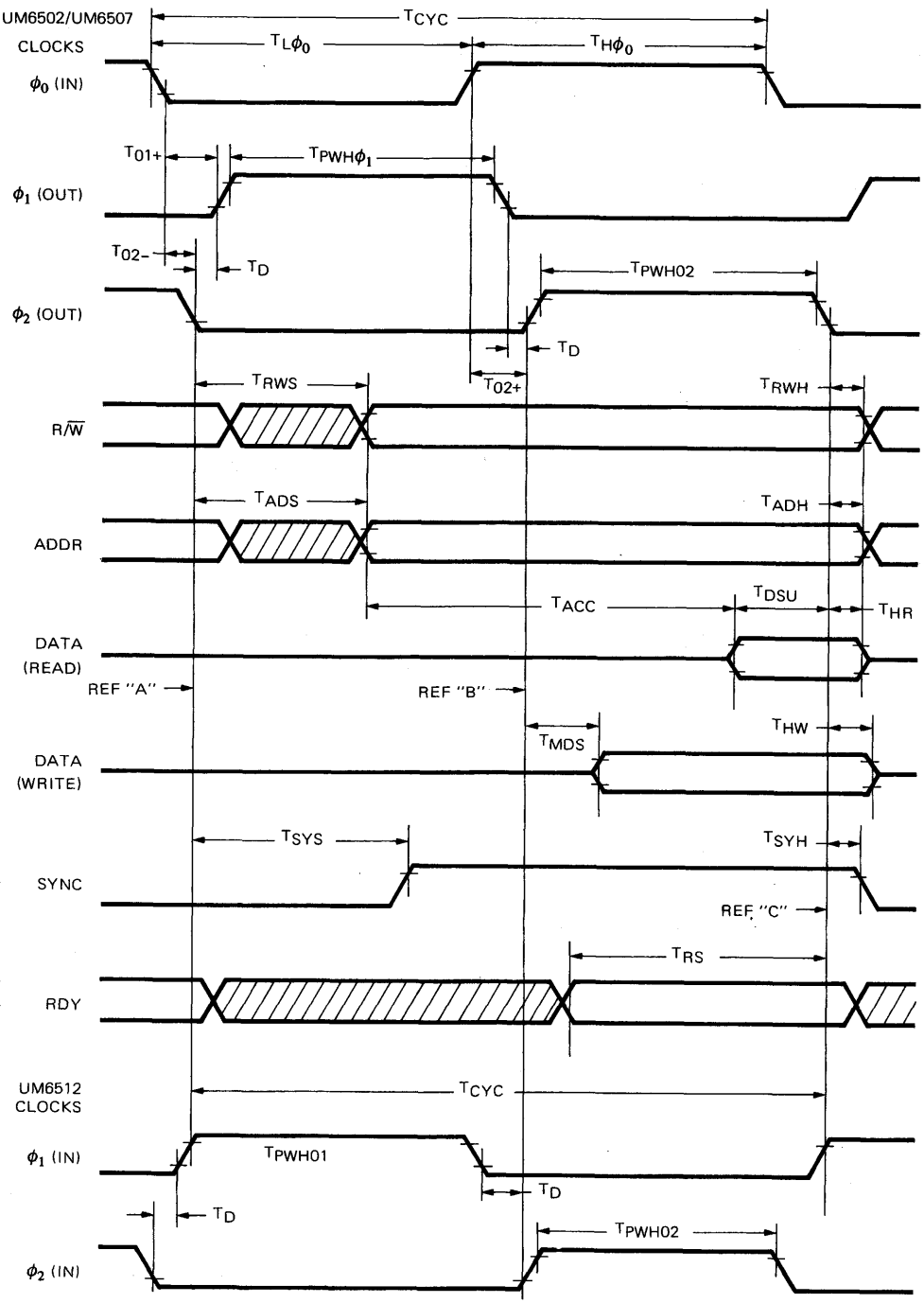
DC Electrical Characteristics

(V_{CC} = 5.0V ± 5%, T_A = 0 – 70°C)

(ϕ_1, ϕ_2 applies to UM6512, ϕ_0 (in) applies to UM6502/UM6507)

Symbol	Parameter	Min.	Max.	Unit
V_{IH}	Input High Voltage			
	Logic and ϕ_0 (in) for UM6502/UM6507 — 1, 2, 3 MHz	+ 2.0	V_{CC}	V
	Logic and ϕ_0 (in) for UM6502/UM6507 — 4 MHz	+ 3.3	V_{CC}	V
	ϕ_1 and ϕ_2 only for UM6512 — All Speeds	V_{CC} – 0.5	V_{CC} + 0.25	V
V_{IL}	Input Low Voltage			
	Logic, ϕ_0(in) (UM6502/UM6507)	–0.3	+0.8	
	ϕ_1, ϕ_2 (UM6512)	–0.3	+0.2	V
I_{IL}	Input Loading (V_{IN} = 0V, V_{CC} = 5.25V)			
	RDY, S.O.	–10	–300	μA
I_{IN}	Input Leakage Current (V_{IN} = 0 to 5.25V, V_{CC} = 0)			
	Logic (Excl. RDY, S.O.)	–	2.5	μA
	ϕ_1, ϕ_2 (UM6512)	–	100	μA
	ϕ_0(in) (UM6502/UM6507)	–	10.0	μA
I_{TSI}	Three-State (Off State) Input Current (V_{IN} = 0.4 to 2.4V, V_{CC} = 5.25V)			
	DB0-DB7	–	±10	μA
V_{OH}	Output High Voltage (I_{LOAD} = –100μAdc, V_{CC} = 4.75V) 1, 2 MHz	2.4	–	V
	SYNC, DB0-DB7, AB0-AB15, R/$\overline{W}$			
V_{OL}	Output Low Voltage (I_{LOAD} = 1.6mAdc, V_{CC} = 4.75V) 1, 2 MHz	–	0.4	V
	SYNC, DB0-DB7, AB0-AB15, R/$\overline{W}$			
P_D	Power Dissipation 1MHz and 2MHz (V_{CC} = 5.25V)	–	700	mW
C	Capacitance (V_{IN} = 0, T_A = 25°C, f = 1 MHz)			
C_{IN}	$\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, S.O., DBE	–	10	
	DB0-DB7	–	15	
C_{OUT}	AB0-AB15, R/$\overline{W}$, SYNC	–	12	pF
C_{ϕ_0} (in)	ϕ_0 (in) (UM6502/UM6507)	–	15	
C_{ϕ_1}	ϕ_1 (UM6512)	–	50	
C_{ϕ_2}	ϕ_2 (UM6512)	–	80	

Timing Waveforms



Dynamic Operating Characteristics

(V_{CC} = 5.0 ± 5%, T_A = 0° to 70°C)

Parameter	Symbol	1 MHz		2 MHz		3 MHz		4 MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
UM6512										
Cycle Time	T_{CYC}	1.00	40	0.50	40	0.33	40	0.25	40	μs
ϕ_1 Pulse Width	$T_{PWH\phi_1}$	430	–	215	–	150	–			ns
ϕ_2 Pulse Width	$T_{PWH\phi_2}$	470	–	235	–	160	–			ns
Delay Between ϕ_1 and ϕ_2	T_D	0	–	0	–	0	–			ns
ϕ_1 and ϕ_2 Rise and Fall Times(1)	T_R, T_F	0	25	0	20	0	15			ns
UM6502/UM6507										
Cycle Time	T_{CYC}	1.00	40	0.50	40	0.33	40	0.25	40	μs
$\phi_{0(IN)}$ Low Time(2)	$T_{L\phi_0}$	480	–	240	–	160	–	110	–	ns
$\phi_{0(IN)}$ High Time(2)	$T_{H\phi_0}$	460	–	240	–	160	–	115	–	ns
ϕ_0 Neg to ϕ_1 Pos Delay(5)	T_{01+}	10	70	10	70	10	70	10	70	ns
ϕ_0 Neg to ϕ_2 Neg Delay(5)	T_{02-}	5	65	5	65	5	65	5	65	ns
ϕ_0 Pos to ϕ_1 Neg Delay(5)	T_{01-}	5	65	5	65	5	65	5	65	ns
ϕ_0 Pos to ϕ_2 Pos Delay(5)	T_{02+}	15	75	15	75	15	75	15	75	ns
$\phi_{0(IN)}$ Rise and Fall Time(1)	T_{RO}, T_{FO}	0	30	0	20	0	15	0	10	ns
ϕ_1 (OUT), Pulse Width	$T_{PWH\phi_1}$	$T_{L\phi_0}$-20	$T_{L\phi_0}$	$T_{L\phi_0}$-20	$T_{L\phi_0}$	$T_{L\phi_0}$-20	$T_{L\phi_0}$	$T_{L\phi_0}$-20	$T_{L\phi_0}$	ns
ϕ_2 (OUT), Pulse Width	$T_{PWH\phi_2}$	$T_{L\phi_0}$-40	$T_{L\phi_0}$-10	$T_{L\phi_0}$-40	$T_{L\phi_0}$-40	$T_{L\phi_0}$-40	$T_{L\phi_0}$-10	$T_{L\phi_0}$-40	$T_{L\phi_0}$-10	ns
Delay Between ϕ_1 and ϕ_2	T_D	5	–	5	–	5	–	5	–	ns
ϕ_1 and ϕ_2 Rise and Fall Times(1, 3)	T_R, T_F	–	25	–	25	–	15	–	15	ns
UM6502/UM6507/UM6512										
R/W Setup Time	T_{RWS}	–	225	–	140	–	110	–	90	ns
R/W Hold Time	T_{RWH}	30	–	30	–	15	–	10	–	ns
Address Setup Time	T_{ADS}	–	225	–	140	–	110	–	90	ns
Address Hold Time	T_{ADH}	30	–	30	–	15	–	10	–	ns
Read Access Time	T_{ACC}	–	650	–	310	–	170	–	110	ns
Read Data Setup Time	T_{DSU}	100	–	50	–	50	–	50	–	ns
Read Data Hold Time	T_{HR}	10	–	10	–	10	–	10	–	ns
Write Data Setup Time	T_{MDS}	20	175	20	100	20	75	–	70	ns
Write Data Hold Time	T_{HW}	60	150	60	150	30	130	20	–	ns
Sync Setup Time	T_{SYS}	–	350	–	175	–	100	–	90	ns
Sync Hold Time	T_{SYH}	30	–	30	–	15	–	15	–	ns
RDY Setup Time(4)	T_{RS}	200	–	200	–	150	–	120	–	ns

Notes:

1. Measured between 10% and 90% points.
2. Measured at 50% point.
3. Load = 1 TTL load + 30 pF.
4. RDY must never switch states within T_{RS} to end of ϕ_2.
5. Load = 100 pF.
6. The 2 MHz devices are identified by an "A" suffix.
7. The 3 MHz devices are identified by a "B" suffix.
8. The 4 MHz devices are identified by a "C" suffix.

Timing Diagram Note:

Because the clock generation for the UM6502/UM6507 and UM6512 is different, the two clock timing sections are referenced to the main timing diagram by three reference lines marked REF 'A', REF 'B' and REF 'C'. Reference between the two sets of clock timings is without meaning. Timing parameters referring to these line and scale variations in the diagrams are of no consequence.

Pin Description

Clocks (ϕ_1, ϕ_2)
The UM6512 requires a two phase non-overlapping clock that runs at the V_{CC} voltage level.

The UM6502/UM6507 clocks are supplied with an internal clock generator. The frequency of these clocks is externally controlled. Clock generator circuits are shown elsewhere in this data sheet.

Address Bus (AB0-AB15)
(See sections on each microprocessor for respective address lines on these devices.)

These outputs are TTL compatible, capable of driving one standard TTL load and 130 pF.

Data Bus (DB0-DB7)
Eight pins are used for the data bus. This is a bidirectional bus, transferring data to and from the device and peripherals. The outputs are three-state buffers, capable of driving one standard TTL load and 130 pF.

Data Bus Enable (DBE)
This TTL compatible input allows external control of the three-state data output buffers and will enable the microprocessor bus driver when in the high state. In normal operation DBE would be driven by the phase two (ϕ_2) clock, thus allowing data output from the microprocessor only during ϕ_2. During the read cycle, the data bus drivers are internally disabled, becoming essentially an open circuit. To disable the data bus drivers externally, DEB should be held low. This signal is available on the UM6512 only.

Ready (RDY)
This input signal allows the user to halt the microprocessor on all cycles except write cycles. A negative transition to the low state during, or coincident with phase one, (ϕ_1) will halt the microprocessor with the output address lines reflecting the current address being fetched. This condition will remain through a subsequent phase two (ϕ_2) in which the Ready signal is low. This feature allows microprocessor interfacing with low speed PROMs as well as fast (max. 2 cycle) Direct Memory Access (DMA). If ready is low during a write cycle, it is ignored until the following read operation. Ready transitions must not be permitted during ϕ_2 time.

Interrupt Request ($\overline{IRQ}$)
This TTL level input requests that an interrupt sequence begin within the microprocessor. The microprocessor will complete the current instruction being executed before recognizing the request. At the time, the interrupt mask bit in the Status Code Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, therefore transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3KΩ external resistor should be used for proper wire-OR operation.

Non-Maskable Interrupt ($\overline{NMI}$)
A negative going transition on this input requests that a non-maskable interrupt sequence be generated within the microprocessor.

$\overline{NMI}$ is an unconditional interrupt. Following completion of the current instruction, the sequence of operations defined for $\overline{IRQ}$ will be performed, regardless of the state interrupt mask flag. The vector address loaded into the program counter, low and high, are locations FFFA and FFFB respectively, thereby transferring program control to the memory vector located at these addresses. The instructions loaded at these locations cause the microprocessor to branch to a non-maskable interrupt routine in memory.

$\overline{NMI}$ also requires an external 3KΩ resistor to V_{CC} for proper wire-OR operations.

Inputs $\overline{IRQ}$ and $\overline{NMI}$ are hardware interrupt lines that are sampled during ϕ_2 (phase 2) and will begin the appropriate interrupt routine on ϕ_1 (phase 1) following the completion of the current instruction.

Set Overflow Flag (S. O.)
A NEGATIVE going edge on this input sets the overflow bit in the Status Code Register. This signal is sampled on the trailing edge of ϕ_1.

SYNC
This output line is provided to identify those cycles in which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during ϕ_1 of an OPCODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the ϕ_1 clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.

Reset ($\overline{RES}$)
This input is used to reset or start the microprocessor from a power down condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge is detected on the input, the microprocessor will immediately begin the reset sequence.

After a system initialization time of six clock cycles, the mask interrupt flag will be set and the microprocessor will load the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control.

After V_{CC} reaches 4.75 volts in a power up routine, reset must be held low for at least two clock cycles. At this time the R/$\overline{W}$ and SYNC signals will become valid. When the reset signal goes high following these two clock cycles, the microprocessor will proceed with the normal reset procedure detailed above.

Read/Write (R/$\overline{W}$)
This output signal is used to control the direction of data transfers between the processor and other circuits on the data bus. A high level on R/$\overline{W}$ signifies data into the processor; a low is for the data transfer out of the processor.

Programming Characteristics

INSTRUCTION SET – ALPHABETIC SEQUENCE

ADC	Add Memory to Accumulator with Carry
AND	"AND" Memory with Accumulator
ASL	Shift left One Bit (Memory or Accumulator)
BCC	Branch on Carry Clear
BCS	Branch on Carry Set
BEQ	Branch on Result Zero
BIT	Test Bits in Memory with Accumulator
BMI	Branch on Result Minus
BNE	Branch on Result not Zero
BPL	Branch on Result Plus
BNK	Force Break
BVC	Branch on Overflow Clear
BVS	Branch on Overflow Set
CLC	Clear Carry Flag
CLD	Clear Decimal Mode
CLI	Clear Interrupt Disable Bit
CLV	Clear Overflow Flag
CMP	Compare Memory and Accumulator
CPX	Compare Memory and Index X
CPY	Compare Memory and Index Y
DEC	Decrement Memory by One
DEX	Decrement Index X by One
DEY	Decrement Index Y by One
EOR	"Exclusive-OR" Memory with Accumulator
INC	Increment Memory by One
INX	Increment Index X by One
INY	Increment Index Y by One
JMP	Jump to New Location
JSR	Jump to New Location Saving Return Address
LDA	Load Accumulator with Memory
LDX	Load Index X with Memory
LDY	Load Index Y with Memory
LSR	Shift One Bit Right (Memory or Accumulator)
NOP	No Operation
ORA	"OR" Memory with Accumulator
PHA	Push Accumulator on Stack
PHP	Push Processor Status on Stack
PLA	Pull Accumulator from Stack
PLP	Pull Processor Status from Stack
ROL	Rotate One Bit Left (Memory or Accumulator)
ROR	Rotate One Bit Right (Memory or Accumulator)
RTI	Return from Interrupt
RTS	Return from Subroutine
SBC	Subtract Memory from Accumulator with Borrow
SEC	Set Carry Flag
SED	Set Decimal Mode
SEI	Set Interrupt Disable Status
STA	Store Accumulator in Memory
STX	Store Index X in Memory
STY	Store Index Y in Memory
TAX	Transfer Accumulator to Index X
TAY	Transfer Accumulator to Index Y
TSX	Transfer Stack Pointer to Index X
TXA	Transfer Index X to Accumulator
TXS	Transfer Index X to Stack Pointer
TYA	Transfer Index Y to Accumulator

ADDRESSING MODES

Accumulator Addressing
This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

Immediate Addressing
In immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

Absolute Addressing
In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 65K bytes of addressable memory.

Zero Page Addressing
The zero page instructions allow for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in a significant increase in code efficiency.

Indexed Zero Page Addressing – (X, Y indexing)
This form of addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y." The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location on page zero. In addition due to the "Zero Page" addressing

nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.

Indexed Absolute Addressing – (X, Y indexing)
This form of addressing is used in conjunction with the X and Y index registers and is referred to as "Absolute, X," and "Absolute, Y." The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index, or count value, and the instruction to contain the base address. This type of indexing allows any location reference and the index to modify multiple fields, resulting in reduced coding and execution time.

Implied Addressing
In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

Relative Addressing
Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

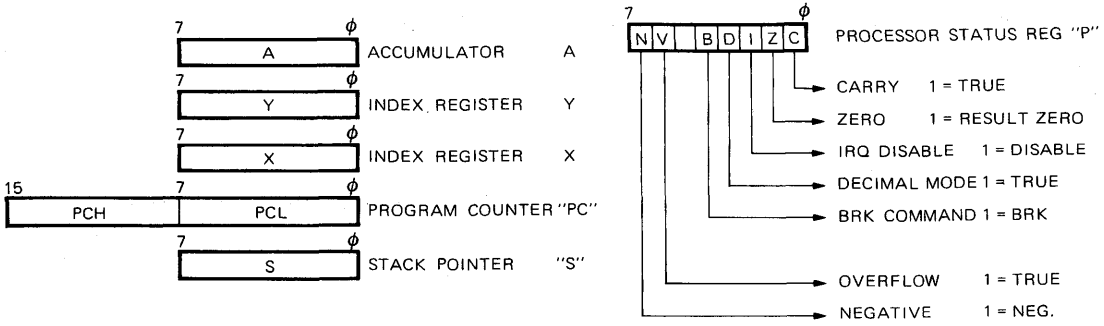
The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set to the next instruction. The range of the offset is-128 to + 127 bytes from the next instruction.

Indexed Indirect Addressing
In indexed indirect addressing (referred to as "Indirect, X"), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location on page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be on page zero.

Indirect Indexed Addressing
In indirect indexed addressing (referred to as "Indirect, Y"), the second byte of the instruction points to a memory location on page zero. The content of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

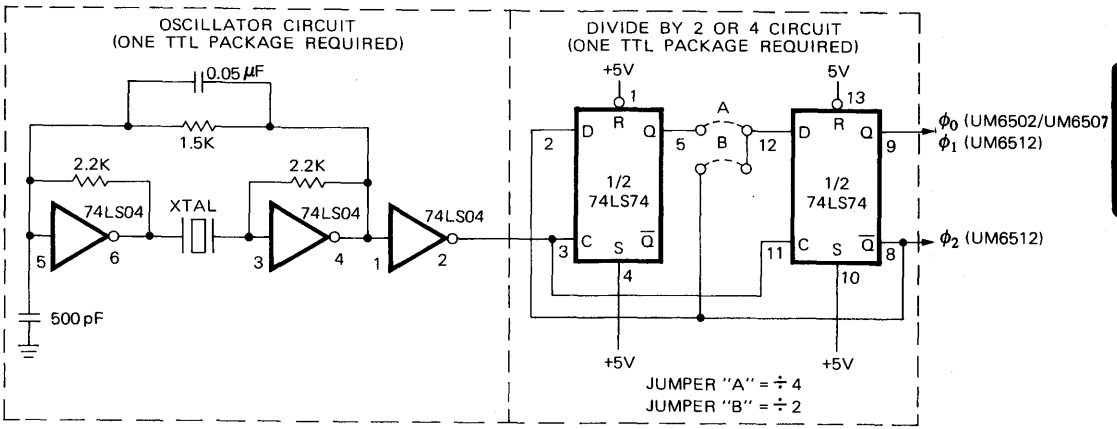
Absolute Indirect
The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The content of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter.

PROGRAMMING MODEL

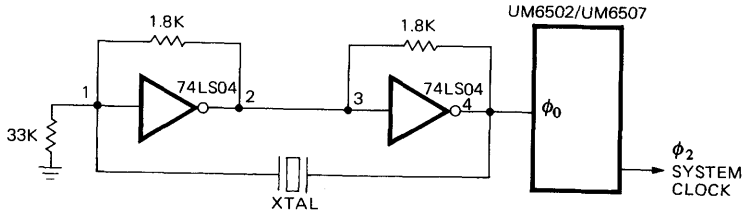


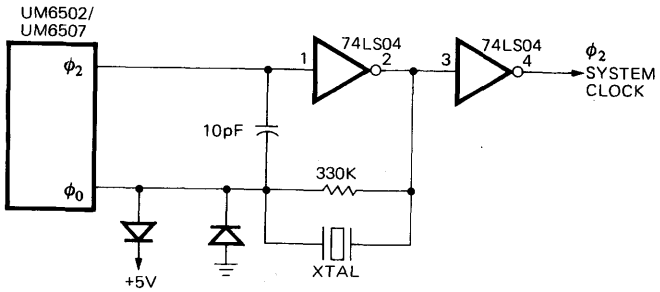
Clock Generation Circuits*

* Crystals used are CTS Knight MP Series or equivalents. (Series Mode)



Crystal Frequency	Output Frequency	
	÷2	÷4
3.579545 MHz	1.7897 MHz	0.894886 MHz
4.194304 MHz	2.097152 MHz	1.048576 MHz





Instruction Set

Instructions				Immediate			Absolute			Zero page			Accum.			Implied			(Ind. X)			((Ind. Y)		
Mnemonic			Operation	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#
A	D	C	A + M + C → A (4) (1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2
A	N	D	A ∧ M → A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2
A	S	L	C ← [7 0] ← 0				0E	6	3	06	5	2	0A	2	1									
B	C	C	BRANCH ON C = 0 (2)																					
B	C	S	BRANCH ON C = 1 (2)																					
B	E	Q	BRANCH ON Z = 1 (2)																					
B	I	T	A ∧ M				2C	4	3	24	3	2												
B	M	I	BRANCH ON N = 1 (2)																					
B	N	E	BRANCH ON Z = 0 (2)																					
B	P	L	BRANCH ON N = 0 (2)																					
B	R	K	BREAK													00	7	1						
B	V	C	BRANCH ON V = 0 (2)																					
B	V	S	BRANCH ON V = 1 (2)																					
C	L	C	0 → C													18	2	1						
C	L	D	0 → D													D8	2	1						
C	L	I	0 → 1													58	2	1						
C	L	V	0 → V													B8	2	1						
C	M	P	A − M	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2
C	P	X	X − M	E0	2	2	EC	4	3	E4	3	2												
C	P	Y	Y − M	C0	2	2	CC	4	3	C4	3	2												
D	E	C	M − 1 → M				CE	6	3	C6	5	2												
D	E	X	X − 1 → X													CA	2	1						
D	E	Y	Y − 1 → Y													88	2	1						
E	O	R	A V M → A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2
I	N	C	M + 1 → M				EE	6	3	E6	5	2												
I	N	X	X + 1 → X													E8	2	1						
I	N	Y	Y + 1 → Y													C8	2	1						
J	M	P	JUMP TO NEW LOC				4C	3	3															
J	S	R	JUMP SUB				20	6	3															
L	D	A	M A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2
L	D	X	M → X (1)	A2	2	2	AE	4	3	A6	3	2												
L	D	Y	M → Y (1)	A0	2	2	AC	4	3	A4	3	2												
L	S	R	0 → [7 0] → C				4E	6	3	46	5	2	4A	2	1									
N	O	P	NO OPERATION													EA	2	1						
O	R	A	A V M → A	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2
P	H	A	A → MS S − 1 → S													48	3	1						
P	H	P	P → MS S − 1 → S													08	3	2						
P	L	A	S + 1 → S MS → A													68	4	1						
P	L	P	S + 1 → S MS → P													28	4	1						
R	O	L	← [7 0] ← [C] ↵				2E	6	3	26	5	2	2A	2	1									
R	O	R	↳ [C] → [0 7] →				6E	6	3	66	5	2	6A	2	1									
R	T	I	RTRN INT													40	6	1						
R	T	S	RTRN SUB													60	6	1						
S	B	C	A − M − C̄ → A (1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2
S	E	C	1 → C													38	2	1						
S	E	D	1 → D													F8	2	1						
S	E	I	1 → 1													78	2	1						
S	T	A	A → M				8D	4	3	85	3	2							81	6	2	91	6	2
S	T	X	X → M				8E	4	3	86	3	2												
S	T	Y	Y → M				8C	4	3	84	3	2												
T	A	X	A → X													AA	2	1						
T	A	Y	A → Y													A8	2	1						
T	S	X	S → X													BA	2	1						
T	X	A	X → A													8A	2	1						
T	X	S	X → S													9A	2	1						
T	Y	A	Y → A													98	2	1						

(1) ADD 1 TO N IF PAGE BOUNDARY IS CROSSED
(2) ADD 1 TO N IF BRANCH OCCURS TO SAME PAGE
ADD 2 TO N IF BRANCH OCCURS TO DIFFERENT PAGE
(3) CARRY NOT = BORROW
(4) IF IN DECIMAL MODE Z FLAG IS INVALID
ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT

Z Page. X			Abs. X			Abs. Y			Relative			Indirect			Z Page. Y			Processor Status Codes								Mnemonic
OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	7	6	5	4	3	2	1	0	
																		N	V		B	D	I	Z	C	
75	4	2	7D	4	3	79	4	3										N	V	.	.	.	.	Z	C	A D C
35	4	2	3D	4	3	39	4	3										N	.	.	.	.	.	Z	.	A N C
16	6	2	1E	7	3													N	.	.	.	.	.	Z	C	A S L
									90	7	2							.	.	.	.	.	.	.	.	B C C
									B0	2	2							.	.	.	.	.	.	.	.	B C S
									F0	2	2															B E Q
																		M_7	M_6	.	.	.	.	Z	.	B I T
									30	2	2							.	.	.	.	.	.	.	.	B M I
									D0	2	2							.	.	.	.	.	.	.	.	B N E
									10	2	2							.	.	.	.	.	.	.	.	B P L
																		.	.	.	1	.	1	.	.	B R K
									50	2	2							.	.	.	.	.	.	.	.	B V C
									70	2	2							.	.	.	.	.	.	.	.	B V S
																		.	.	.	.	.	.	.	0	C L C
																		.	.	.	.	0	.	.	.	C L D
																		.	.	.	.	.	0	.	.	C L I
D5	4	2	DD	4	3	D9	4	3										.	0	.	.	.	.	.	.	C L V
																		N	.	.	.	.	.	Z	C	C M P
																		N	.	.	.	.	.	Z	C	C P X
																		N	.	.	.	.	.	Z	C	C P Y
D6	6	2	DE	7	3													N	.	.	.	.	.	Z	.	D E C
																		N	.	.	.	.	.	Z	.	D E X
55	4	2	5D	4	3	59	4	3										N	.	.	.	.	.	Z	.	D E Y
F6	6	2	FE	7	3													N	.	.	.	.	.	Z	.	E O R
																		N	.	.	.	.	.	Z	.	I N C
																		N	.	.	.	.	.	Z	.	I N X
												6C	5	3				N	.	.	.	.	.	Z	.	I N Y
																		.	.	.	.	.	.	.	.	J M P
B5	4	2	BD	4	3	B9	4	3										.	.	.	.	.	.	.	.	J S R
																		N	.	.	.	.	.	Z	.	L D A
						BE	4	3							B6	4	2	N	.	.	.	.	.	Z	.	L D X
B4	4	2	BC	4	3													N	.	.	.	.	.	Z	.	L D Y
56	6	2	5E	7	3													0	.	.	.	.	.	Z	C	L S R
																		.	.	.	.	.	.	.	.	L O P
15	4	2	1D	4	3	19	4	3										N	.	.	.	.	.	Z	.	O R A
																		.	.	.	.	.	.	.	.	P H A
																		.	.	.	.	.	.	.	.	P H P
																		N	.	.	.	.	.	Z	.	P L A
36	6	2	3E	7	3																(RESTORED)					P L P
																		N	.	.	.	.	.	Z	C	R L O
76	6	2	7E	7	3													N	.	.	.	.	.	Z	C	R O R
																					(RESTORED)					R O T
																		.	.	.	.	.	.	.	.	R T I
F5	4	2	FD	4	3	F9	4	3										N	V	.	.	.	.	Z	(3)	S T S
																		.	.	.	.	1	.	.	1	S B C
																		.	.	.	.	.	.	.	.	S E D
95	4	2	9D	5	3	99	5	3										.	.	.	.	.	1	.	.	S E I
																		.	.	.	.	.	.	.	.	S T A
94	4	2													96	4	2	.	.	.	.	.	.	.	.	S T X
																		.	.	.	.	.	.	.	.	S T Y
																		N	.	.	.	.	.	Z	.	T A X
																		N	.	.	.	.	.	Z	.	T A Y
																		N	.	.	.	.	.	Z	.	T S X
																		N	.	.	.	.	.	Z	.	T X S
																		.	.	.	.	.	.	.	.	T Y A
																		N	.	.	.	.	.	Z	.	T Y S

X INDEX X
Y INDEX Y
A ACCUMULATOR
M MEMORY PER EFFECTIVE ADDRESS
Ms MEMORY PER STACK POINTER

\+ ADD
– SUBTRACT
∧ AND
V OR
⊻ EXCLUSIVE OR

M_7 MEMORY BIT 7
M_6 MEMORY BIT 6
n NO. CYCLES
NO. BYTES

Ordering Information

1 MHz	2 MHz	3 MHz	4 MHz
UM6502	UM6502A	UM6502B	UM6502C
UM6507	–	–	–
UM6512	UM6512A	UM6512B	UM6512C

Part Number	Clocks	Pins	IRQ	NMI	RYD	Addressing
UM6502	On-Chip	40	√	√	√	64K
UM6507	On-Chip	28			√	8K
UM6512	External	40	√	√	√	64K

UM6502E

8-Bit Microprocessor

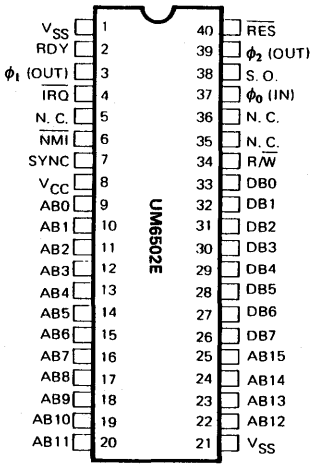
Features

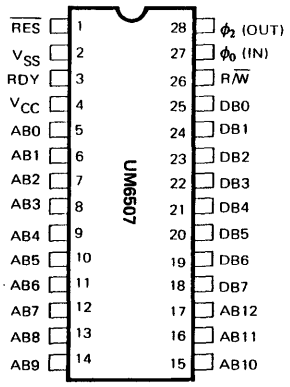
- UM6502E is the enhanced timing version of UM6502
- Single 5V ± 5% power supply
- N channel, silicon gate, depletion load technology
- 56 instructions
- Decimal and binary arithmetic
- Thirteen addressing modes
- True indexing capability
- Programmable stack pointer
- Variable length stack
- Interrupt capability
- Non-Maskable interrupt
- Bi-directional data bus
- Addressable memory range of up to 64K bytes
- "Ready" input
- Direct memory access capability
- Bus compatible with MC6800
- Choice of external or on-board clocks
- 1MHz, 2MHz, 3MHz and 4MHz versions
- On-chip clock options
  - External single clock input
  - Crystal time base input
- Pipeline architecture

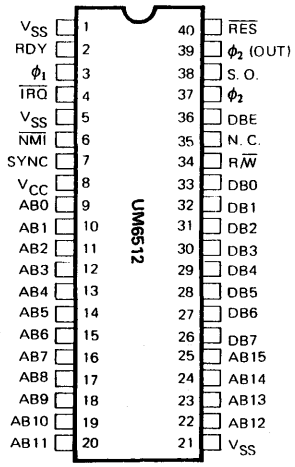
General Description

The UM6502/UM6502E/UM6507/UM6512 microprocessors are totally software compatible with one another. These products provide a selection of addressable memory range, interrupt input options and on-chip clock oscillators and drivers. The UM6502/UM6502E/UM6507 on-chip clock versions are aimed at high performance, low cost applications where single phase inputs or crystals provide the time base. The UM6512 external clock version is geared for the multi-processor system applications where maximum timing control is mandatory. These products are bus compatible with the MC6800 product offering.

Pin Configurations







Absolute Maximum Ratings*

Supply Voltage V_{CC} . . . . . −0.3 to +7.0V
Input Voltage V_{in} . . . . . −0.3 to +7.0V
Operating Temperature T_A . . . . . 0 to 70°C
Storage Temperature T_{STG} . . . . . −55 to +150°C

*Comments

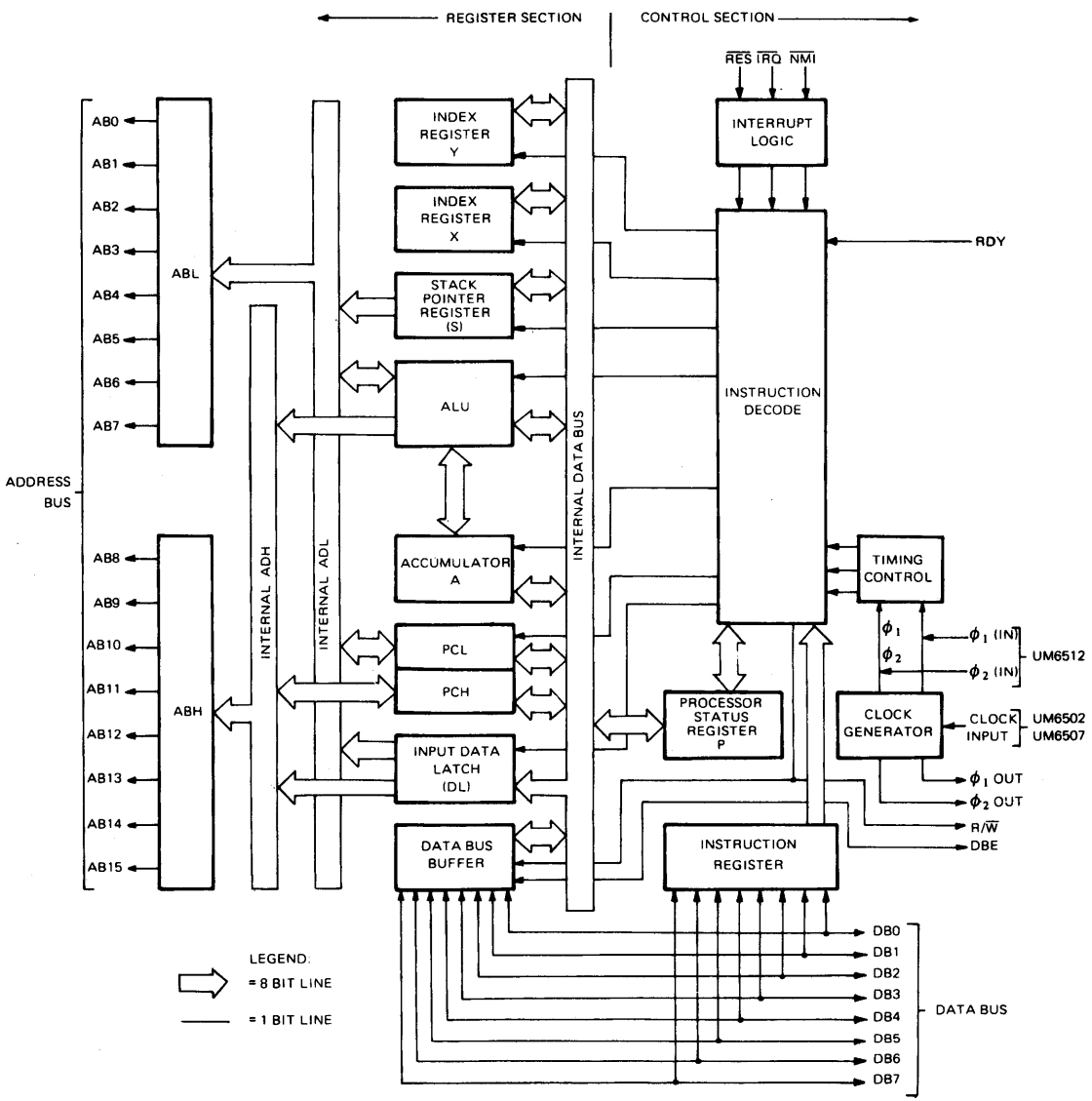
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{CC} = 5.0V ± 5%, T_A = 0 − 70°C)

(ϕ_1, ϕ_2 applies to UM6512, $\phi_{0(in)}$ applies to UM6502/UM6502E/UM6507)

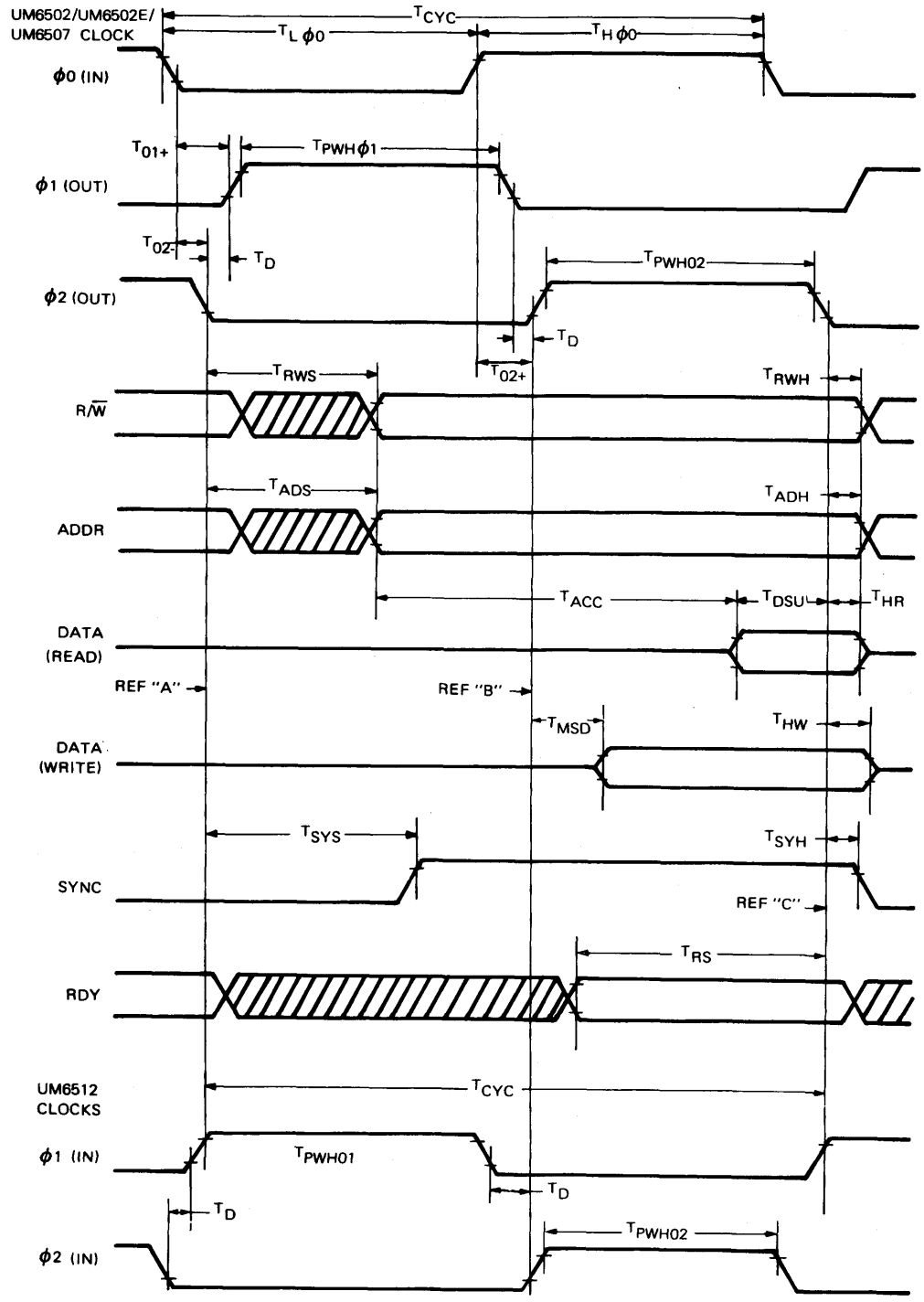
Symbol	Parameter	Min.	Max.	Unit
V_{IH}	Input High Voltage			
	Logic and ϕ0 (in) for UM6502/UM6502E/UM6507 — 1, 2, 3 MHz	+ 2.0	V_{CC}	V
	Logic and ϕ0 (in) for UM6502/UM6502E/UM6507 — 4 MHz	+ 3.3	V_{CC}	V
	ϕ_1 and ϕ_2 only for UM6512 — All Speeds	V_{CC} − 0.5	V_{CC} + 0.25	V
V_{IL}	Input Low Voltage			
	Logic, $\phi_{0(in)}$ (UM6502/UM6502E/UM6507)	−0.3	+0.8	
	ϕ_1, ϕ_2 (UM6512)	−0.3	+0.2	V
I_{IL}	Input Loading (V_{in} = 0 V, V_{CC} = 5.25V) RDY, S.O.	−10	−300	µA
I_{in}	Input Leakage Current (V_{in} = 0 to 5.25 V, V_{CC} = 0)			
	Logic (Excl. RDY, S.O.)	–	2.5	µA
	ϕ_1, ϕ_2 (UM6512)	–	100	µA
	$\phi_{0(in)}$ (UM6502/UM6502E/UM6507)	–	10.0	µA
I_{TSI}	Three-State (Off State) Input Current (V_{in} = 0.4 to 2.4 V, V_{CC} = 5.25 V) DB0-DB7	–	± 10	µA
V_{OH}	Output High Voltage (I_{LOAD} = −100 µAdc, V_{CC} = 4.75 V) 1, 2 MHz SYNC, DB0-DB7, AB0-AB15, R/$\overline{W}$	2.4	–	V
V_{OL}	Output Low Voltage (I_{LOAD} = 1.6mAdc, V_{CC} = 4.75V) 1, 2 MHz SYNC, DB0-DB7, AB0-AB15, R/$\overline{W}$	–	0.4	V
P_D	Power Dissipation 1MHz and 2 MHz (V_{CC} = 5.25V)	–	700	mW
C	Capacitance (V_{in} = 0, T_A = 25°C, f = 1 MHz)			
C_{in}	$\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, S.O., DBE	–	10	
	DB0-DB7	–	15	
C_{out}	AB0-AB15, R/$\overline{W}$, SYNC	–	12	pF
$C\phi_{0(in)}$	$\phi_{0(in)}$ (UM6502/UM6502E/UM6507)	–	15	
$C\phi_1$	ϕ_1 (UM6512)	–	50	
$C\phi_2$	ϕ_2 (UM6512)	–	80	

Block Diagram



Notes: 1. Clock generator is not included on UM6512.
2. Addressing capability and control options vary with each product.

Timing Waveforms



Dynamic Operating Characteristics (V_{CC} = 5.0 ± 5%, T_A = 0° to 70°C)

Parameter	Symbol	1 MHz		2 MHz		3 MHz		4 MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
UM6502E										
Cycle Time	T_{CYC}	1.00	40	0.50	40	0.33	40	0.25	40	μs
ϕ_0 (IN) Low Time[2]	$TL\phi_0$	480	–	240	–	160	–	110	–	ns
ϕ_0 (IN) High Time[2]	$TH\phi_0$	460	–	240	–	160	–	115	–	ns
ϕ_0 Neg to ϕ_1 Pos Delay[5]	T_{01+}	10	70	–	50	–	45	–	35	ns
ϕ_0 Neg to ϕ_2 Neg Delay[5]	T_{02-}	5	65	–	45	–	40	–	35	ns
ϕ_0 Pos to ϕ_1 Neg Delay[5]	T_{01-}	5	65	–	45	–	40	–	30	ns
ϕ_0 Pos to ϕ_2 Pos Delay[5]	T_{02+}	15	75	–	45	–	45	–	35	ns
ϕ_0 (IN) Rise and Fall Time[1]	T_{RO}, T_{FO}	0	30	–	20	–	15	–	10	ns
ϕ_1 (OUT), Pulse Width	$T_{PWH\phi_1}$	$T_{L\phi_0}$-20	$T_{L\phi_0}$	$T_{L\phi_0}$-20	$T_{L\phi_0}$	$T_{L\phi_0}$-20	$T_{L\phi_0}$	$T_{L\phi_0}$-20	$T_{L\phi_0}$	ns
ϕ_2 (OUT), Pulse Width	$T_{PWH\phi_2}$	$T_{L\phi_0}$-40	$T_{L\phi_0}$-10	$T_{L\phi_0}$-40	$T_{L\phi_0}$-40	$T_{L\phi_0}$-40	$T_{L\phi_0}$-40	$T_{L\phi_0}$-40	$T_{L\phi_0}$-10	ns
Delay Between ϕ_1 and ϕ_2	T_D	5	–	5	–	5	–	5	–	ns
ϕ_1 and ϕ_2 Rise and Fall Times[1, 3]	T_R, T_F	–	25	–	25	–	15	–	15	ns
UM6502E										
R/W Setup Time	T_{RWS}	–	125	–	100	–	75	–	60	ns
R/W Hold Time	T_{RWH}	30	–	30	–	15	–	15	–	ns
Address Setup Time	T_{ADS}	–	125	–	100	–	75	–	70	ns
Address Hold Time	T_{ADH}	30	–	30	–	15	–	15	–	ns
Read Access Time	T_{ACC}	–	1000-225	–	500-150	–	330-115	–	250-105	ns
Read Data Setup Time	T_{DSU}	100	–	50	–	40	–	35	–	ns
Read Data Hold Time	T_{HR}	10	–	10	–	10	–	10	–	ns
Write Data Setup Time	T_{MDS}	20	175	–	100	–	75	–	60	ns
Write Data Hold Time	T_{HW}	60	–	60	–	30	–	30	–	ns
Sync Setup Time	T_{SYS}	–	125	–	100	–	75	–	60	ns
Sync Hold Time	T_{SYH}	30	–	30	–	15	–	15	–	ns
RDY Setup Time[4]	T_{RS}	200	–	150	–	120	–	120	–	ns
UM6512										
Cycle Time	T_{CYC}	1.00	40	0.50	40	0.33	40	0.25	40	μs
ϕ_1 Pulse Width	$T_{PWH\phi_1}$	430	–	215	–	150	–			ns
ϕ_2 Pulse Width	$T_{PWH\phi_2}$	470	–	235	–	160	–			ns
Delay Between ϕ_2 and ϕ_2	T_D	0	–	0	–	0	–			ns
ϕ_1 and ϕ_2 Rise and Fall Times[1]	T_R, T_F	0	25	0	20	0	15			ns

(Cont.)

Parameter	Symbol	1 MHz		2 MHz		3 MHz		4 MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
UM6502/UM6507										
Cycle Time	T_{CYC}	1.00	40	0.50	40	0.33	40	0.25	40	μs
ϕ_1 (IN) Low Time(2)	$T_{L\phi_0}$	480	–	240	–	160	–	110	–	ns
ϕ_0 (IN) High Time(2)	$T_{H\phi_0}$	460	–	240	–	160	–	115	–	ns
ϕ_0 Neg to ϕ_1 Pos Delay(5)	T_{01+}	10	70	10	70	10	70	10	70	ns
ϕ_0 Neg to ϕ_2 Neg Delay(5)	T_{02-}	5	65	5	65	5	65	5	65	ns
ϕ_0 Pos to ϕ_1 Neg Delay(5)	T_{01-}	5	65	5	65	5	65	5	65	ns
ϕ_0 Pos to ϕ_2 Pos Delay(5)	T_{02+}	15	75	15	75	15	75	15	75	ns
ϕ_0 (IN) Rise and Fall Time(1)	T_{RO}, T_{FO}	0	30	0	20	0	15	0	10	ns
ϕ_1 (OUT), Pulse Width	$T_{PWH\phi_1}$	$T_{L\phi_0}$-20	$T_{L\phi_0}$	$T_{L\phi_0}$-20	$T_{L\phi_0}$	$T_{L\phi_0}$-20	$T_{L\phi_0}$	$T_{L\phi_0}$-20	$T_{L\phi_0}$	ns
ϕ_2 (OUT), Pulse Width	$T_{PWH\phi_2}$	$T_{L\phi_0}$-40	$T_{L\phi_0}$-10	$T_{L\phi_0}$-40	$T_{L\phi_0}$-40	$T_{L\phi_0}$-40	$T_{L\phi_0}$-10	$T_{L\phi_0}$-40	$T_{L\phi_0}$-10	ns
Delay Between ϕ_1 and ϕ_2	T_D	5	–	5	–	5	–	5	–	ns
ϕ_1 and ϕ_2 Rise and Fall Times(1, 3)	T_R, T_F	–	25	–	25	–	15	–	15	ns
UM6502/UM6507/UM6512										
R/W Setup Time	T_{RWS}	–	225	–	140	–	110	–	90	ns
R/W Hold Time	T_{RWH}	30	–	30	–	15	–	10	–	ns
Address Setup Time	T_{ADS}	–	225	–	140	–	110	–	90	ns
Address Hold Time	T_{ADH}	30	–	30	–	15	–	10	–	ns
Read Access Time	T_{ACC}	–	650	–	310	–	170	–	110	ns
Read Data Setup Time	T_{DSU}	100	–	50	–	50	–	50	–	ns
Read Data Hold Time	T_{HR}	10	–	10	–	10	–	10	–	ns
Write Data Setup Time	T_{MDS}	20	175	20	100	20	75	–	70	ns
Write Data Hold Time	T_{HW}	60	150	60	150	30	130	20	–	ns
Sync Setup Time	T_{SYS}	–	350	–	175	–	100	–	90	ns
Sync Hold Time	T_{SYH}	30	–	30	–	15	–	15	–	ns
RDY Setup Time(4)	T_{RS}	200	–	200	–	150	–	120	–	ns

Notes:

1. Measured between 10% and 90% points.
2. Measured at 50% points.
3. Load = 1 TTL load + 30 pF.
4. RDY must never switch states within T_{RS} to end of ϕ_2.
5. Load = 100 pF.

Timing Diagram Note:

Because the clock generation for the UM6502/UM6502E/ UM6507 and UM6512 is different, the two clock timing sections are referenced to the main timing diagram by three reference lines marked REF 'A', REF 'B' and REF 'C'. Reference between the two sets of clock timings is without meaning. Timing parameters referring to these lines and scale variations in the diagrams are of no consequence.

PIN FUNCTIONS

Clocks (ϕ_1, ϕ_2)
The UM6512 requires a two phase non-overlapping clock that runs at the V_{CC} voltage level.

The UM6502/UM6502E/UM6507 clocks are supplied with an internal clock generator. The frequency of these clocks is externally controlled. Clock generator circuits are shown elsewhere in this data sheet.

Address Bus (AB0-AB15)
(See sections on each microprocessor for respective address lines on those devices.)

These outputs are TTL compatible, capable of driving one standard TTL load and 130 pF.

Data Bus (DB0-DB7)
Eight pins are used for the data bus. This is a bi-directional bus, transferring data to and from the device and peripherals. The outputs are three-state buffers, capable of driving one standard TTL load and 130 pF.

Data Bus Enable (DBE)
This TTL compatible input allows external control of the three-state data output buffers and will enable the microprocessor bus driver when in the high state. In normal operation DBE would be driven by the phase two (ϕ_2) clock, thus allowing data output from microprocessor only during ϕ_2. During the read cycle, the data bus drivers are internally disabled, becoming essentially an open circuit. To disable data bus drivers externally, DBE should be held low. This signal is available on the UM6512 only.

Ready (RDY)
This input signal allows the user to halt the microprocessor on all cycles except write cycles. A negative transition to the low state during or coincident with phase one, (ϕ_1) will halt the microprocessor with the output address lines reflecting the current address being fetched. This condition will remain through a subsequent phase two (ϕ_2) in which the Ready signal is low. This feature allows microprocessor interfacing with low speed PROMS as well as fast (max. 2 cycle) Direct Memory Access (DMA). If ready is low during a write cycle, it is ignored until the following read operation. Ready transitions must not be permitted during ϕ_2 time.

Interrupt Request ($\overline{IRQ}$)
This TTL level input requests that an interrupt sequence begin within the microprocessor. The microprocessor will complete the current instruction being executed before recognizing the request. At the time, the interrupt mask bit in the Status Code Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no futher interrupts may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, therefore transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3KΩ external resistor should be used for proper wire-OR operation.

Non-Maskable Interrupt ($\overline{NMI}$)
A negative going transition on this input requests that a non-maskable interrupt sequence be generated within the microprocessor.

$\overline{NMI}$ is an unconditional interrupt. Following completion of the current instruction, the sequence of operations defined for $\overline{IRQ}$ will be performed, regardless of the state interrupt mask flag. The vector addresses loaded into the program counter, low and high, are locations FFFA and FFFB respectively, thereby transferring program control to the memory vector located at these addresses. The instructions loaded at these locations cause the microprocessor to branch to a non-maskable interrupt routine in memory.

$\overline{NMI}$ also requires an external 3KΩ resistor to V_{CC} for proper wire-OR operations.

Inputs $\overline{IRQ}$ and $\overline{NMI}$ are hardware interrupts lines that are sampled during ϕ_2 (phase 2) and will begin the appropriate interrupt routine on the ϕ_1 (phase 1) following the completion of the current instruction.

Set Overflow Flag (S. O.)
A NEGATIVE going edge on this input sets the overflow bit in the Status Code Register. This signal is sampled on the trailing edge of ϕ_1.

SYNC
This output line is provided to identify those cycles in which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during ϕ_1 of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the ϕ_1 clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.

Reset ($\overline{RES}$)
This input is used to reset or start the microprocessor from a power down condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge is detected on the input, the microprocessor will immediately begin the reset sequence.

After a system initialization time of six clock cycles, the mask interrupt flag will be set and the microprocessor will load the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control.

After V_{CC} reaches 4.75 volts in a power up routine, reset must be held low for at least two clock cycles. At this time the R/$\overline{W}$ and SYNC signal will become valid.

When the reset signal goes high following these two clock cycles, the microprocessor will proceed with the normal reset procedure detailed above.

Read/Write (R/$\overline{W}$)
This output signal is used to control the direction of data transfers between the processor and other circuits on the data bus. A high level on R/$\overline{W}$ signifies data into the processor; a low is for the data transfer out of the processor.

PROGRAMMING CHARACTERISTICS

INSTRUCTION SET – ALPHABETIC SEQUENCE

ADC	Add Memory to Accumulator with Carry
AND	"AND" Memory with Accumulator
ASL	Shift left One Bit (Memory or Accumulator)
BCC	Branch on Carry Clear
BCS	Branch on Carry Set
BEQ	Branch on Result Zero
BIT	Test Bits in Memory with Accumulator
BMI	Branch on Result Minus
BNE	Branch on Result not Zero
BPL	Branch on Result Plus
BNK	Force Break
BVC	Branch on Overflow Clear
BVS	Branch on Overflow Set
CLC	Clear Carry Flag
CLD	Clear Decimal Mode
CLI	Clear Interrupt Disable Bit
CLV	Clear Overflow Flag
CMP	Compare Memory and Accumulator
CPX	Compare Memory and Index X
CPY	Compare Memory and Index Y
DEC	Decrement Memory by One
DEX	Decrement Index X by One
DEY	Decrement Index Y by One
EOR	"Exclusive-or" Memory with Accumulator
INC	Increment Memory by One
INX	Increment Index X by One
INY	Increment Index Y by One
JMP	Jump to New Location
JSR	Jump to New Location Saving Return Address
LDA	Load Accumulator with Memory
LDX	Load Index X with Memory
LDY	Load Index Y with Memory
LSR	Shift One Bit Right (Memory or Accumulator)
NOP	No Operation
ORA	"OR" Memory with Accumulator
PHA	Push Accumulator on Stack
PHP	Push Processor Status on Stack
PLA	Pull Accumulator from Stack
PLP	Pull Processor Status from Stack
ROL	Rotate One Bit Left (Memory or Accumulator)
ROR	Rotate One Bit Right (Memory or Accumulator)
RTI	Return from Interrupt
RTS	Return from Subroutine
SBC	Subtract Memory from Accumulator with Borrow
SEC	Set Carry Flag
SED	Set Decimal Mode
SEI	Set Interrupt Disable Status
STA	Store Accumulator in Memory
STX	Store Index X in Memory
STY	Store Index Y in Memory
TAX	Transfer Accumulator to Index X
TAY	Transfer Accumulator to Index Y
TSX	Transfer Stack Pointer to Index X
TXA	Transfer Index X to Accumulator
TXS	Transfer Index X to Stack Pointer
TYA	Transfer Index Y to Accumulator

ADDRESSING MODES

Accumulator Addressing
This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

Immediate Addressing
In immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

Absolute Addressing
In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 65K bytes of addressable memory.

Zero Page Addressing
The zero page instructions allow for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. careful use of the zero page can result in significant increase in code efficiency.

Indexed Zero Page Addressing – (X, Y indexing)
This form of addressing is used in conjunction with the index register and is referred to as "Zero Page, "X" or "Zero Page, Y." The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally due to the "Zero Page" addressing nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.

Indexed Absolute Addressing – (X, Y indexing)
This form of addressing is used in conjunction with X and Y index registers and is referred to as "Absolute,

X," and "Absolute, Y." The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

Implied Addressing

In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

Relative Addressing

Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is-128 to + 127 bytes from the next instruction.

Indexed Indirect Addressing

In indexed indirect addressing (referred to as [Indirect, X]), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose content is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

Indirect Indexed Addressing

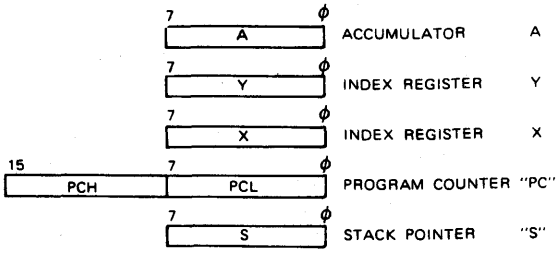
In indirect indexed addressing (referred to as [Indirect], Y), the second byte of the instruction points to a memory location in page zero. The content of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

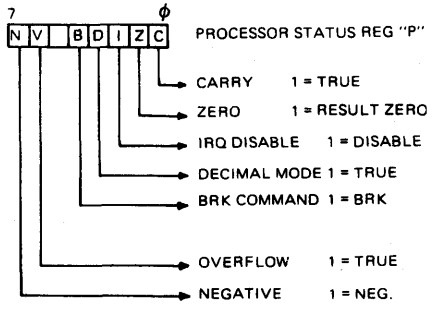
Absolute Indirect

The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The content of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter.

PROGRAMMING CHARACTERISTICS

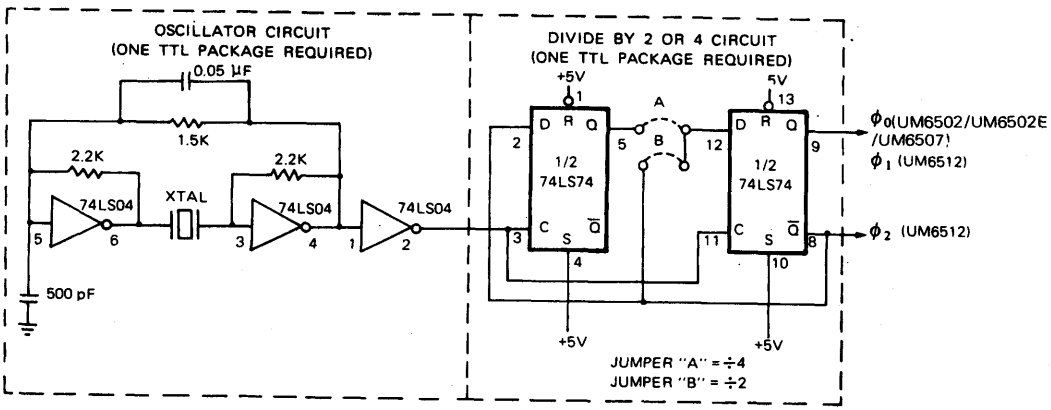
PROGRAMMING MODEL



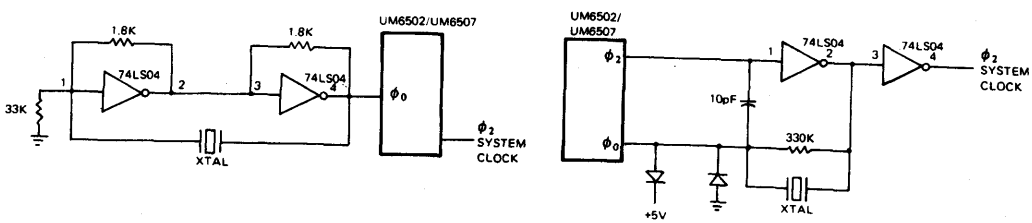


Clock Generation Circuits*

*Crystals used are CTS Knight MP Series or equivalents. (Series Mode)



Crystal Frequency	Output Frequency	
	÷2	÷4
3.579545 MHz	1.7897 MHz	0.894886 MHz
4.194304 MHz	2.097152 MHz	1.048576 MHz



Crystal Application Circuit

Ordering Information

1 MHz	2 MHz	3 MHz	4 MHz
UM6502	UM6502A	UM6502B	UM6502C
UM6502E	UM6502AE	UM6502BE	UM6502CE
UM6507	–	–	–
UM6512	UM6512A	UM6512B	UM6512C

Part Number	Clocks	Pins	IRQ	NMI	RYD	Addressing
UM6502	On-Chip	40	√	√	√	64K
UM6502E	On-Chip	40	√	√	√	64K
UM6507	On-Chip	28	√	√	√	8K
UM6512	External	40	√	√	√	64K

Instruction Set

INSTRUCTIONS				IMME-DIATE			ABSO-LUTE			ZERO-PAGE			ACCUM			IMPLIED			(IND. X)			(IND. Y)		
MNEMONIC			OPERATION	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#
A	D	C	A + M + C → A (4) (1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2
A	N	D	A ∧ M → A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2
A	S	L	C ← [7 0] ←0				0E	6	3	06	5	2	0A	2	1									
B	C	C	BRANCH ON C = 0 (2)																					
B	C	S	BRANCH ON C = 1 (2)																					
B	E	Q	BRANCH ON Z = 1 (2)																					
B	I	T	A ∧ M				2C	4	3	24	3	2												
B	M	I	BRANCH ON N = 1 (2)																					
B	N	E	BRANCH ON Z = 0 (2)																					
B	P	L	BRANCH ON N = 0 (2)																					
B	R	K	BREAK													00	7	1						
B	V	C	BRANCH ON V = 0 (2)																					
B	V	S	BRANCH ON V = 1 (2)																					
C	L	C	0 → C													18	2	1						
C	L	D	0 → D													D8	2	1						
C	L	I	0 → 1													58	2	1						
C	L	V	0 → V													B8	2	1						
C	M	P	A − M	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2
C	P	X	X − M	E0	2	2	EC	4	3	E4	3	2												
C	P	Y	Y − M	C0	2	2	CC	4	3	C4	3	2												
D	E	C	M − 1 → M				CE	6	3	C6	5	2												
D	E	X	X − 1 → X													CA	2	1						
D	E	Y	Y − 1 → Y													88	2	1						
E	O	R	A V M → A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2
I	N	C	M + 1 → M				EE	6	3	E6	5	2												
I	N	X	X + 1 → X													E8	2	1						
I	N	Y	Y + 1 → Y													C8	2	1						
J	M	P	JUMP TO NEW LOC				4C	3	3															
J	S	R	JUMP SUB				20	6	3															
L	D	A	M → A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2
L	D	X	M → X (1)	A2	2	2	AE	4	3	A6	3	2												
L	D	Y	M → Y (1)	A0	2	2	AC	4	3	A4	3	2												
L	S	R	0 → [7 0] → C				4E	6	3	46	5	2	4A	2	1									
N	O	P	NO OPERATION													EA	2	1						
O	R	A	A V M → A	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2
P	H	A	A → MS S − 1 → S													48	3	1						
P	H	P	P → MS S − 1 → S													08	3	2						
P	L	A	S + 1 → S MS → A													68	4	1						
P	L	P	S + 1 → S MS → P													28	4	1						
R	O	L	← [7 0] ← [C] ←				2E	6	3	26	5	2	2A	2	1									
R	O	R	→ [C] → [0 7] →				6E	6	3	66	5	2	6A	2	1									
R	T	I	RTRN INT													40	6	1						
R	T	S	RTRN SUB													60	6	1						
S	B	C	A − M − C̄ → A (1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2
S	E	C	1 → C													38	2	1						
S	E	D	1 → D													F8	2	1						
S	E	I	1 → 1													78	2	1						
S	T	A	A → M				8D	4	3	85	3	2							81	6	2	91	6	2
S	T	X	X → M				8E	4	3	86	3	2												
S	T	Y	Y → M				8C	4	3	84	3	2												
T	A	X	A → X													AA	2	1						
T	A	Y	A → Y													A8	2	1						
T	S	X	S → X													BA	2	1						
T	X	A	X → A													8A	2	1						
T	X	S	X → S													9A	2	1						
T	Y	A	Y → A													98	2	1						

Notes: (1) ADD 1 TO N IF PAGE BOUNDARY IS CROSSED
(2) ADD 1 TO N IF BRANCH OCCURS TO SAME PAGE
ADD 2 TO N IF BRANCH OCCURS TO DIFFERENT PAGE
(3) CARRY NOT = BORROW
(4) IF IN DECIMAL MODE Z FLAG IS INVALID
ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT

Z PAGE. X			ABS. X			ABS. Y			RELA-TIVE			INDI-RECT			Z PAGE. Y			PROCESSOR STATUS CODES								
OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	7	6	5	4	3	2	1	0	MNEMONIC
																		N	V	.	B	D	I	Z	C	
75	4	2	7D	4	3	79	4	3										N	V	.	.	.	.	Z	C	ADC
35	4	2	3D	4	3	39	4	3										N	.	.	.	.	.	Z	.	AND
16	6	2	1E	7	3													N	.	.	.	.	.	Z	C	ASL
									90	7	2							.	.	.	.	.	.	.	.	BCC
									B0	2	2							.	.	.	.	.	.	.	.	BCS
									F0	2	2							M_7	M_6	.	.	.	.	Z	.	BEQ
									30	2	2							.	.	.	.	.	.	.	.	BMI
									D0	2	2							.	.	.	.	.	.	.	.	BNE
									10	2	2							.	.	.	.	.	.	.	.	BPL
									50	2	2							.	.	.	.	1	.	1	.	.	BRK
									70	2	2							.	.	.	.	.	.	.	.	BVC
																		.	.	.	.	.	.	.	.	BVS
																		.	.	.	.	.	.	.	0	CLC
																		.	.	.	.	0	.	.	.	CLD
D5	4	2	DD	4	3	D9	4	3										.	0	.	.	.	.	0	.	.	CLI
																		.	.	.	.	.	.	.	.	CLV
																		N	.	.	.	.	.	Z	C	CMP
																		N	.	.	.	.	.	Z	C	CPX
																		N	.	.	.	.	.	Z	C	CPY
D6	6	2	DE	7	3													N	.	.	.	.	.	Z	.	DEC
																		N	.	.	.	.	.	Z	.	DEX
55	4	2	5D	4	3	59	4	3										N	.	.	.	.	.	Z	.	DEY
F6	6	2	FE	7	3													N	.	.	.	.	.	Z	.	EOR
																		N	.	.	.	.	.	Z	.	INC
																		N	.	.	.	.	.	Z	.	INX
												6C	5	3				N	.	.	.	.	.	Z	.	INY
B5	4	2	BD	4	3	B9	4	3										.	.	.	.	.	.	.	.	JMP
																		N	.	.	.	.	.	Z	.	JSR
						BE	4	3							B6	4	2	N	.	.	.	.	.	Z	.	LDA
B4	4	2	BC	4	3													N	.	.	.	.	.	Z	.	LDX
56	6	2	5E	7	3													0	.	.	.	.	.	Z	C	LDY
																		.	.	.	.	.	.	.	.	LSR
15	4	2	1D	4	3	19	4	3										N	.	.	.	.	.	Z	.	NOP
																		.	.	.	.	.	.	.	.	ORA
																		.	.	.	.	.	.	.	.	PHA
																		.	.	.	.	.	.	.	.	PHP
																		N	.	.	.	.	.	Z	.	PLA
36	6	2	3E	7	3															(RESTORED)						PLP
																		N	.	.	.	.	.	Z	C	ROL
76	6	2	7E	7	3													N	.	.	.	.	.	Z	C	ROR
																				(RESTORED)						RTI
F5	4	2	FD	4	3	F9	4	3										N	V	.	.	.	.	Z	(3)	RTS
																		.	.	.	.	.	.	.	1	SBC
																		.	.	.	.	1	.	.	.	SEC
																		.	.	.	.	.	.	1	.	SED
95	4	2	9D	5	3	99	5	3										.	.	.	.	.	.	.	.	SEI
																		.	.	.	.	.	1	.	.	STA
94	4	2													96	4	2	.	.	.	.	.	.	.	.	STX
																		.	.	.	.	.	.	.	.	STY
																		N	.	.	.	.	.	Z	.	TAX
																		N	.	.	.	.	.	Z	.	TAY
																		N	.	.	.	.	.	Z	.	TSX
																		.	.	.	.	.	.	.	.	TXA
																		.	.	.	.	.	.	Z	.	TXS
																		N	.	.	.	.	.	Z	.	TYA

X INDEX X
Y INDEX Y
A ACCUMULATOR
M MEMORY PER EFFECTIVE ADDRESS
Ms MEMORY PER STACK POINTER

\+ ADD
− SUBTRACT
∧ AND
V OR
∀ EXCLUSIVE OR

M_7 MEMORY BIT 7
M_6 MEMORY BIT 6
n NO. CYCLES
NO. BYTES

PC Mainboard I

Part No.	Description	Page
UM74HCT590	8 bit Binary Counter with Output Registers	2-3
UM74HCT612	Memory Mapper	2-7
UM74HC646	Octal Bus Transceiver and Register	2-13
UM82C088	PC/XT Integration Chip	2-19
UM82C284-10/-12	Clock Generator and Ready Interface	2-41
UM82C288-10/-12	Bus Controller	2-48
UM82C54/-2	CMOS Programmable Interval Timer	2-63
UM82C55A	CMOS Programmable Peripheral Interface	2-79
UM82C59A-2	CMOS Programmable Interrupt Controller	2-98
UM82C84AE	CMOS Clock Generator and Driver	2-115
UM82152	Cache Controller	2-122
UM8237AE/-4/-5	Programmable DMA Controller (DMAC)	2-126
UM8253/-5	Programmable Interval Timer	2-142
UM8259A-2	Programmable Interrupt Controller	2-153

UMC

UM74HCT590

8-bit Binary Counter with Output Registers

Features

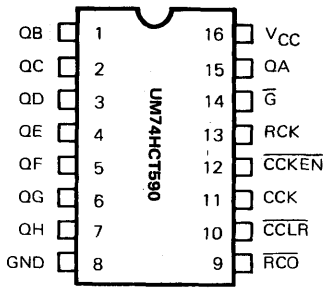
- 8-bit binary counter with parallel register output.
- 3-state register output.
- Direct clear to counter.
- High speed counter with guaranteed frequency: DC to 20 MHz.
- High driving capability (I_{OL} = 24 mA, V_{OL} = 0.5V) for direct interface with TTL, NMOS and CMOS devices.
- Can drive up to 20 TTL loads.

General Description

This is an 8-bit binary counter that feeds an 8-bit storage register. The register has parallel Tri-state outputs QA ~ QH enabled by $\overline{G}$ = 0. Two separate clocks, CCK and RCK, are provided for both the binary counter and storage register. The binary counter features a direct clear input $\overline{CCLR}$ and a count enable input $\overline{CCKEN}$. For cascading, a ripple carry output $\overline{RCO}$ is provided. Expansion is easily accomplished for two stages by connecting $\overline{RCO}$ of the first stage to $\overline{CCKEN}$ of the second stage. Cascading for larger count chains can be accomplished by connecting $\overline{RCO}$ of each stage to CCK of the following stage.

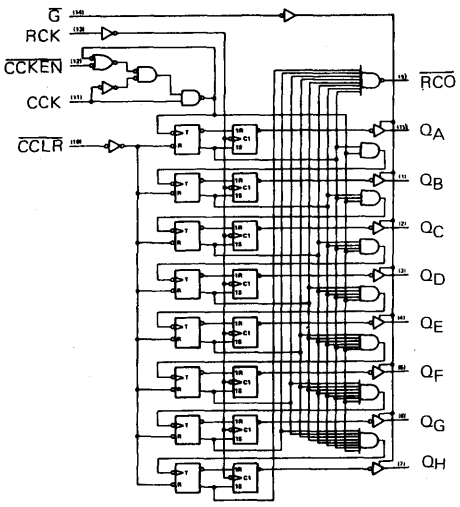
Both the counter and register clocks are positive-edge. When connecting both clocks together, the counter state will always be one count ahead of the register.

Pin Configuration



QA~QH	Register Output.
RCK	Register Clock, Positive Trigger.
CCK	Counter Clock, Positive Trigger.
$\overline{RCO}$	Ripple Carry Output.
$\overline{G}$	Output Enable, $\overline{G}$ = 1 ⇒ Output = High-Z.
$\overline{CCKEN}$	Counter Clock Enable, Active Low.
$\overline{CCLR}$	Counter Clear, Active Low.

Block Diagram



Absolute Maximum Ratings*

Supply Voltage, V_{CC} . . . . . –0.5 to 7V

Input Voltage V_I . . . . . –0.5V to +7V

Operating Free-Air Temperature Range . . . –40°C to 85°C

Storage Temperature Range . . . . . –55°C to 125°C

Maximum Power Dissipation . . . . . 0.55 mW

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 5V, T_A = 0°C to 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{CC}	Power Supply	4.5	5	5.5	V	
V_{IH}	Input High-Level Voltage	2.0	–	–	V	
V_{IL}	Input Low-Level Voltage	–	–	0.8	V	
I_{OH}	High-Level Output Current On QA ~ QH	–	–	–4	mA	V_{OH} = 3.0V
I_{OL}	Low-Level Output Current On QA ~ QH	–	–	24	mA	V_{OL} = 0.5V
I_{OHR}	High-Level Output Current On $\overline{RCO}$	–	–	0.4	mA	$V_{\overline{RCO}}$ = 3.4V
I_{OLR}	Low-Level Output Current On $\overline{RCO}$	–	–	8	mA	$V_{\overline{RCO}}$ = 0.5V
V_{OH}	High-Level Output Voltage	3.0	3.8	–	V	$\lvert I_{OH} \rvert$ or $\lvert I_{OHR} \rvert$ = Max.
V_{OL}	Low-Level Output Voltage	–	0.4	0.5	V	I_{OL} or I_{OLR} = Max.
I_{IN}	Input Current	–1.0	–	+1.0	μA	V_{IN} = 5V ~ 0V
I_{OZ}	OFF-State Output Current	–8	–	+8	μA	V_O = 5V ~ 0V.
I_{CC}	Operating Supply Current	–	–	100	μA	

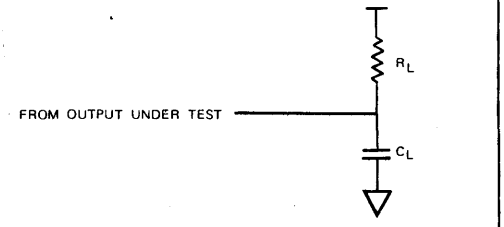
Timing Requirement and Switching Characteristics:
(V_{DD} = 5V, T_A = 0°C to 85°C)

Parameter		Min.	Typ.	Max.	Unit	Conditions
Clock Frequency CCK or CCR: $F_{max.}$		20	35	–	MHz	
Pulse Width of CCK or RCK: T_W		20	–	–	ns	Recommended Value
Pulse Width of $\overline{CCLR}$: T_W		20	–	–	ns	Recommended Value
Count enable time: $\overline{CCKEN}$ Low before CCK ↑		20	–	–	ns	Recommended Value
Clear inactive set-up time: T_{SU} $\overline{CCLR}$ Low go High before CCK ↑		20	–	–	ns	Recommended Value
Time Delay from CCK ↑ to $\overline{RCO}$ ↑: T_{PLH}		–	15	25	ns	C_L = 15 pf. R_L = 2KΩ
Time Delay from CCK ↑ to $\overline{RCO}$ ↓: T_{PHL}		–	20	25	ns	
Time Delay from $\overline{CCLR}$ ↓ to $\overline{RCO}$ ↑: T_{PLH}		–	20	25	ns	
Time Delay from RCK ↑ to Q ↑: T_{PLH}		–	15	25	ns	C_L = 45 PF R_L = 667Ω
Time Delay from RCK ↑ to Q ↓: T_{PHL}		–	20	25	ns	
Time Delay when $\overline{G}$ ↓	Q Floating to Q Low: T_{PZL}	–	15	20	ns	
	Q Floating to Q High: T_{PZH}	–	–	20	ns	
Time Delay when $\overline{G}$ ↑	Q High to Q Floating: T_{PHZ}	–	15	20	ns	C_L = 5 PF R_L = 667Ω
	Q Low to Q Floating: T_{PLZ}	–	–	15	ns	

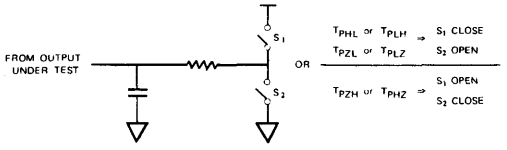
Note: The Parameter Symbol, Voltage Waveform and Measurement Information is Shown on the Next Page.

Parameter Measurement: (Conditions under V_{DD} = 5V, T_A = 25°C)

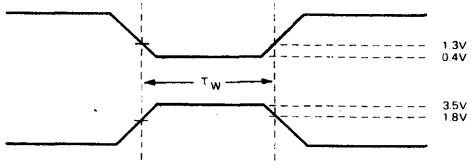
Totem Pole Outputs:



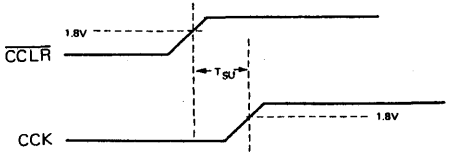
Tri-State Outputs: (QA ~ QH)



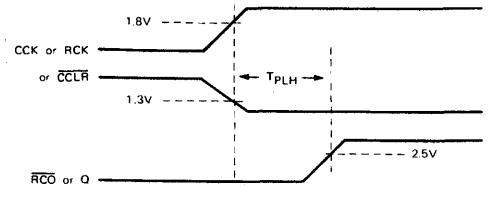
T_W:



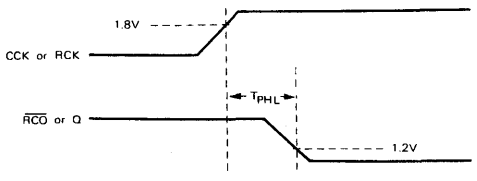
T_{SU}:



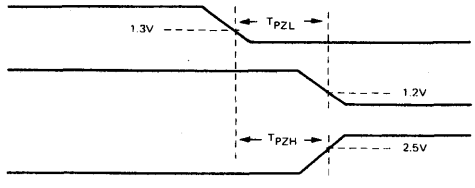
T_{PLH}:



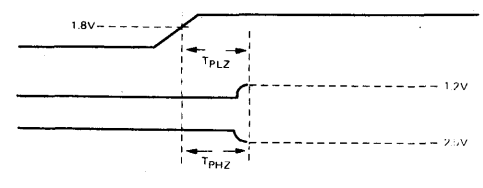
T_{PHL}:



T_{PZL}, T_{PZH}: $\overline{G}$



T_{PHZ}, T_{PLZ}: $\overline{G}$



UMC

UM74HCT612

Memory Mapper

Features

- Fully compatible with TTL, NMOS and CMOS devices.
- Expands 4 address lines to 12 address lines.
- Designed for paged memory mapping.
- High-current 3-state outputs.

General Description

The UM74HCT612 essentially contains a 4-line to 16-line decoder and a 16-word by 12-bit RAM. It is designed to expand a microprocessor's memory address capability by 8 bits (from 4 to 12). That is, four bits of the memory address bus can be used to select one of 16 map registers that contain 12 bits each. These 12 bits are presented to the system memory address bus along with the unused memory address bit from the CPU. By periodically re-loading the mapper registers from the data bus, one can access any of the 16 pages of memory.

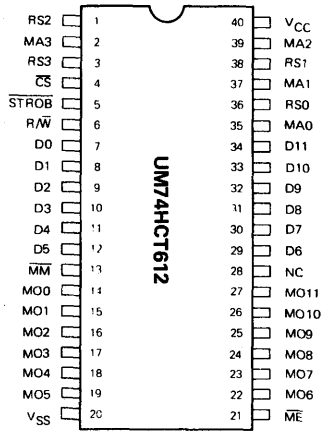
There are four modes of operation (read, write, map, and pass). When $\overline{CS}$ (Chip Select) is active low, through D0 ~ D7, data may be read from or written into the map register selected by the register select inputs (RS0 ~ RS3) under the control of R/$\overline{W}$.

When $\overline{CS}$ is high and $\overline{MM}$ (Map Mode Control) is active low, the map operation will output the contents of map register selected by the map address input (MA0 ~ MA3).

When $\overline{CS}$ and $\overline{MM}$ are both high (pass mode), the address bit on MA0 ~ MA3 appears at MO8 ~ MO11, respectively, with the other bits forcing low level. MO0 ~ MO7 are low.

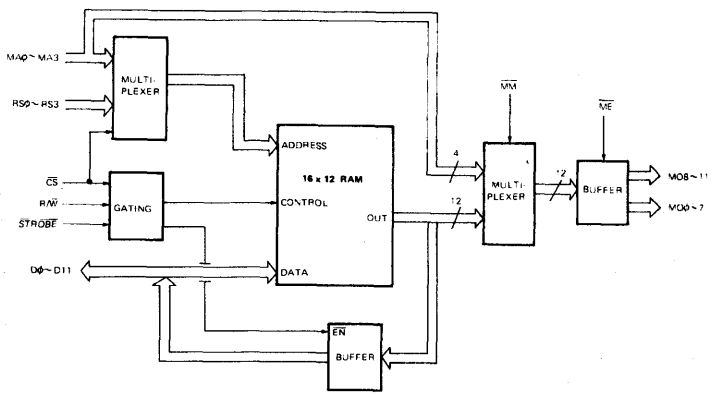
All outputs are tri-state outputs with high current capability. The $\overline{STROBE}$ input is used to enter data into selected map register during I/O operation. Map outputs are enabled by the $\overline{ME}$ input.

Pin Configuration



*NC: Not connected.

Block Diagram



Absolute Maximum Ratings*

D.C. Supply Voltage, V_{DD} . . . . . −0.5V to 7V (respect to V_{SS})
Input Voltage V_I . . . . . −0.5V to 7V
Operating Temperature . . . . . 0°C to 70°C
Storage Temperature . . . . . −65°C to 150°C
Maximum Power Dissipation 0.1W

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(V_{DD} = 5V ± 10%, T_A = 0°C ~ 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{DD}	Power Supply	4.5	5	5.5	V	Recommended
V_{IH}	Input High-Level Voltage	2.0	–	–	V	Recommended
V_{IL}	Input Low-Level Voltage	–	–	0.8	V	Recommended
V_{OHD}	Output High-Level Voltage on D0 ~ D11	4.4	4.9	–	V	I_{OH} = −20 μA
		3.8	4.0	–	V	I_{OH} = −6.0 mA
V_{OHM}	Output High-Level Voltage on MO0 ~ MO11	4.4	4.9	–	V	I_{OH} = −20 μA
		3.8	4.3	–	V	I_{OH} = −8.0 mA
V_{OLD}	Output Low-Level Voltage on D0 ~ D11	–	0.001	0.1	V	I_{OL} = 20 μA
		–	0.3	0.4	V	I_{OL} = 12 mA
V_{OLM}	Output Low-Level Voltage on MO0 ~ MO11	–	0.001	0.1	V	I_{OL} = 20 μA
		–	0.4	0.5	V	I_{OL} = 20 mA
I_{IN}	Input Current	−1.0	–	1.0	μA	V_{IN} = 5V ~ 0V
I_{OZ}	OFF-State Output Current	−5	–	5	μA	V_o = 3V ~ 0V
I_{CC}	Steady Current	–	–	10	μA	V_{IN} = V_{DD} or 0V, No Load.

Timing Requirement and Switching Characteristics: (V_{DD} = 5V ± 10%, T_A = 0°C to 70°C)

Parameter	Min.	Typ.	Max.	Unit	Conditions
Pulse Width of $\overline{STROB}$: Tsbw	75	–	–	ns	Recommended Value
$\overline{CS}$ Setup Time: Tcssu ($\overline{CS}$ low to $\overline{STROB}$ low)	20	–	–	ns	Recommended Value
R/$\overline{W}$ Setup Time: Trwsu (R/W low to $\overline{STROB}$ low)	20	–	–	ns	Recommended Value
RS Setup Time: Trssu (RS valid to $\overline{STROB}$ low)	20	–	–	ns	Recommended Value
DATA Setup Time: Tdasu (D0–D11 valid to $\overline{STROB}$ high)	75	–	–	ns	Recommended Value
CS Hold Time: Tcshd ($\overline{STROB}$ high to $\overline{CS}$ high)	20	–	–	ns	Recommended Value
R/$\overline{W}$ Hold Time: Trwhd ($\overline{STROB}$ high to R/$\overline{W}$ high)	20	–	–	ns	Recommended Value
RS Hold Time: Trshd ($\overline{STROB}$ high to RS invalid)	20	–	–	ns	Recommended Value
DATA Hold Time: Tdahd ($\overline{STROB}$ high to D0 – D11 invalid)	20	–	–	ns	Recommended Value
RS to D0–D11: TRSDV (TpHL or TpLH)	–	39	75	ns	Figure 1 with RL = 1K, CL = 50P_f Timing Diagram see Figure 6.
$\overline{CS}$ ↓ to D0–D11: TCLDV (TpZL or TpZH)	–	26	50	ns	
$\overline{CS}$ ↑ to D0–D11, disable: TCHDZ (TpHZ or TpLZ)	–	38	65	ns	
R/$\overline{W}$ ↑ to D0–D11: TWHDV (TpZL or TpZH)	–	20	35	ns	
R/$\overline{W}$ ↓ to D0–D11, disable: TWLDZ (TpHZ or TpLZ)	–	30	50	ns	
$\overline{CS}$ ↑ to MO0–MO11. TCHQ (TpHL or TpLH)	–	48	85	ns	Figure 1 with RL = 1K; CL = 50P_f Timing Diagram see Figure 7.
$\overline{MM}$ ↓ to MO0–MO11: TMLQ (TpHL or TpLH)	–	20	40	ns	
$\overline{MM}$ ↑ to MO0–MO11: TMHQ (TpHL or TpLH)	–	22	40	ns	
MA to MO0–MO11, $\overline{MM}$ = low: TAVQ1 (TpHL or TpLH)	–	39	70	ns	
MA to MO8–MO11, $\overline{MM}$ = high: TAVQ2 (TpHL or TpLH)	–	13	30	ns	
$\overline{ME}$ ↓ to MO0–MO11: TELQ (TpZL or TpZH)	–	17	30	ns	
$\overline{ME}$ ↑ to MO0–ME11, disable: TEHQZ (TpHZ or TpLZ)	–	14	25	ns	

Note: *See Figures 2, 3, 4, and 5, for definitions of TpLH, TpHL, TpHZ, TpLZ, TpZH, TpZL.*

Pin Description

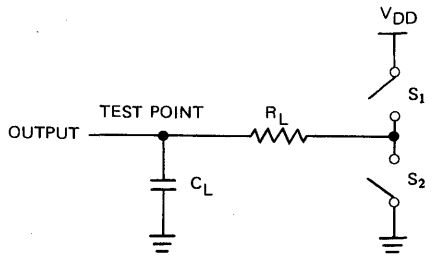
Symbol	Description
D0–D11	I/O connection to data and control bus. Used for reading from or writing into the map register.
RS0–RS3	Register select inputs for I/O operation.
R/$\overline{W}$	Read or write control pin used in I/O operation. When low, data bus is used to write into register. When high, data bus is used to read from register.
$\overline{STROB}$	Strobe input. Used to enter data into register.
$\overline{CS}$	Chip select input. When low, the Read and Write Modes are active.
MA0–MA3	Inputs to select one of 16 registers, when in map mode.
MO0–MO11	Map outputs. Present the map register contents to the system memory address bus in the map mode. When in pass mode, these outputs provide the map address data on MO8 – MO11 and low level on MO0–MO11.
$\overline{MM}$	Map mode input. When low, the map mode is active; when high, it is in pass mode.
$\overline{ME}$	Map output enable pin. When low, outputs MO0–MO11 are active. When high, these are high impedance.

Function Table

$\overline{CS}$	$\overline{MM}$	R/$\overline{W}$	$\overline{STROBE}$	Operation
0	X	0	0	Write Mode, D0 ~ D7 ⇒ Selected Register.
0	X	1	X	Read Mode, Selected Register ⇒ D0 ~ D7.
1	0	X	X	Map Mode, Register Contents ⇒ MO0 ~ MO11 (If $\overline{ME}$ = 0).
1	1	X	X	Pass Mode. MA0 ~ MA3 ⇒ MD8 ~ MD11 and MD0 ~ MD7 are all low (If $\overline{ME}$ = 0).

Parameter Measurements

3-State Output



Parameter	S_1	S_2
TpHL	Open	Open
TpLH		
TpZH	Open	Closed
TpHZ		
TpZL	Closed	Open
TpLE		

Figure 1

Set-Up and Rise, Fall Times

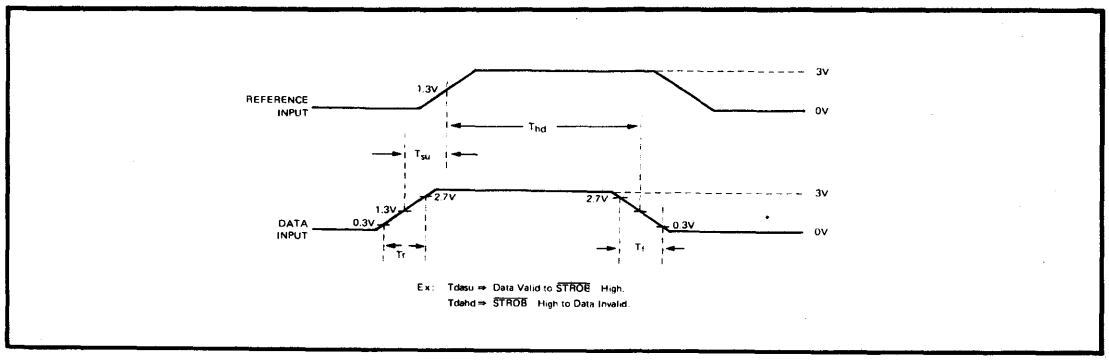


Figure 2

Pulse Duration

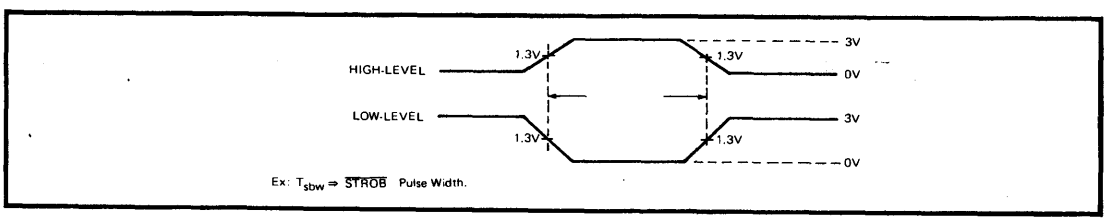


Figure 3

Delay Times

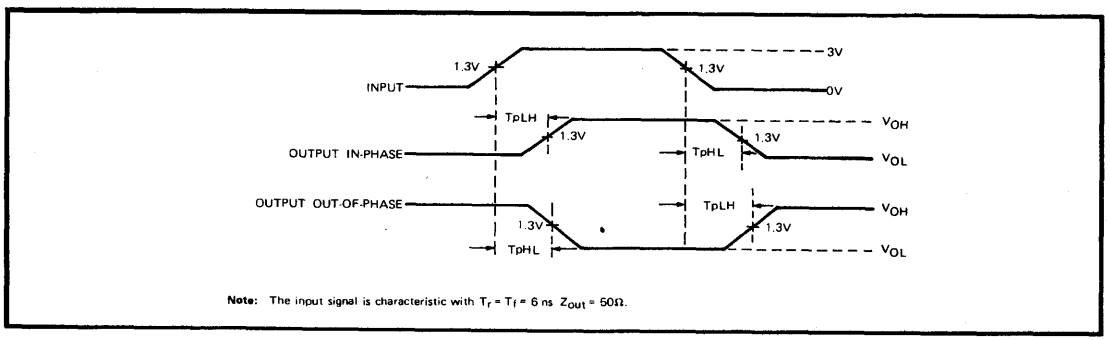


Figure 4

Enable or Disable

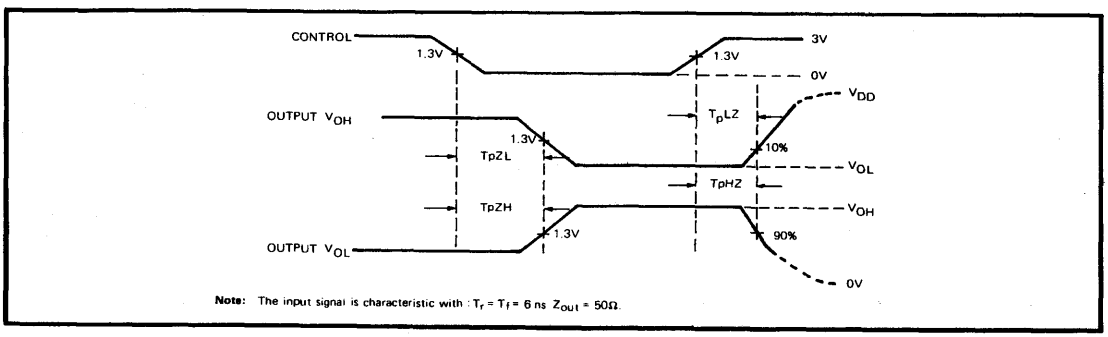


Figure 5

Timing Waveforms

Read and Write Mode

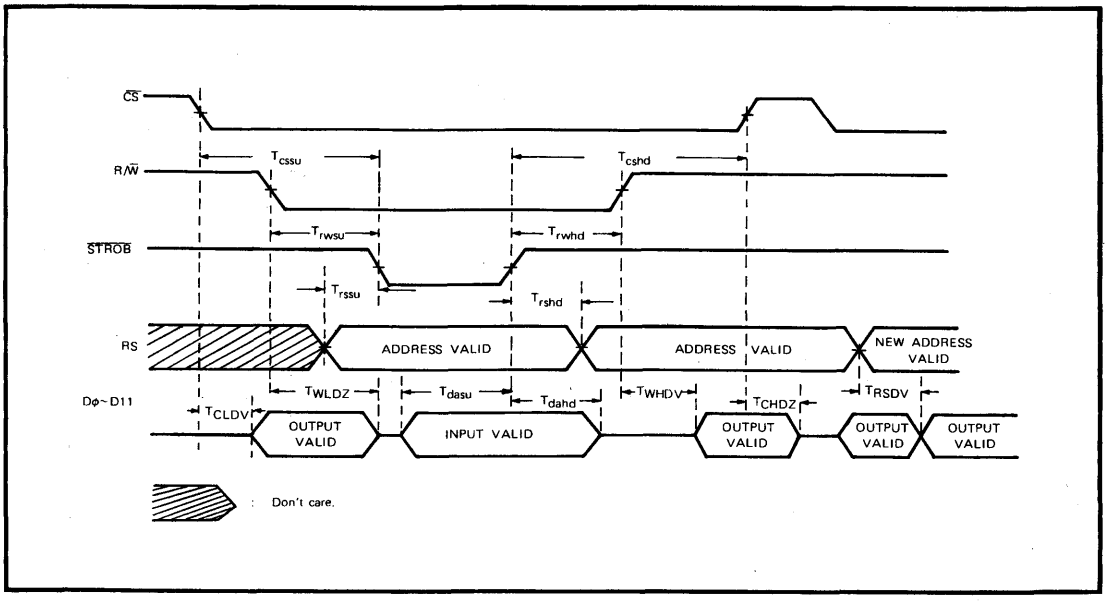


Figure 6

Map and Pass Mode

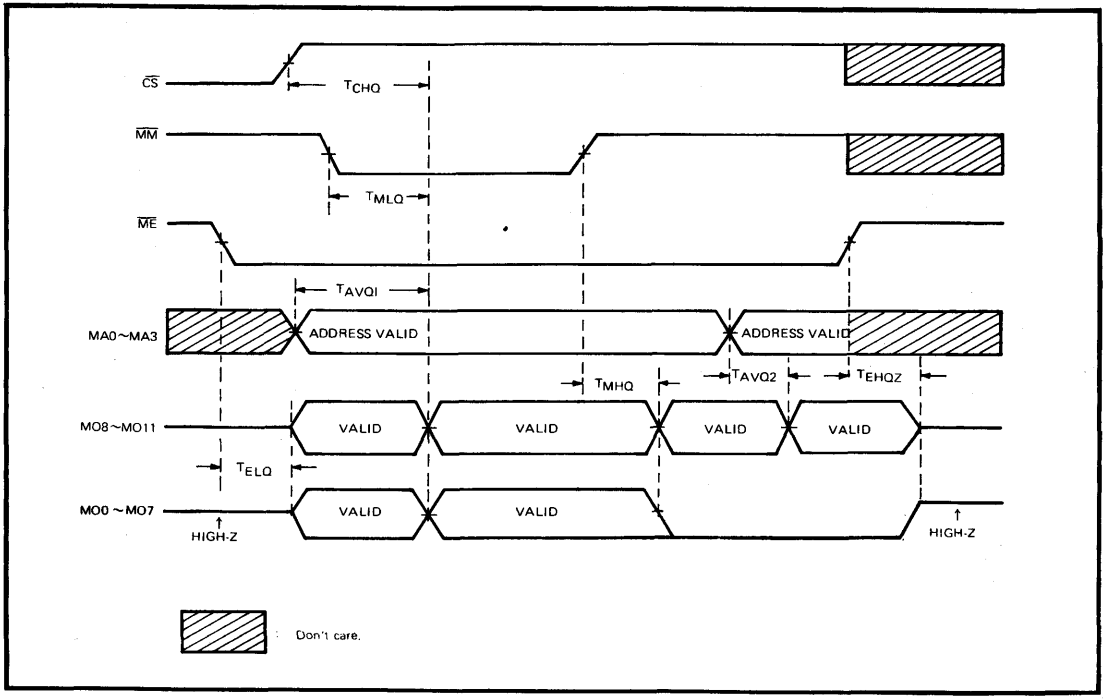


Figure 7

UMC

UM74HCT646

Octal Bus Transceiver and Register

Features

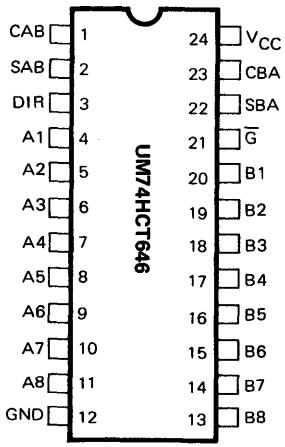
- 8 bi-directional data bus
- Transmits real-time data or stored data in either direction
- 3-state outputs with driving capability for direct bus interface
- Low power consumption with function, pin-out, speed and drive compatibility with 74LS logic family and interfaces directly with TTL, NMOS and CMOS devices
- Available in 24 lead DIP

General Description

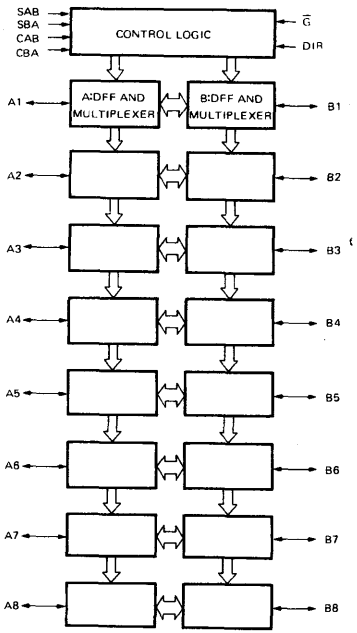
The UM74HCT646, fabricated using the UMC silicon gate CMOS process, is a bi-directional bus transceiver with D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers.

Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CAB or CBA). The examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Supply Voltage, V_{CC} 7V

Operating Free-Air Temperature

Range . . . . . 0°C to 70°C

Storage Temperature Range . . . . . −55°C to 125°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{CC} = 5V, T_A = 25°C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V	
V_{IH}	High-Level Input Voltage	2.0	–	–	V	
V_{IL}	Low-Level Input Voltage	–	0.5	0.8	V	
I_I	Input Current (all except I/O pins)	–	0.01	0.1	μA	V_I = 0V ~ 5V
V_{OH}	High-Level Output Voltage	4.8	–	–	V	$\|I_{OH}\|$ = 20 μA
		3.0	–	–	V	$\|I_{OH}\|$ = Max
V_{OL}	Low-Level Output Voltage	–	–	0.1	V	I_{OL} = 20 μA
		–	–	0.5	V	I_{OL} = 24 mA
I_{OZ}	3-state Leakage Current When Output is Disabled	–	–	0.5	μA	V_O = 0 ~ 5V
I_{CC}	Quiescent Supply Current	–	–	8	μA	V_{IN} = 0U or V_{CC} with No Load

AC Characteristics (Input t_r, $t_f \leq$ 2 ns)

Symbol	Parameter	Conditions†		T_A = 25°C, V_{CC} = 5.0V			Unit
				Min.	Typ.	Max.	
f_{max}	Maximum Clock Frequency	C_L = 50 pF		30	45	–	MHz
t_{PLH}	Maximum Propagation Delay, A or B Input to B or A Output	C_L = 50 pF		–	12	25	ns
t_{PHL}		C_L = 50 pF		–	12	25	
t_{PLH}	Maximum Propagation Delay, CBA or CAB Input to A or B Output	C_L = 50 pF		–	16	35	ns
t_{PHL}		C_L = 50 pF		–	16	35	
t_{PLH}	Maximum Propagation Delay, SBA or SAB Input to A or B Output (with A or B High)	C_L = 50 pF		–	16	35	ns
t_{PHL}		C_L = 50 pF		–	16	35	
t_{PLH}	Maximum Propagation Delay, SBA or SAB Input to A or B Output (with A or B High)	C_L = 50 pF		–	16	35	ns
t_{PHL}		C_L = 50 pF		–	16	35	
t_{PZL}	Maximum Output Enable Time, G or DIR Input to A or B Output	R_L = 1 kΩ	C_L = 50 pF	–	20	45	ns
t_{PZH}			C_L = 50 pF	–	20	45	
t_{PHZ}	Maximum Output Disable Time, G or DIR Input to A or B Output	R_L = 1 kΩ, C_L = 50 pF		–	20	45	ns
t_{PLZ}				–	20	45	
t_w	Pulse Duration, Clock High or Low			12	–	–	ns
t_{SU}	Setup Time, A before CAB ↑ or B before CAB ↑			15	–	–	ns

Pin Description

Symbol	Description
A1 ~ A8	Bi-directional data bus and register input
B1 ~ B8	Bi-directional data bus and register input
$\overline{G}$	Output enable. This pin is an active low pin, when high all outputs are disabled and A and B ports are isolated.
DIR	Direction control. This pin is used to determine the direction of data flow. When DIR = 1 ⇒ From A → B DIR = 0 ⇒ From B → A
SAB SBA	Determines whether data transmitted is from the data inputs or the register associated with those pins. When SAB (SBA) = 1 ⇒ Register → B (A) Bus. SAB (SBA) = 1 ⇒ A (B) → B (A)
CAB CBA	Positive trigger clock. When rising edge is triggered, data from A (B) input are loaded into their associated register.

The transceiver function can work only when $\overline{G}$ is active low (G=0). DIR determines the direction of data flow. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both.

Enable ($\overline{G}$) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when enable $\overline{G}$ is active (low). In the isolation mode (control $\overline{G}$ high). Data may be stored in one register and/or B data may be stored in the other register.

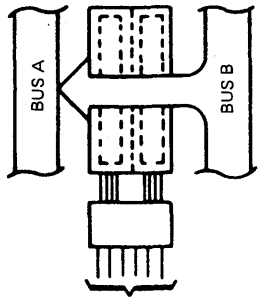
When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

Function Table

Inputs						Data I/O†		Operation or Function
G	DIR	CAB	CBA	SAB	SBA	A1 Thru A8	B1 Thru B8	
X	X	↑	X	X	X	Input	Not specified	Store A, B unspecified
X	X	X	↑	X	X	Not specified	Input	Store B, A unspecified
H	X	↑	↑	X	X	Input	Input	Store A and B Data
H	X	H or L	H or L	X	X			Isolation, hold storage
L	L	X	H or L	X	L	Output	Input	Real-time B Data to A Bus
L	L	X	X	X	H			Stored B Data to A Bus
L	H	H or L	X	L	X	Input	Output	Real-time A Data to B Bus
L	H	X	X	H	X			Stored A Data to B Bus

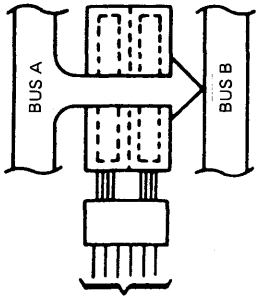
† The data output functions may be enabled or disabled by various signals at the G and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

Bus Management Functions



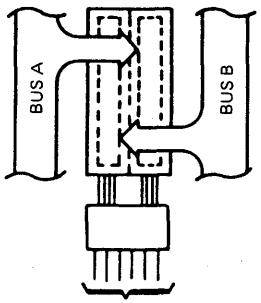
(21) $\overline{G}$	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	L	X	H or L	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



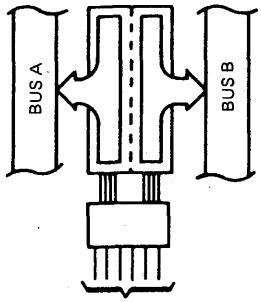
(21) $\overline{G}$	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	H	H or L	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



(21) $\overline{G}$	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

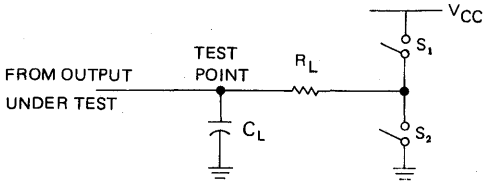
STORAGE FROM
A, B, OR A AND B



(21) $\overline{G}$	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	L	X	X	X	H
L	H	X	X	H	X

TRANSFER
STORED DATA
TO A OR B

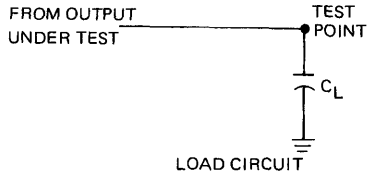
Parameter Measurements



LOAD CIRCUIT

Parameter		R_L	C_L	S_1	S_2
t_{en}	t_{PZH}	1 KΩ	50 pF	OPEN	CLOSED
	t_{PZL}			CLOSED	OPEN
t_{dis}	t_{PHZ}	1 KΩ	50 pF	OPEN	CLOSED
	t_{PLZ}			CLOSED	OPEN

Figure 1. 3-state Outputs



Parameter		C_L
t_{pd} or t_t	Standard outputs	50 pF
	High-current outputs	50 pF

Figure 2. Totem-Pole Outputs

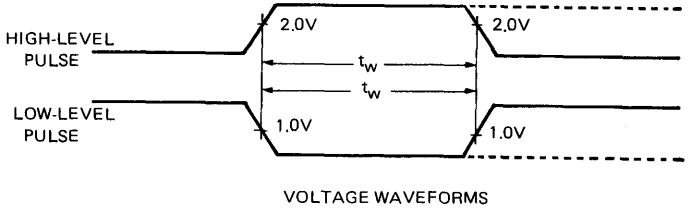


Figure 3. Pulse Durations

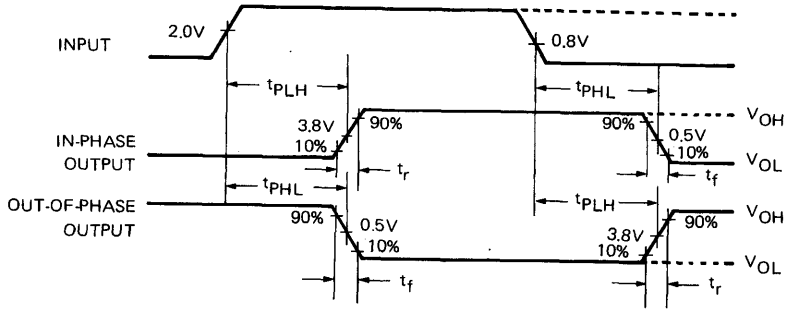


Figure 4. Propagation Delay Times and Output Transition Times

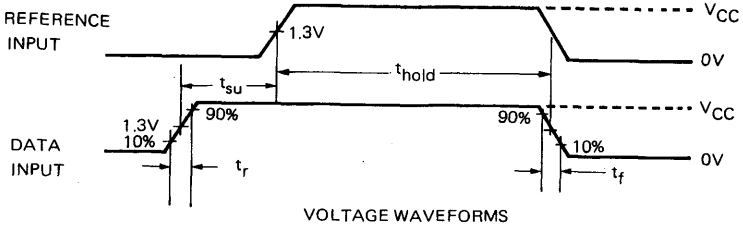


Figure 5. Setup and Hold Times and Input Rise and Fall Time

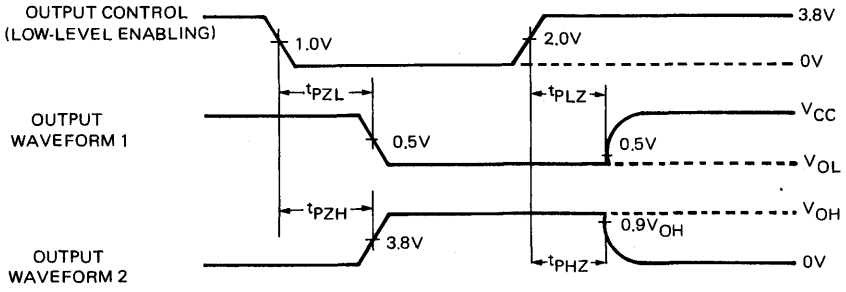


Figure 6. Enable and Disable Times for 3-state Outputs

Ordering Information

Number	Package
UM74HCT646	24L DIP

UMC

UM82C088

PC/XT Integration Chip

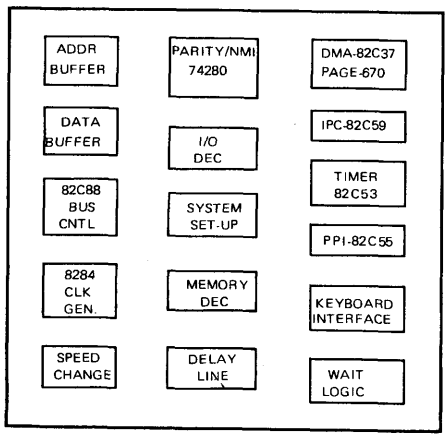
Features

- Fully IBM-PC/XT compatible
- 82C84 Clock generator with 2 clock-inputs to generate the CPU clock. These are 14.318 MHz and 30 MHz which will support 4.77 MHz and 10 MHz CPU clocks with 1/3 duty cycle.
- 82C88 Bus Controller
- 82C37 4 channel DMA controller, channel 0 is used for DRAM refresh
- 82C59 8 channel interrupt controller, level 0 is used for system time base, and level 1 for keyboard input
- 82C53 3 channel timer, channel 0 is used for system time base, channel 1 for DRAM refresh, and channel 2 for speaker audio
- 82C55 Peripheral I/O, used for keyboard interface and system configuration switch (same as the PC/XT)
- 74322 Keyboard interface, supports PC/XT type keyboard
- 74280 Parity check and generator
- 74670 4 bit page register for DMA
- Wait state logic
- NMI control logic
- ROM decoder for one 2764 and one 27256
- RAM decoder for 4164 or 41256 DRAM
- H/W and S/W CPU speed change and indicator
- Built-in delay line for RAS, CAS
- Low power consumption: less than 300 mW at 10 MHz CPU speed
- Small PCB size: 100 pin plastic Flat package

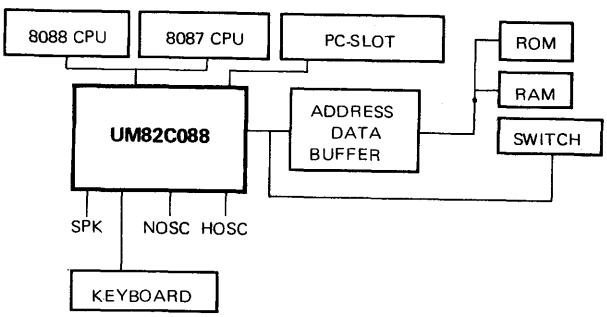
General Description

The UM82C088 is an IC specifically designed to function as the peripheral controller for 8088 microprocessors in an IBM PC/XT compatible computer. It is implemented in 1.5μ CMOS technology and is packaged in a 100 pin plastic flat package.

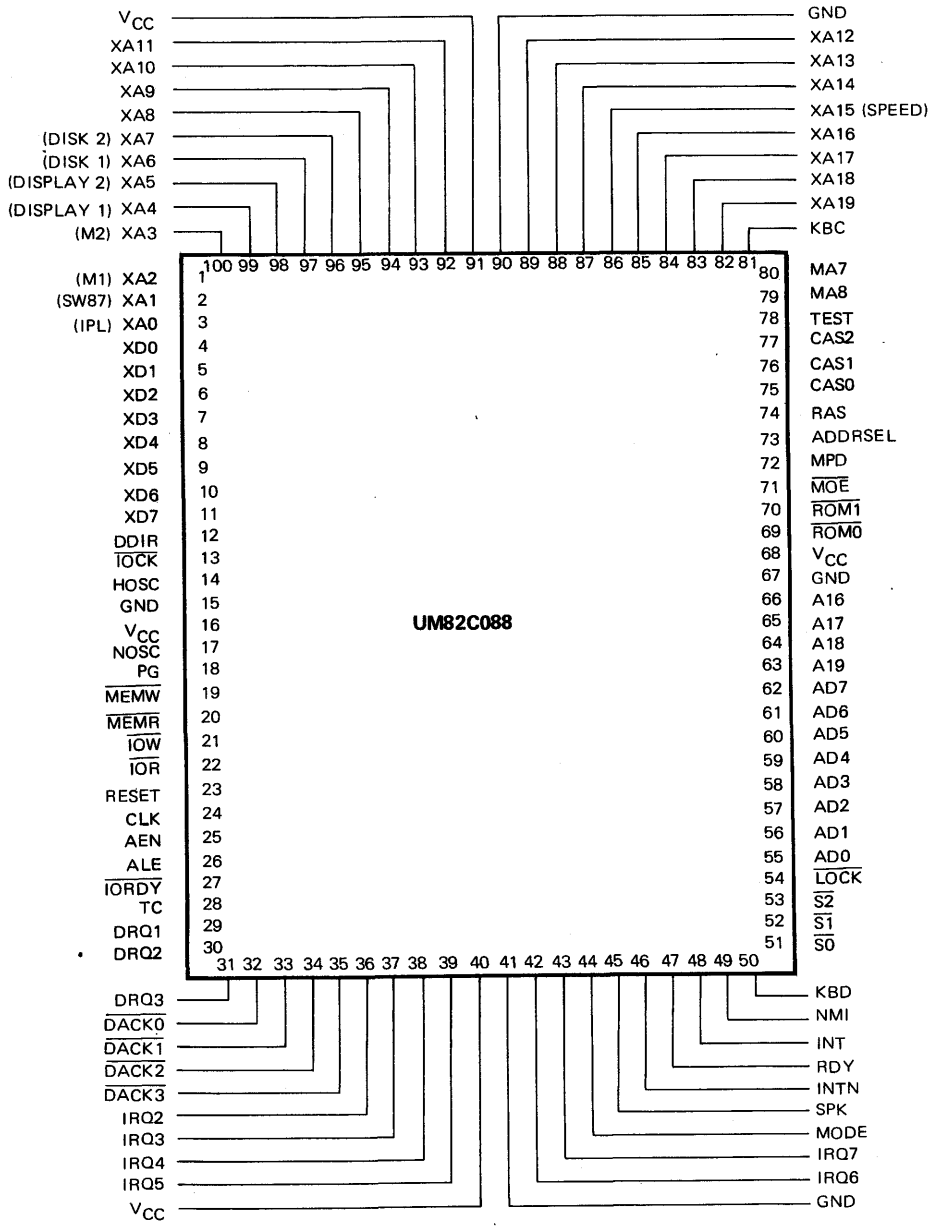
Block Diagram



System Configuration



Pin Configuration



Pin Description

Pin No.	Symbol	I/O	Description
17	NOSC	I	The clock input pin to which a 14.318 MHz clock is attached. The frequency is 3 times the CLK frequency in 4.77 MHz mode.
14	HOSC	I	The 2nd clock input pin to which a high speed clock is attached (max frequency = 30 MHz). The oscillator frequency is 3 times the CLK frequency during high speed mode.
24	CLK	O	The clock output signal used by the 8088 CPU. The frequency of this line is 1/3 duty cycle of NOSC or HOSC, depending on which speed mode is selected.
18	PG	I	Power-Good is an active high input signal which is used to generate the RST output. An RC connection can be used to establish a power up reset of proper duration.
23	RST	O	Reset, an active high output signal which is used to reset the CPU and system. Its timing characteristics are determined by pin PG.
22	$\overline{IOR}$	O	This command output line instructs an I/O device to transmit its data on to the data bus. It is supported by the internal 82C88 during the CPU cycle or the internal 82C37 during the DMA cycle. This signal is active low.
21	$\overline{IOW}$	O	This command output line instructs an I/O device to read the data on the data bus. It is supported by the internal 82C88 during the CPU cycle or the internal 82C37 during the DMA cycle. This signal is active low.
20	$\overline{MEMR}$	O	This command output line instructs the memory to drive its data onto the data bus. It is supported by the internal 82C88 during the CPU cycle or the internal 82C37 during the DMA cycle. This signal is active low.
19	$\overline{MEMW}$	O	This command output line instructs the memory to record the data present on the data bus. It is supported by the internal 82C88 during the CPU cycle or the internal 82C37 during the DMA cycle. This signal is active low.
26	ALE	O	Address latch enable. This output signal serves to strobe the address from CPU into the address latch. This signal is active high.
25	AEN	O	Address enable output. Used to control the system bus for the CPU or DMA. When high, the DMA controller has control of the address bus, data bus and command lines.
51 ⋮ 53	$\overline{S0}$ ⋮ $\overline{S2}$	I	Status input pin from the CPU. The internal 82C88 decodes these inputs to generate command and control signals at the appropriate times.
54	$\overline{LOCK}$	I	Input pin that indicates that the internal 82C37 is not to gain control of the system bus while lock is active low.
49	NMI	O	Non-maskable interrupt. An edge trigger (a transition from low to high) output to the 8088 CPU which causes a type 2 interrupt. (a transition from low to high). There are three different sources to generate NMI: one is input from lock, the others are internal parity check logic and INTN input.

Pin Description (Continued)

Pin No.	Symbol	I/O	Description
48	INT	O	Interrupt output, this pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU and is generated from internal 82C59.
46	INTN	I	Input from external 8087 NPX to generate an NMI output to indicate an error condition of 8087.
47	RDY	O	Ready output. This output acknowledges the internal wait logic or $\overline{\text{IORDY}}$ input pin, which will complete the data transfer. This signal is active high.
27	$\overline{\text{IORDY}}$	I	Input signal used to insert wait state into CPU & DMA bus cycles.
71	$\overline{\text{MOE}}$	O	Output signal used to enable the external memory buffer, which is selected by internal memory decoder logic ($\overline{\text{ROM0}}$-$\overline{\text{ROM1}}$ & CAS0-CAS2). This line is active low.
12	DDIR	O	Output signal which controls the direction of pins XD0-XD7. A high on this line indicates data from system to chip, and low on this line indicates data from chip to system.
74	RAS	O	Memory column address, active high.
75 ⋮ 77	CAS0 ⋮ CAS2	O	Generated by internal memory decoder logic to strobe DRAM column address, address range from 00000H to 9FFFFH, total 3 banks for 256KB DRAM (max. 640KB). These signals are active high.
73	ADDRSEL	O	Address select used to select the DRAM row-address or column-address. A high indicates the row address has been selected and a low indicates the column address is enabled.
79 80	MA8 MA7	O	Provides DRAM chips MA7, MA8 address lines. First cycle is row-address and second cycle is column address and refresh cycle address.
72	MPD	I/O	Memory parity data. Inputs when $\overline{\text{MEMR}}$ is active, and outputs when $\overline{\text{MEMW}}$ is active. Used for internal parity-check logic.
69 70	$\overline{\text{ROM0}}$ $\overline{\text{ROM1}}$	O	Generated by internal memory decoder logic to enable the external EPROM chips. Address Ranges from F6000H to FFFFFH max, to select two 27256s or one 2764 and one 27256. These lines are active low.
55 ⋮ 62	AD0 ⋮ AD7	I/O	Address/Data bus. These eight lines constitute the time in multiplexed memory/IO address & data buses, which are connected directly to the 8088 CPU AD0-AD7 bus.
66 ⋮ 63	A16 ⋮ A19	I	Address bus. These are the four most significant address lines for memory/IO operations and are connected directly to the 8088 CPU A16/S3-A19/S6 bus.
3 ⋮ 1 100 ⋮ 96	XA0 ⋮ XA7	I/O	Address bus. Comes from system buses AD0-AD7 which are internally latched by ALE during the CPU-Cycle, and are supported by the internal 82C37 during the DMA-Cycle.

Pin Description (Continued)

Pin No.	Symbol	I/O	Description
85 ⋮ 82	XA16 ⋮ XA19	O	Address bus comes from system buses A16-A19 which are outputs only.
4 ⋮ 11	XD0 ⋮ XD7	I/O	Data bus outputs when the CPU write is active from the system bus AD0-AD7. Inputs when the CPU read is active or during the DMA cycle.
95 ⋮ 92 89 ⋮ 86	XA8 ⋮ XA15	I/O	Address pins A8 through A15 are Bi-directional and are supported by the external 8088 CPU A8-A15 bus during the CPU cycle, and by the internal 82C37 during the DMA cycle.
36 ⋮ 39 42 ⋮ 43	IRQ2 ⋮ IRQ7	I	These six input-only signals are used to generate interrupt requests to the CPU from the internal 82C59. IRQ2 is highest priority an ' IRQ7 the lowest. A rising-edge signal will generate an INT output to the CPU if the level of the 82C59 is not masked.
29 ⋮ 31	DRQ1 ⋮ DRQ3	I	These three lines are active-high input-only lines used by the peripherals to request DMA cycles, which are connected to the internal 82C37.
32 ⋮ 35	$\overline{\text{DACK0}}$ ⋮ $\overline{\text{DACK3}}$	O	These four signals are low-level active output-only signals issued by the internal 82C37 to indicate that the corresponding DRQ has been honored and the 82C37 will take the bus and proceed with the requested DMA cycle.
28	TC	O	Terminal count. This signal is an output-only active high signal issued by the internal 82C37. It indicates that one of the DMA channels has reached its preprogrammed number of transfer cycles.
13	$\overline{\text{IOCK}}$	I	This is a low-level input-only signal used to report error conditions on the bus-attached interface circuits. This signal when set low, will generate a NMI output.
81	KBC	I/O	Keyboard clock. When pulled low by internal logic, will reset the external keyboard. Otherwise the clock generated by the external keyboard is used as data.
50	KBD	I/O	Keyboard data. When pulled low from internal logic KBD will reset the external keyboard, or a serial data transmitting line from the keyboard to the internal logic, which is SYNC'd with the keyboard clock.
45	SPK	O	Generated from the internal 82C53. Can generate a programmable frequency output to drive an external AMP for a speaker.
44	MODE	O	Speed indicator. A high on this line indicates the CPU is working in high speed mode, a low on this line indicates the CPU is working in 4.77 MHz mode.

Pin Description (Continued)

Pin No.	Symbol	I/O	Description
16 40 68 91	VCC	–	Power supply.
15 41 67 90	GND	–	Ground
78	TEST		This pin is provided for TEST only.

Set Up Descriptions

The following set up signals are multiplexed inputs with XA bus, but only available during RST active.

(a) Set up Pin Description

Pin No.	Symbol	I/O	Description
3	IPL	I/O	82C55 port C-BIT 0, during port B-BIT 3 = 0.
2	SW87	I/O	82C55 port C-BIT 1, used to decide 8087 existence during port B-BIT3 = 0.
1 100	M1 M2	I/O	Memory size setting Port OEOH, Bit 4, 5.
99 98	DISPLAY1 DISPLAY2	I/O	82C55 port C-Bit 0, 1. Used to decide display card type during port B-Bit 3 = 1.
97 96	DISK1 DISK2	I/O	82C55 port C-Bit 2, 3. Used to decide disk number during port B-Bit 3 = 1.
86	HL	I/O	Select CPU speed, 1 = Low, 0 = High.

(b) Set up DIP-SW Description

SW NO	Description		ON	OFF	SW NO	Description		ON	OFF
SW-1		Speed	H1	L0	SW-5	6-ON	Disk	EGA	CGA
SW-2		8087	W/O	W		6-OF	Type	–	MGA
SW-3	4-On	Mem Size	640K	512K	SW-7	8-On	Disk No.	1 Disk	2 Disk
	4-Off		–	256K		8-Off		3 Disk	4 Disk

Functional Description

Clock Generator

The clock generator is the functional equivalent of an 82C84 generator. It also generates the clock for the timer.

Features:

- Generates system clock for the 8088.
- Frequency sources are TTL signals
- TTL outputs for peripheral devices.
- Power-up reset for the processor.
- READY synchronization.

Bus Controller

The bus controller is the functional equivalent of an 8288 for CPU bus operations, and generates the bus controls for CPU operations.

Mode Controller

The system clock can be switched via either software or hardware:

Software user can write port $\phi C\phi H$ to select the system clock. A write command to this port will toggle CPU speed.

Hardware user can utilize a button key or a jumper to XA15 (HL) signal to select the appropriate mode during power on reset.

Each switching manner is independent of the other. Hardware setting is recognized only when RST is active, after then the system clock can be switched only by software.

Wait State Generator

When system clock is running at 4.77 MHz, the wait state generator generates one wait state on all CPU I/O and DMA operations. When system clock is 10 MHz, the wait state generator inserts 4 wait states on all CPU I/O operations and 1 wait state on all DMA operations. It also synchronizes the external ready (I/O CHRDY) that may be used to generate wait states for slower I/O devices.

No wait state is inserted for on-board memory access. When the system clock is running at the turbo rate (10 MHz) two wait states will be inserted for memory access on the expansion slots.

Inserted wait state:

	Low	High
Onboard Memory	0	0
Onboard I/O	1	4
Slot Memory	0	2
Slot I/O	1	4
DMA	1	1

DMA

The DMA (Direct Memory Access) is the functional equivalent of an 82C37 DMA controller. This function improves the microprocessor's system by allowing external devices to directly transfer information from the system memory. Channel 0 is reserved for the refresh of RAM memory.

Features:

- Address increment or decrement.
- Four independent DMA channels.
- Software DMA request. Enable/disable control of individual DMA requests. Independent autoinitialization of all channels.

Interrupt Controller

The programmable interrupt controller in the UM82C088 functions as a system-wide interrupt manager in a Turbo XT system, which is compatible to an Intel 82C59 interrupt controller. This function controls when and which I/O device is being serviced by the microprocessor in an efficient manner.

Features:

- Eight level priority controller.
- Programmable base vector address.
- Programmable interrupts modes (algorithms).
- Compatible with the 8088.

Timer

The timer is the functional equivalent of an 82C53 timer. Channel 0 is tied to interrupt 0, channel 1 is used to generate refresh, and channel 2 is used for the speaker port.

Features:

- Three independent 16-bit counters.
- Count binary or BCD.

PIO

The PIO is used for system configuration, to control the keyboard and speaker ports, and to enable error checks.

Keyboard Port

The keyboard port connects to an IBM compatible keyboard.

Parity Generator

The parity generator checks and generates even parity for RAM memory.

*Remarks:

(1) Port 0C0H: Write only.
A write command to this port will toggle CPU speed.

(2) Port 0E0H: Status Read only.

Bit 4	Bit 5	Bit 6	Bit 7
M1	M2	X	Speed mode

Memory Size.
11: 256KB
01: 512KB
-0: 640KB

0 Low
1 High

Programming

The UM82C088 accepts I/O read/write commands from the CPU.

I/O Address Map

Address	Definition
000H-01FH	DMA Contoller (82C37)
020H-03FH	Interrupt Controller (82C59)
040H-05FH	System Timer (82C53)
060H-07FH	Parallel port (82C55)
080H-09FH	DMA Page Register (74670)
0A0H-0BFH	NMI Mask Register
0C0H-0C3H	Change Speed
0E0H-0E3H	Status

The timer is programmed the same as the 82C53 timer, the DMA controller is programmed the same as the 82C37 DMA controller, and the interrupt controller is programmed the same as the 82C59 interrupt controller.

PIO

The PIO is the equivalent of the 82C55 PIO, but it is configured in a fixed way for system configuration, controling the speaker port, and the keyboard port.

Keyboard Data Register

The keyboard data register is a read only register that is used to read data from the keyboard. When a character is in the register, interrupt 1 will be sent to the interrupt controller. The register may be cleared by setting bit 7 of the PIO register.

DC Electrical Characteristics (V_{CC} = 4.75 to 5.25V, T_A = 0 to 70°C)

Symbol	Parameter	Min.	Max.	Unit	Conditions
V_{IL}	Input Low Voltage	–0.3	+0.8	V	
V_{IH}	Input High Voltage	+2.2	V_{CC}+0.3	V	
V_{OL}	Output Low Voltage		+0.4	V	I_{OL} = 4.0 mA
					I_{OL} = 16.0 mA (K_{BC}, K_{BD}, M_{PD} only)
V_{OH}	Output High Voltage	+3.0		V	I_{OH} = –2.0 mA
					I_{OH} = 8.0 mA (M_{PD} only)
V_{IHR}- V_{ILR}	PG Input Hysteresis	0.25		V	
I_{CC}	Operating Supply Current		50	mA	

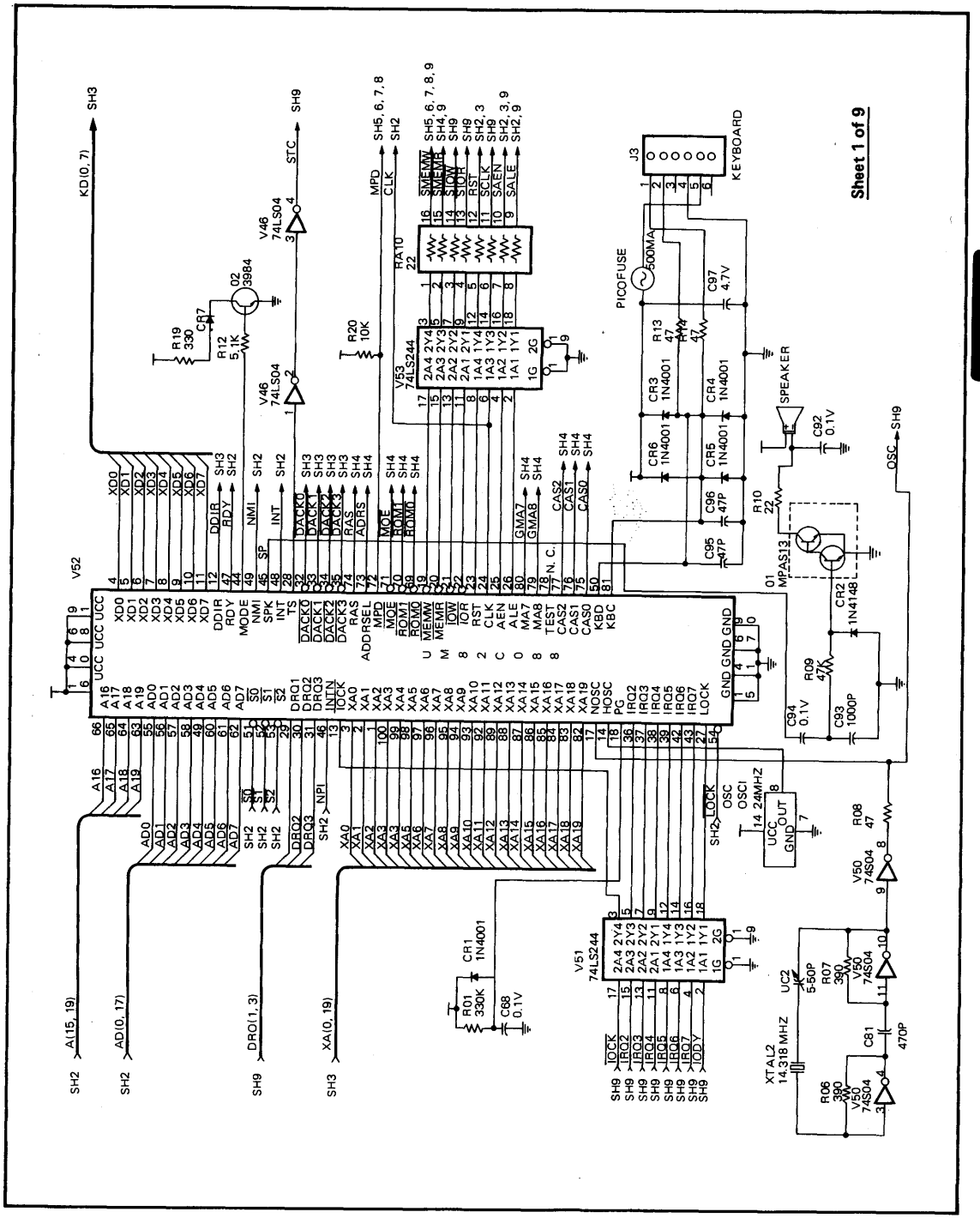
AC Characteristics (V_{CC} = 4.75 to 5.25V, T_A = 0 to 70°C, C_L = 20pF)

Symbol	Parameter	Normal Speed		High Speed		Unit
		Min.	Max.	Min.	Max.	
T1	Input clock period	70		30		ns
T2	Input clock high time	25		12		ns
T3	Input clock low time	25		12		ns
T4	Input clock rising/falling time		3		3	ns
T5	CPU CLK High time	75	82	38	45	ns
T6	CPU CLK Low time	125	133	53	61	ns
T7	CPU CLK cycle period	210		100		ns
T8	High speed mode change to low speed mode CLK high time	110	180			ns
T9	Low speed mode change to high speed mode CLK high time			110	140	ns
T10	RDY delay time	−10	0	−10	0	ns
T11	ALE active delay time (from status)	4	20	4	20	ns
T12	ALE inactive delay time (from CLK)	0	15	0	15	ns
T13	Command active delay time (from CLK)	0	15	0	15	ns
T14	Command inactive delay time (from CLK)	0	15	0	15	ns
T15	Status inactive setup time	35		35		ns
T16	Address (AD0–AD7, XA8–XA15, A16–A19) valid to $\overline{MOE}$ active/inactive delay		40		40	ns
T17	Command active/inactive to RAS active/ inactive, MEM READ cycle		6		6	ns
	Command active to RAS active, MEM WRITE cycle	37	76	20	39	ns
	Command inactive to RAS inactive, MEM WRITE cycle	2	41	2	24	ns
T18	Command active to ADDRSEL active delay, MEM READ cycle	36	73	19	36	ns
	Command active to ADDRSEL active delay, MEM WRITE cycle	106	143	52	69	ns
T19	Command inactive to ADDRSEL inactive delay, MEM READ cycle	36	73	19	36	ns
	Command inactive to ADDRSEL inactive delay, MEM WRITE cycle	71	108	34	54	ns
T20	Command active to CAS active delay, MEM READ cycle	106	145	52	71	ns
	Command active to CAS active delay, MEM WRITE cycle	176	215	83	105	
T21	Command inactive to CAS inactive delay, MEM READ cycle		8		8	ns
	Command inactive to CAS inactive delay, MEM WRITE cycle	2	43	2	26	ns

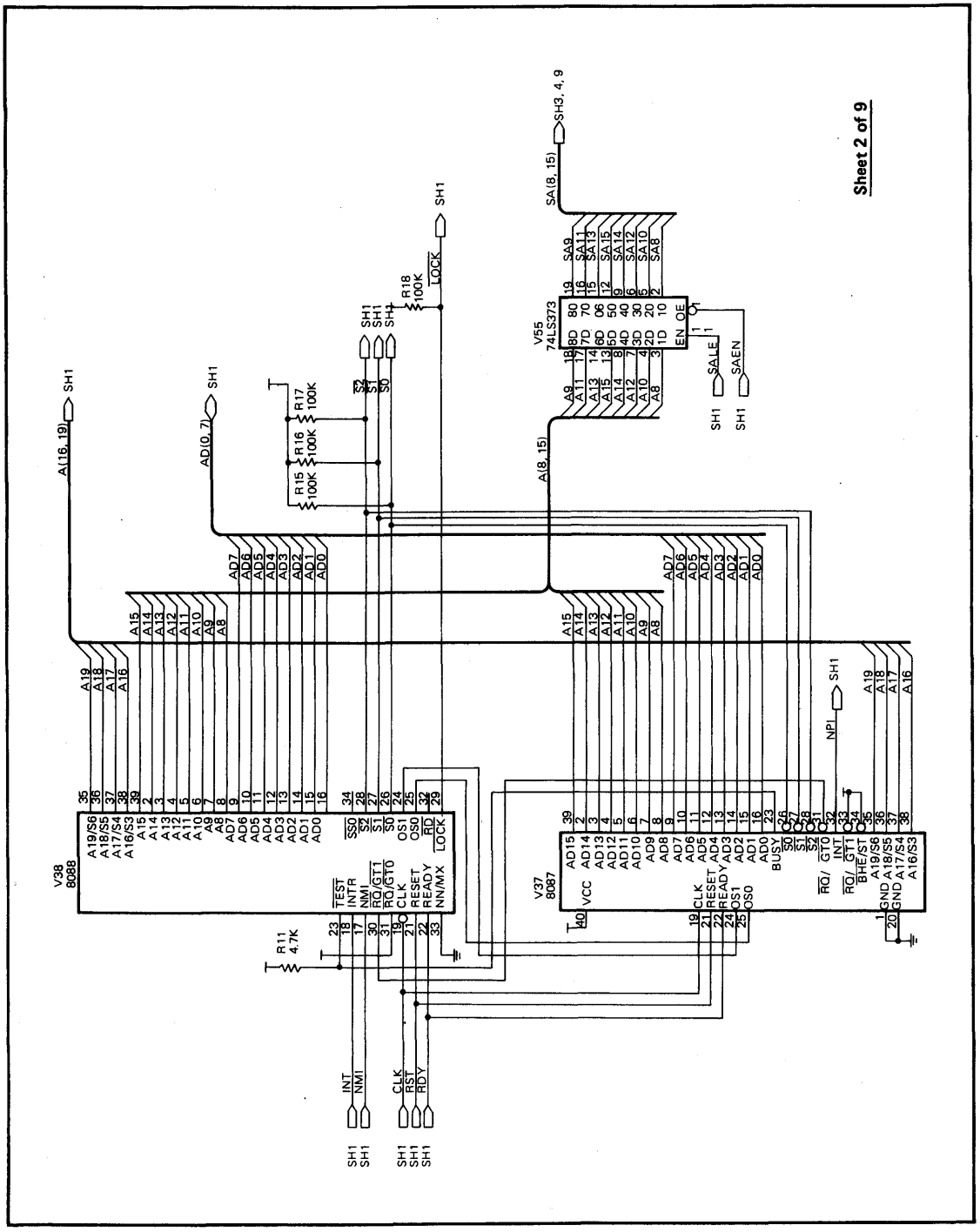
AC Characteristics (Continued)

Symbol	Parameter	Normal Speed		High Speed		Unit
		Min.	Max.	Min.	Max.	
T22	Command to $\overline{MOE}$ delay (ROM cycle)		12		12	ns
T23	Command to $\overline{ROM}$ delay		12		12	ns
T24	XD to AD bus delay		40		40	
T25	Read data hold time	10		10		ns
T26	Command inactive to AD0–AD7 output floating	35		30		ns
T27	Command active to AD0–AD7 active	95	180	23	105	ns
T28	Command active to data valid for on board IOR	115	210	43	135	ns
T29	AD to XD bus, MPD active		40		40	ns
T30	AD to XD bus, MPD inactive delay		40		40	ns
T31	Address setup time	30		30		ns
T32	Address hold time	25		25		ns
T33	CLK to DDIR delay		50		50	ns
T34	On board IOW data setup time	150		150		ns
T35	On board IOW data hold time	25		25		ns
T36	XA address to MA7, MA8 delay		40		40	ns
T37	ADDRSEL to MA7, MA8 delay		10		10	ns
T38	$\overline{DACKX}$ delay time (from DCLK Low)		170		170	ns
T39	AEN active delay time (from DCLK high)		140		140	ns
T40	AEN inactive delay time (from DCLK high)	110	140	100	220	ns
T41	XA15–XA0 active delay time (from DCLK high)		110		110	ns
T42	XA15–XA0 inactive delay time (from DCLK low)	110		100		ns
T43	XA19–XA16 active delay time (from $\overline{DACKX}$ active)		40		40	ns
T44	XA19–XA16 inactive delay time (from DCLK low)	110		100		ns
T45	DMA read command active delay time from DCLK high)		150		150	ns
T46	DMA read command inactive delay time (from DCLK high)		145		145	ns
T47	DMA write command active delay time (from DCLK high)		150		150	ns
T48	DMA write command inactive delay time (from DCLK high)		115		115	ns
T49	DMA cycle DDIR delay time (from AEN)		40		40	ns
T50	TC delay time (from DCLK high)		40		40	ns

Application Circuits



Application Circuits (Continued)



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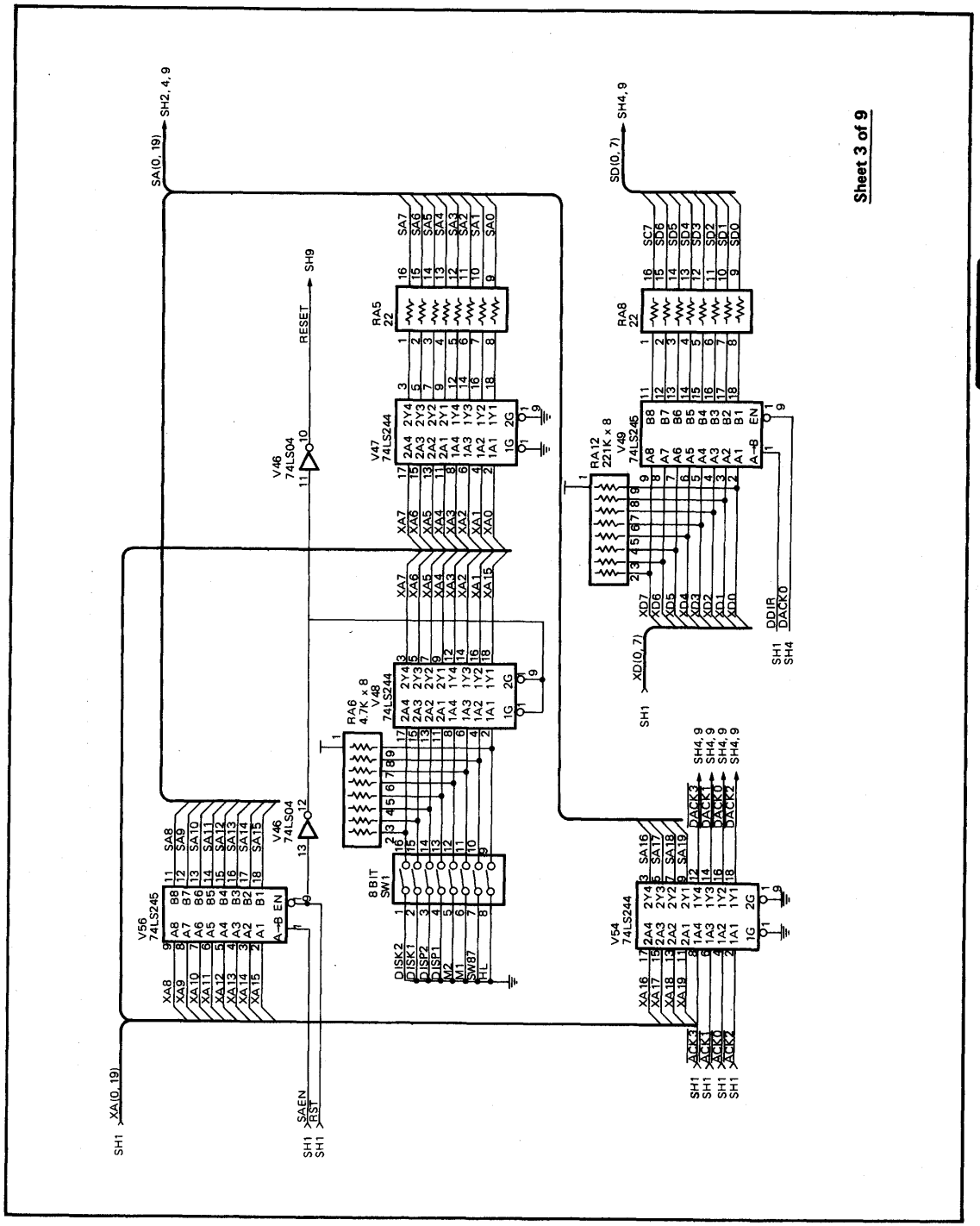
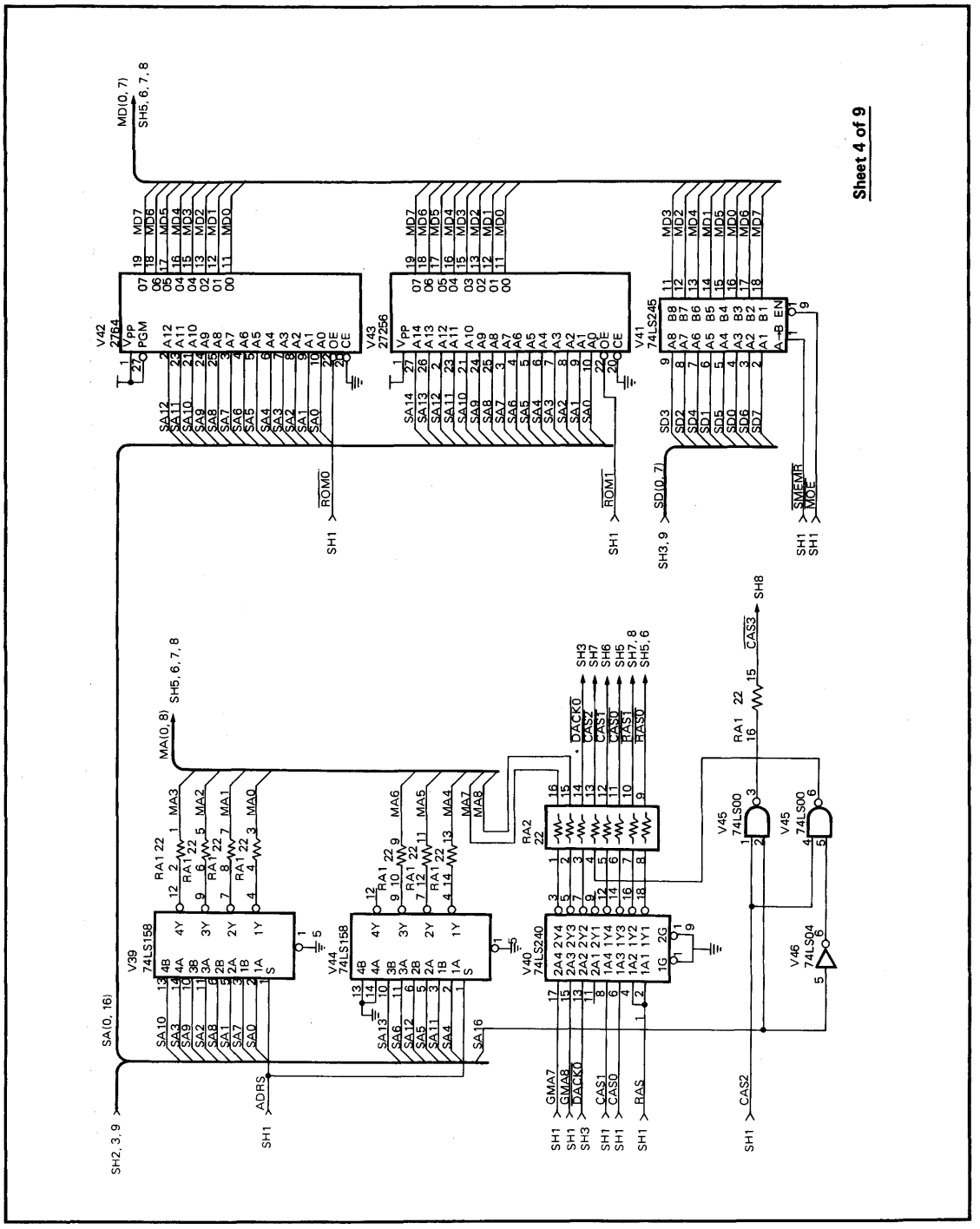


Application Circuits (Continued)



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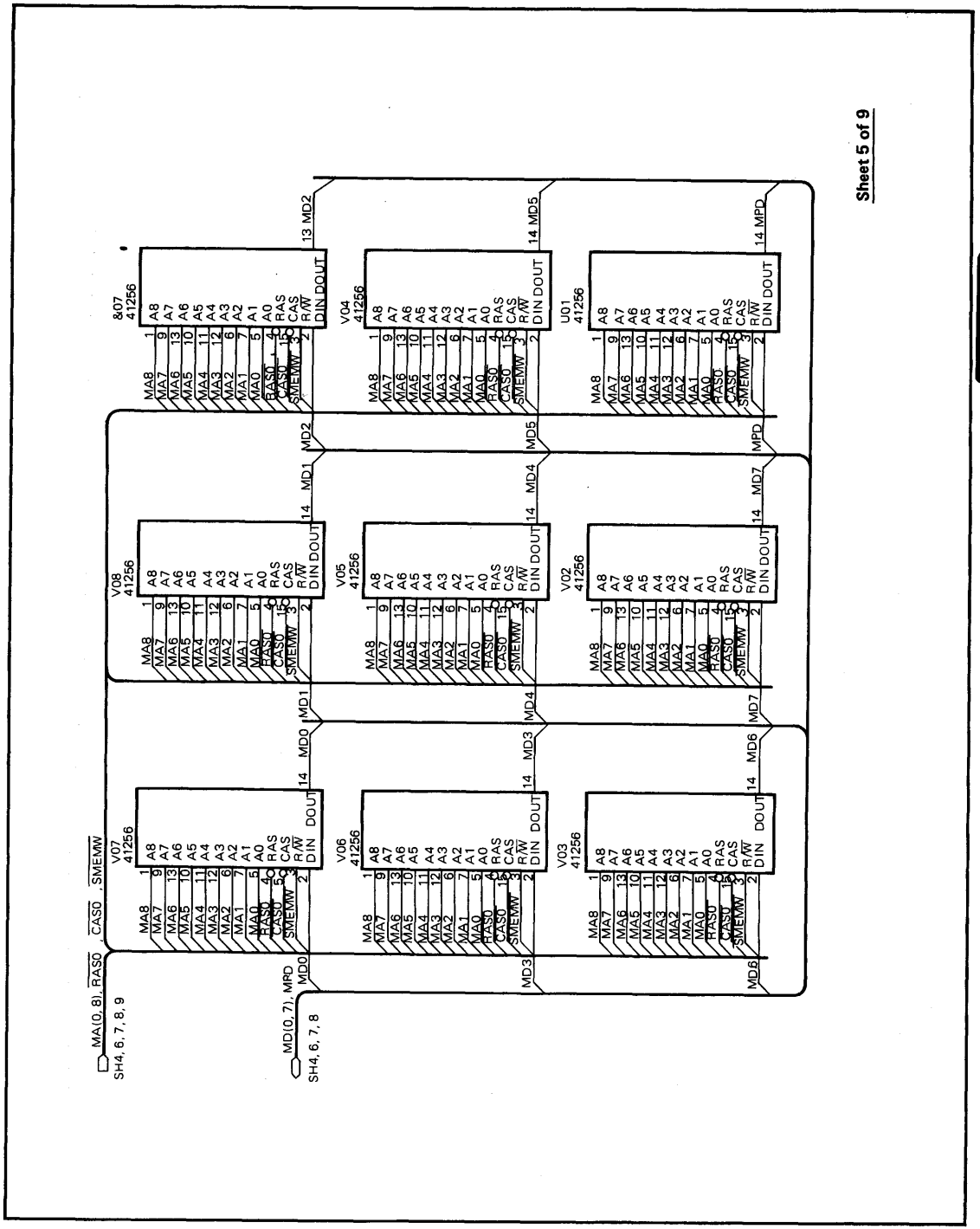

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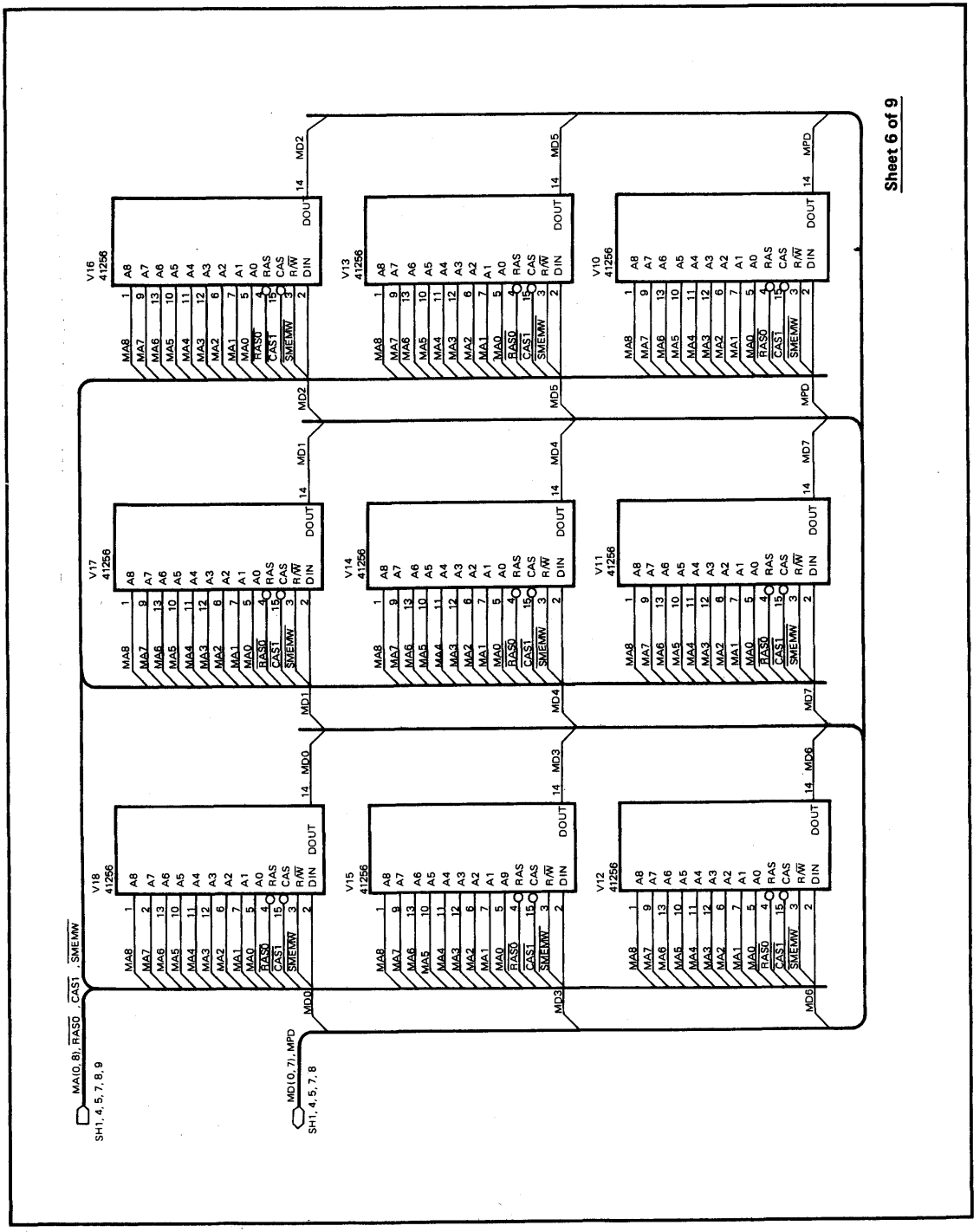

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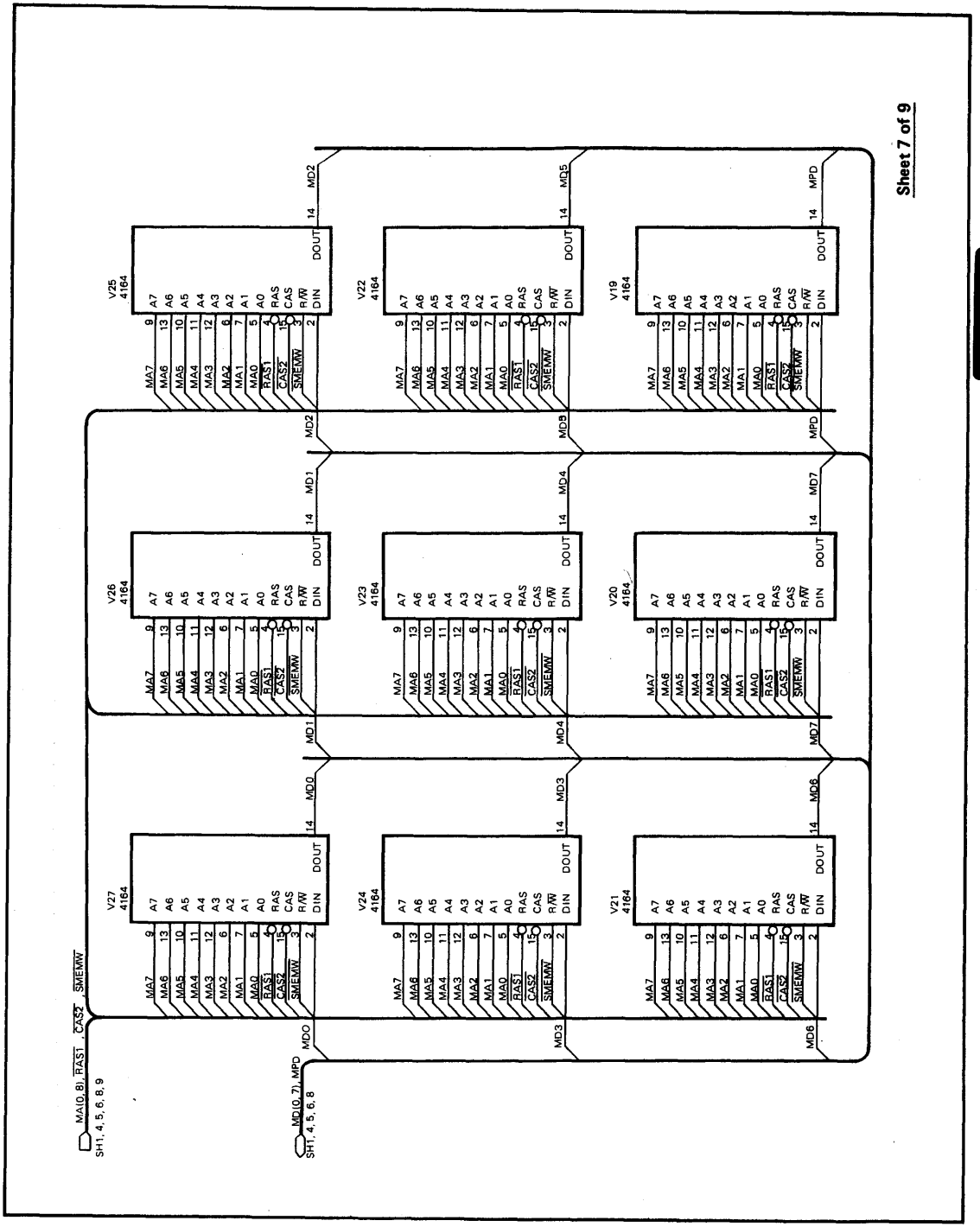

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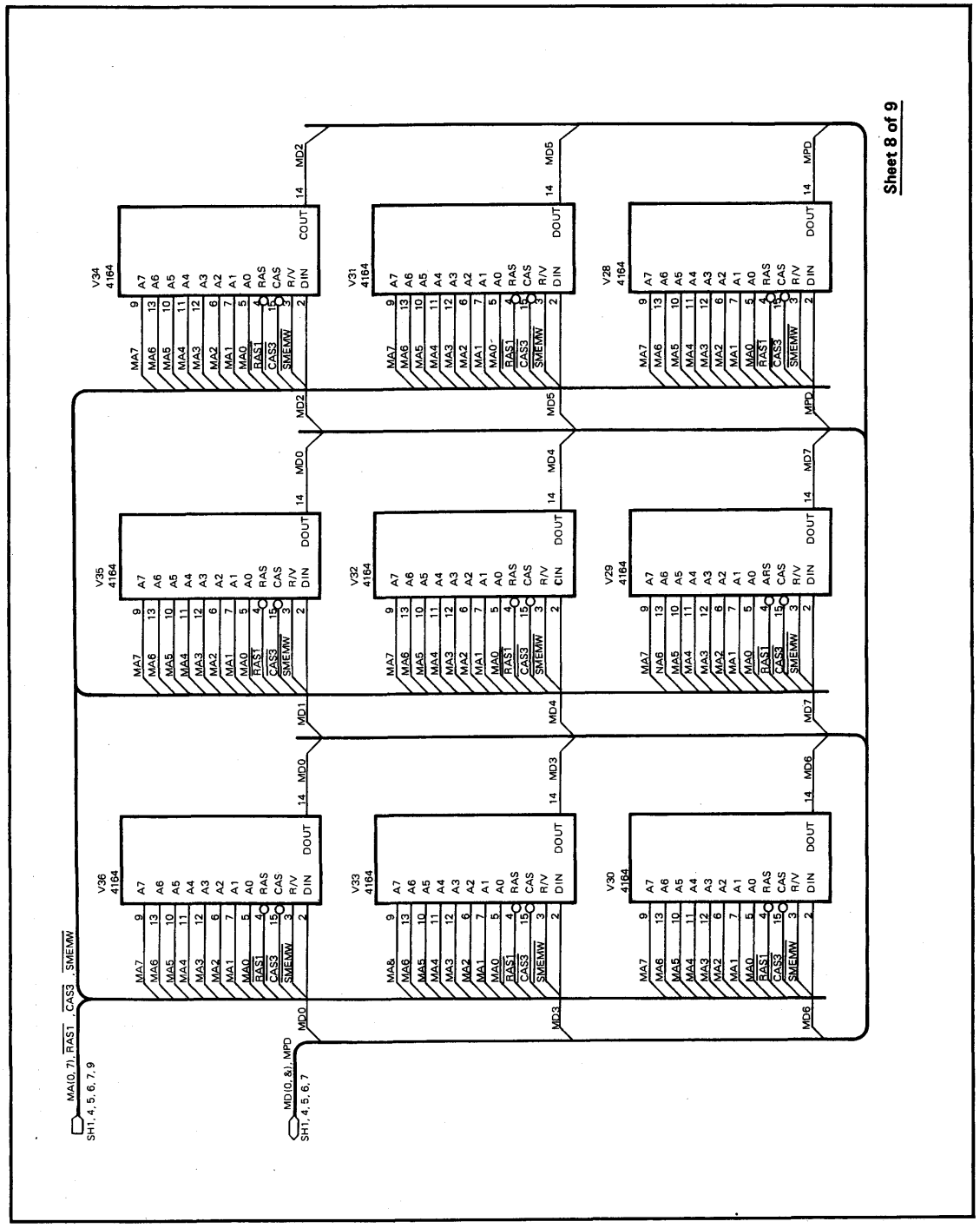

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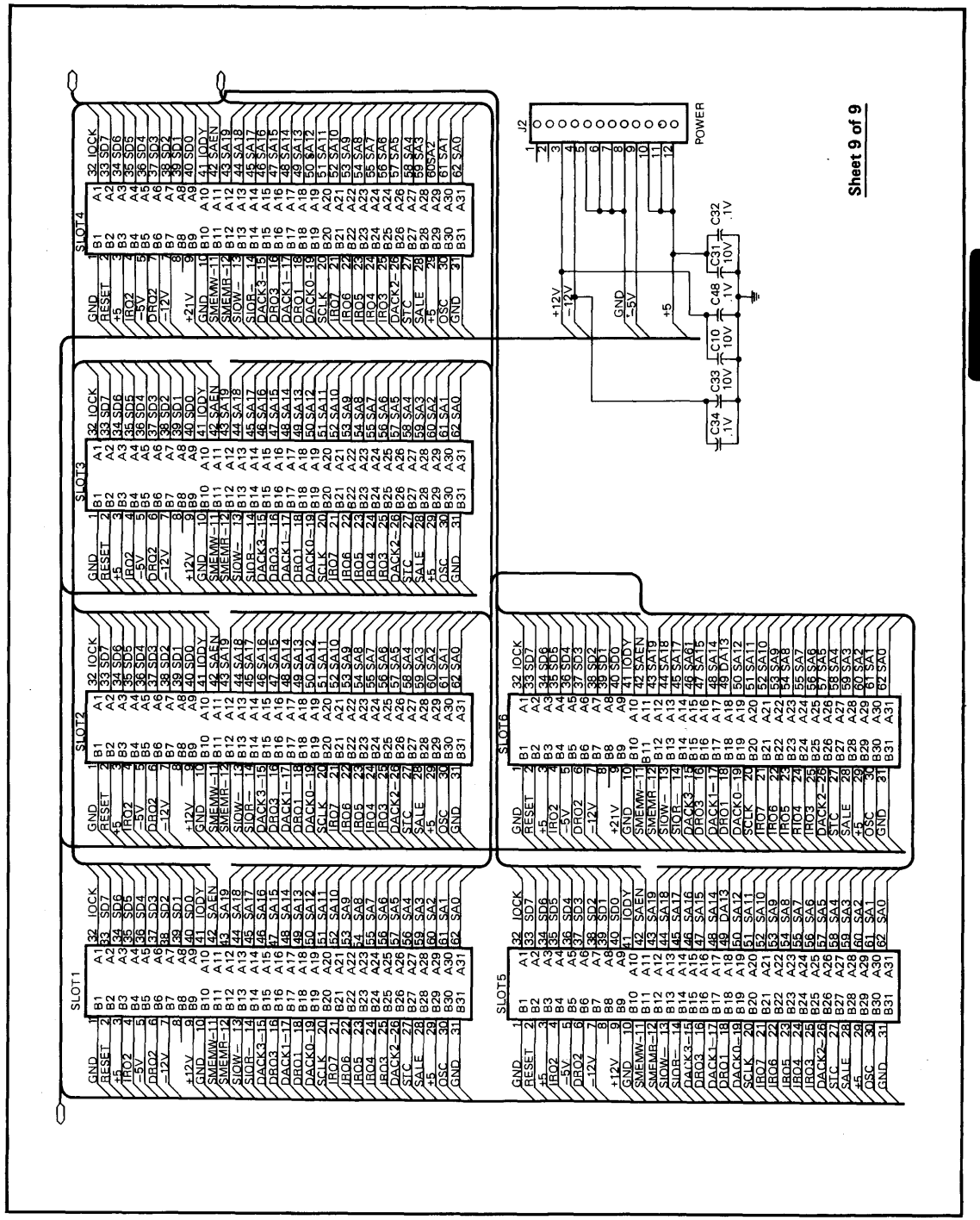
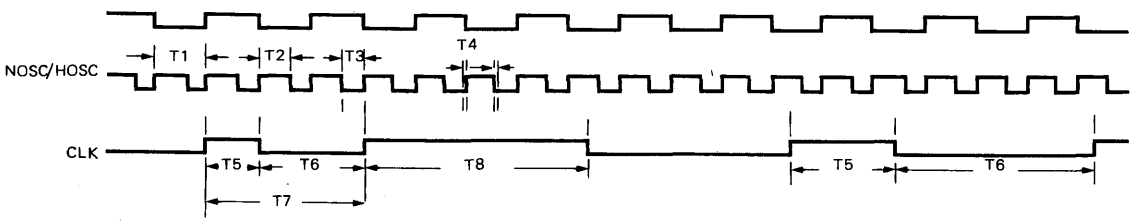
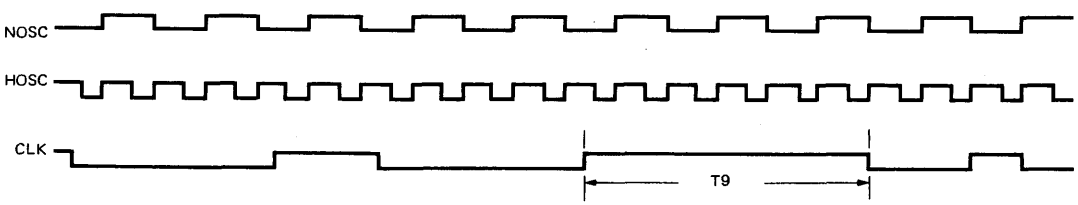


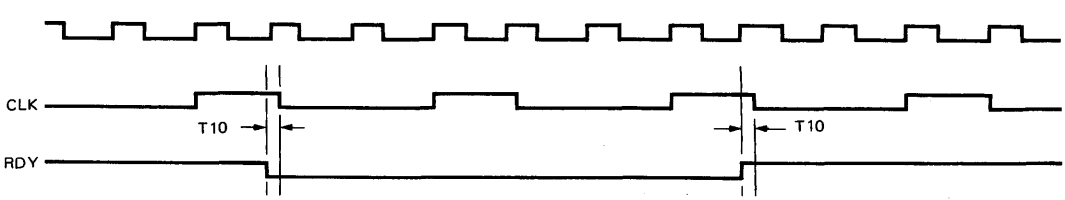
Timing Waveforms



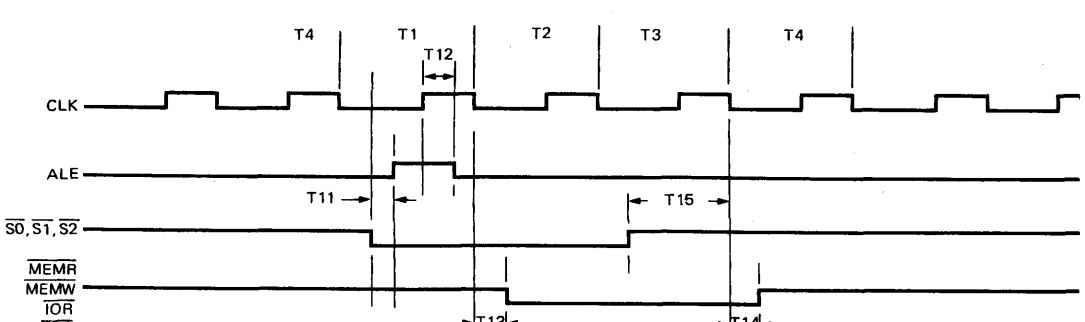
High Speed Change to Low Speed



Low Speed Change to High Speed

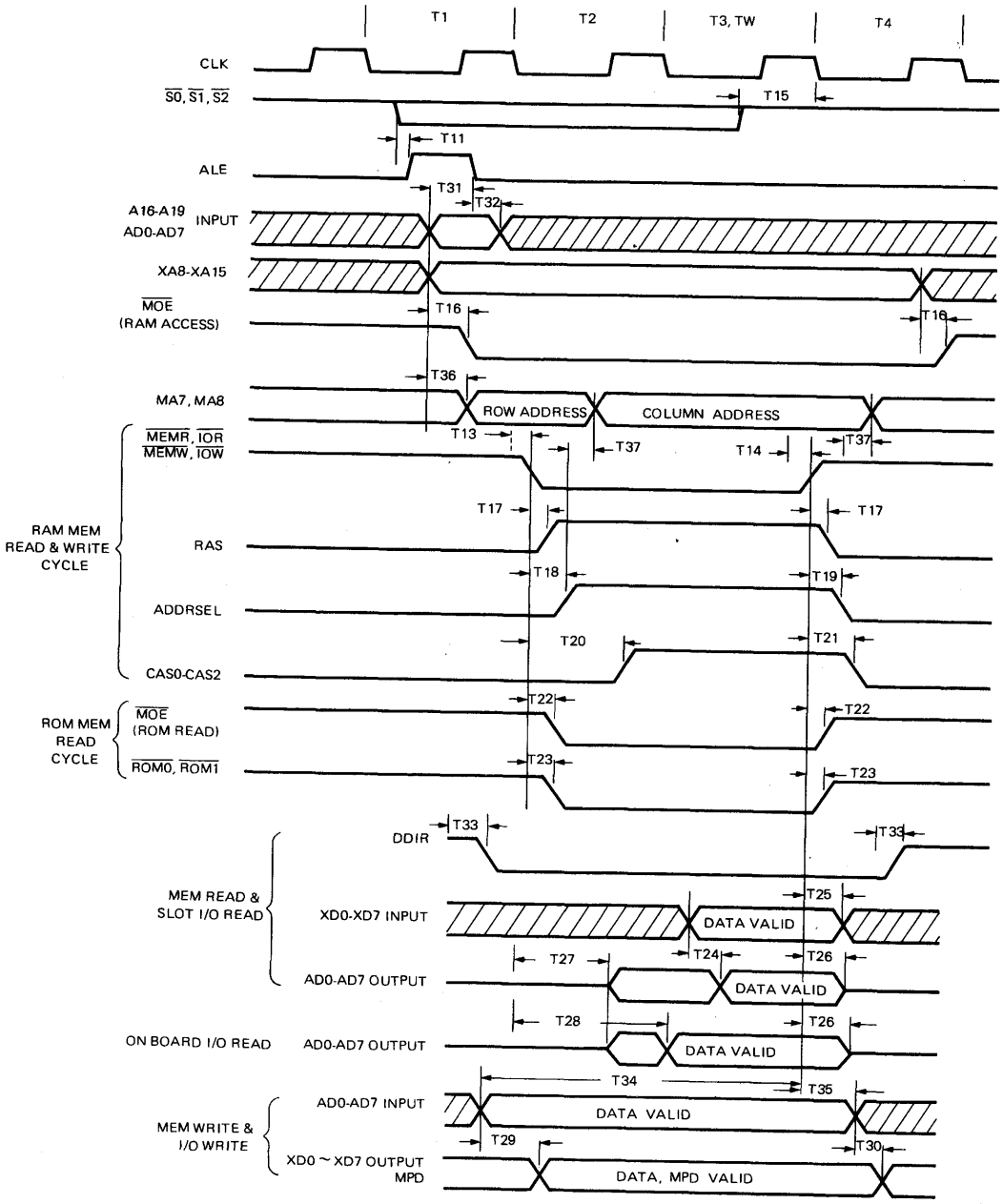


RDY TIMING



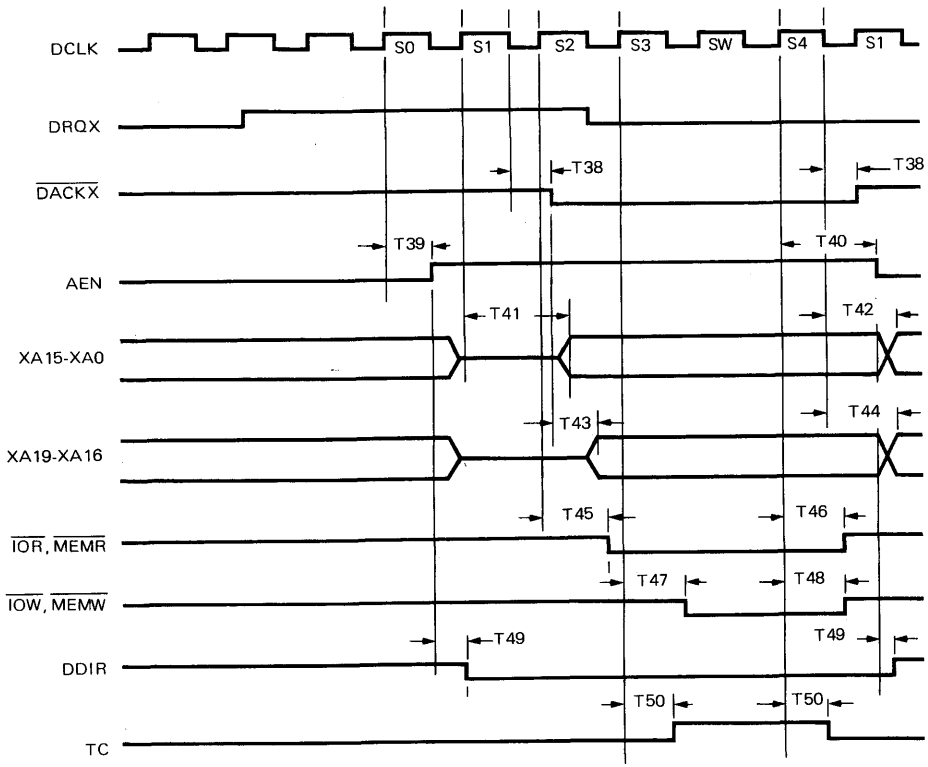
CPU Timing

Timing Waveforms (Continued)



Read, Write Timing

Timing Waveforms (Continued)



DMA Cycle Timing

Ordering Information

Part No.	Package
UM82C088F	100pin F.P.

UMC

UM82C284-10/-12

Clock Generator and Ready Interface

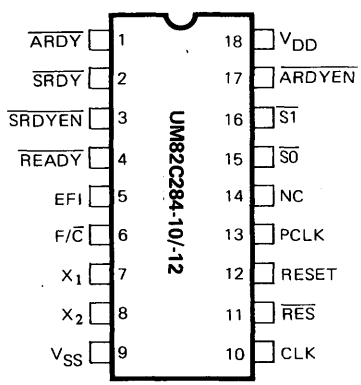
Features

- Generates system clock for 80286 processors
- Uses crystal or TTL signal for frequency source
- Provides local READY and Multibus* READY synchronization
- Single +5V power supply
- Generates system reset output from Schmitt Trigger input
- 10 MHz and 12.5 MHz versions

General Description

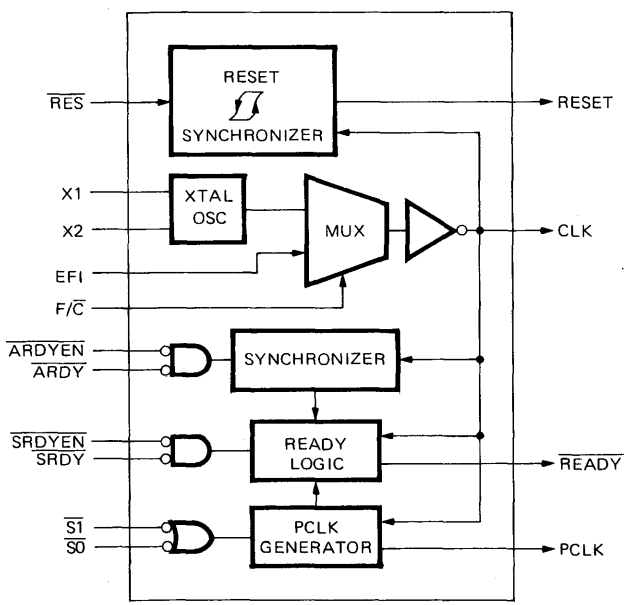
UM82C284-10/-12 is a clock generator/driver which provides clock signals for 80286 processors and support components. It also contains logic to supply $\overline{\text{READY}}$ to the CPU from either asynchronous or synchronous sources and synchronous RESET from an asynchronous input with hysteresis. It is fabricated using the Si-Gate CMOS process.

Pin Configuration



* Multibus is an Intel Trademark

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . −65°C to +150°C
All Output and Supply Voltages . . . . . −0.5V to +7V
All Input Voltages . . . . . −1.0V to +5.5V
Power Dissipation . . . . . 1 Watt

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Description

Symbol	I/O	Description
CLK	O	System Clock is the signal used by the processor and support devices which must be synchronous with the processor. The frequency of the CLK output is twice the desired internal processor clock frequency. CLK can drive both TTL and MOS level inputs.
F/$\overline{C}$	I	Frequency/Crystal Select is a strapping option to select the source for the CLK output. When F/$\overline{C}$ is strapped LOW, the internal crystal oscillator drives CLK. When F/$\overline{C}$ is strapped HIGH, the EFI input drives the CLK output.
X1, X2	I	Crystal In are the pins to which a parallel resonant fundamental mode crystal is attached for the internal oscillator. When F/$\overline{C}$ is LOW, the internal oscillator will drive the CLK output at the crystal frequency. The crystal frequency must be twice the desired internal processor clock frequency.
EFI	I	External Frequency In drives CLK when the F/$\overline{C}$ input is strapped HIGH. The EFI input frequency must be twice the desired internal processor clock frequency.
PCLK	O	Peripheral Clock is an output which provides a 50% duty cycle clock with 1/2 the frequency of CLK. PLCK will be in phase with the internal processor clock following the first bus cycle after the processor has been reset.
$\overline{ARDYEN}$	I	Asynchronous Ready Enable is an active LOW input which qualifies the $\overline{ARDY}$ input. $\overline{ARDYEN}$ selects $\overline{ARDY}$ as the source of ready for the current bus cycle. Inputs to $\overline{ARDYEN}$ may be applied asynchronously to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs.
$\overline{ARDY}$	I	Asynchronous Ready is an active LOW input used to terminate the current bus cycle. The $\overline{ARDY}$ input is qualified by $\overline{ARDYEN}$. Inputs to $\overline{ARDY}$ may be applied asynchronously to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs.
$\overline{SRDYEN}$	I	Synchronous Ready Enable is an active LOW input which qualifies $\overline{SRDY}$. $\overline{SRDYEN}$ selects $\overline{SRDY}$ as the source for $\overline{READY}$ to the CPU for the current bus cycle. Setup and hold times must be satisfied for proper operation.
$\overline{SRDY}$	I	Synchronous Ready is an active LOW input used to terminate the current bus cycle. The SRDY input is qualified by the $\overline{SRDYEN}$ input. Setup and hold times must be satisfied for proper operation.
$\overline{READY}$	O	Ready is an active LOW output which signals that the current bus cycle is to be completed. The $\overline{SRDY}$, $\overline{SRDYEN}$, $\overline{ARDY}$, $\overline{ARDYEN}$, $\overline{S1}$, $\overline{S0}$ and $\overline{RES}$ inputs which control $\overline{READY}$ are explained later in the $\overline{READY}$ generator section. $\overline{READY}$ is an open collector output requiring an external 300 ohm pullup resistor.
$\overline{S0}$, $\overline{S1}$	I	Status inputs prepare the UM82C284-10/-12 for a subsequent bus cycle. $\overline{S0}$ and $\overline{S1}$ synchronize PCLK to the internal processor clock and control $\overline{READY}$. These inputs have pullup resistors to keep them HIGH if nothing is driving them. Setup and hold times must be satisfied for proper operation.
RESET	O	Reset is an active HIGH output which is derived from the $\overline{RES}$ input. RESET is used to force the system into an initial state. When RESET is active, $\overline{READY}$ will be active (LOW).
$\overline{RES}$	I	Reset In is an active LOW input which generates the system reset signal, RESET. Signals to $\overline{RES}$ may be applied asynchronously to CLK. A Schmitt trigger input is provided on $\overline{RES}$, so that an RC circuit can be used to provide a time delay. Setup and hold times are given to assure a guaranteed response to synchronous inputs.
V_{DD}		System Power: +5V power supply.
V_{SS}		System Ground: 0 volts.

Functional Description

Introduction

The UM82C284-10/-12 generates the clock, ready, and reset signals required for 80286 processors and support components. The UM82C284-10/-12 is packaged in an 18-pin DIP and contains a crystal controlled oscillator, MOS clock generator, peripheral clock generator, Multibus ready synchronization logic and system reset generation logic.

Clock Generator

The CLK output provides the basic timing control for an 80286 system. CLK has output characteristics sufficient to drive MOS devices. CLK is generated by either an internal crystal oscillator or an external source as selected by the F/$\overline{C}$ strapping option. When F/$\overline{C}$ is LOW, the crystal oscillator drives the CLK output. When F/$\overline{C}$ is HIGH, the EFI input drives the CLK output.

The UM82C284-10/-12 provides a second clock output (PCLK) for peripheral devices. PCLK is CLK divided by two. PCLK has a duty cycle of 50% and TTL-output drive characteristics. PCLK is normally synchronized to the internal processor clock.

After reset, the PCLK signal may be out of phase with the internal processor clock. The $\overline{S1}$ and $\overline{S0}$ signals of the first bus cycle are used to synchronize PCLK to the internal processor clock. The phase of the PCLK output changes by extending its HIGH time beyond one system clock (see waveforms). PCLK is forced HIGH whenever either $\overline{S0}$ or $\overline{S1}$ were active (LOW) for the two previous CLK cycles. PCLK continues to oscillate when both $\overline{S0}$ and $\overline{S1}$ are HIGH.

Since the phase of the internal processor clock will not change, except during reset, the phase of PCLK will not change, except during the first bus cycle after reset.

Oscillator

The oscillator circuit of the UM82C284-10/-12 is a linear Pierce Oscillator which requires an external parallel resonant, fundamental mode & crystal. The output of the oscillator is internally buffered. The crystal frequency chosen should be twice the required internal processor clock frequency. The crystal should have a typical load capacitance of 32 pF.

X1 and X2 are the oscillator crystal connections. For stable operation of the oscillator, two loading capacitors are recommended, as shown in Figure 1. The sum of the board capacitance and loading capacitance should equal the values shown. It is advisable to limit stray board capacitances (not including the effect of the loading capacitors or crystal capacitance) to less than 10 pF between the X1 and X2 pins. Decouple V_{DD} and V_{SS} as close to the UM82C284/-10/-12 as possible.

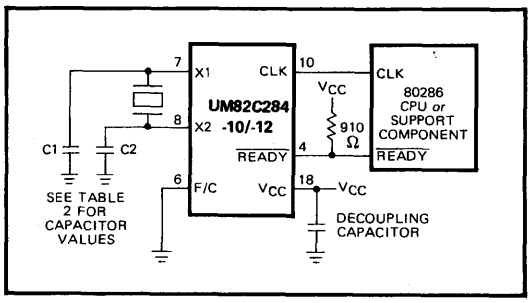


Figure 1. Recommended Crystal and $\overline{READY}$ Connections

Reset Operation

The reset logic provides the RESET output to force the system into a known, initial state. When the $\overline{RES}$ input is active (LOW), the RESET output becomes active (HIGH). $\overline{RES}$ is synchronized internally at the falling edge of CLK before generating the RESET output (see waveforms). Synchronization of the RES input introduces a one or two CLK delay before affecting the RESET output.

At power up, a system does not have a stable V_{DD} and CLK. To prevent spurious activity, $\overline{RES}$ should be asserted until V_{CC} and CLK stabilize at their operating values. 80286 processors and support components also require their RESET Inputs to be HIGH a minimum of 16 CLK cycles. An RC network, as shown in Figure 2, will keep $\overline{RES}$ LOW long enough to satisfy both needs.

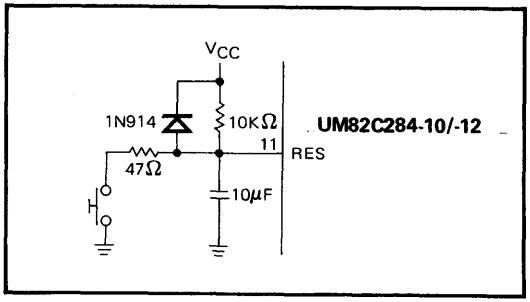


Figure 2. Typical RC $\overline{RES}$ Timing Circuit

A Schmitt Trigger input with hysteresis on RES assures a single transition of RESET with an RC circuit on $\overline{RES}$. The hysteresis separates the input voltage level at which the circuit output switches from HIGH to LOW from the input voltage level at which the circuit output switches from LOW to HIGH. The $\overline{RES}$ HIGH to LOW input transition voltage is lower than the $\overline{RES}$ LOW to HIGH input transition voltage. As long as the slope of the $\overline{RES}$

input voltage remains in the same direction (increasing or decreasing) around the $\overline{RES}$ input transition voltage, the RESET output will make a single transition.

Ready Operation

The UM82C284-10/-12 accepts two ready sources for the system ready signal which terminates the current bus cycle. Either a synchronous ($\overline{SRDY}$) or asynchronous ready ($\overline{ARDY}$) source may be used. Each ready input has an enable ($\overline{SRDYEN}$ and $\overline{ARDYEN}$) for selecting the type of ready source required to terminate the current bus cycle. An address decoder would normally select one of the enable inputs.

$\overline{READY}$ is enabled (LOW), if either $\overline{SRDY}$ + $\overline{SRDYEN}$ = "0" or $\overline{ARDY}$ + $\overline{ARDYEN}$ = "0" when sampled by the UM82C284-10/-12 $\overline{READY}$ generation logic. $\overline{READY}$ will remain active for at least two CLK cycles.

The $\overline{READY}$ output has an open-collector driver allowing other ready circuits to be wire-ORed with it, as shown in Figure 1. The $\overline{READY}$ signal of an 80286 system requires an external 910 ohm ± 5% pull-up resistor. To force the $\overline{READY}$ signal inactive (HIGH) at the start of a bus cycle, the $\overline{READY}$ output floats when either $\overline{S1}$ or $\overline{S0}$ are sampled LOW at the falling edge of CLK. Two system clock periods are allowed for the pull-up resistor to pull the $\overline{READY}$ signal to V_{IH}. When RESET is active, $\overline{READY}$ is forced active one CLK later (see waveforms).

Figure 3 illustrates the operation of $\overline{SRDY}$ and $\overline{SRDYEN}$. These inputs are sampled on the falling edge of CLK when $\overline{S1}$ and $\overline{S0}$ are inactive and PCLK is HIGH. $\overline{READY}$ is forced active when both $\overline{SRDY}$ and $\overline{SRDYEN}$ are sampled as LOW.

Figure 4 shows the operation of $\overline{ARDY}$ and $\overline{ARDYEN}$. These inputs are sampled by an internal synchronizer at each falling edge of CLK. The output of the synchronizer is then sampled when PCLK is HIGH. If the synchronizer finds both the $\overline{ARDY}$ and $\overline{ARDYEN}$ have been resolved as active, the $\overline{SRDY}$ and $\overline{SRDYEN}$ inputs are ignored. Either $\overline{ARDY}$ or $\overline{ARDYEN}$ must be HIGH at the end of T_s (see figure 4).

$\overline{READY}$ remains active until either $\overline{S1}$ or $\overline{S0}$ are sampled LOW, or the ready inputs are sampled as inactive.

Table 2. UM82C284-10/-12 Crystal Loading Capacitance Values

Crystal Frequency	C1 Capacitance (pin 7)	C2 Capacitance (pin 8)
1 to 8 MHz	60 pF	40 pF
8 to 25 MHz	25 pF	15 pF

Note: Capacitance values must include stray board capacitance.

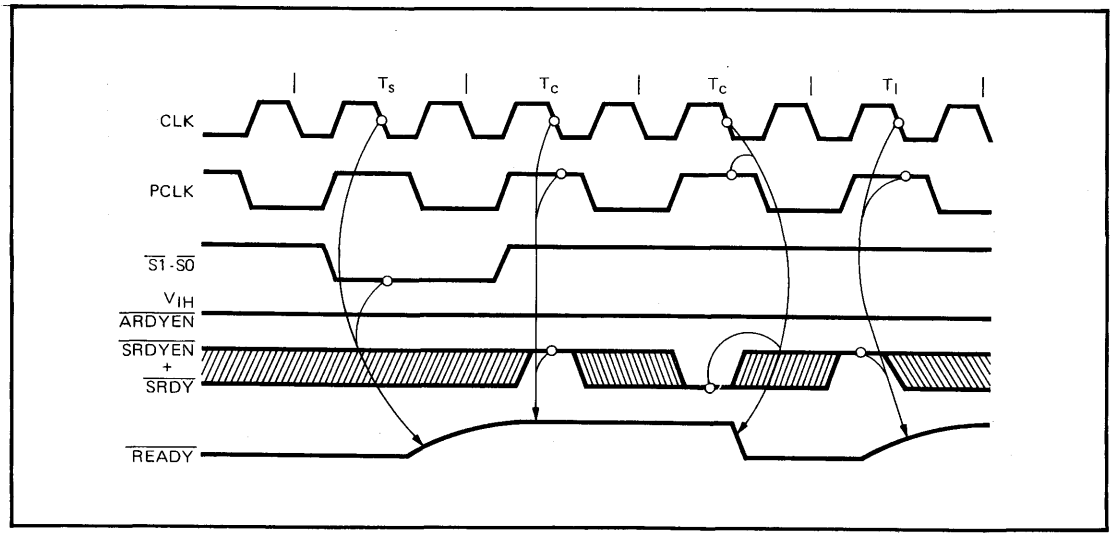


Figure 3. Synchronous Ready Operation

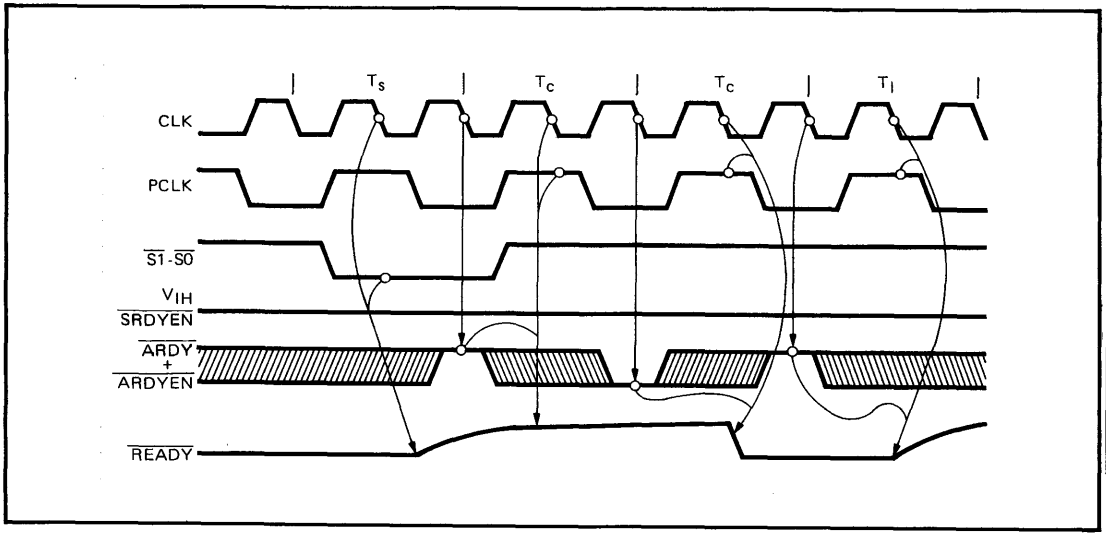


Figure 4. Asynchronous Ready Operation

DC Electrical Characteristics

(T_A = 0°C to 70°C, V_{DD} = 5V, ±10%)

Symbol	Parameter	10 MHz		12.5 MHz		Unit	Conditions
		Min.	Max.	Min.	Max.		
V_{IL}	Input LOW Voltage		0.8		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		2.0		V	
V_{IHR}	$\overline{RES}$ and EFI Input HIGH Voltage	2.6		2.6		V	
V_{HYS}	$\overline{RES}$ Input Hysteresis	0.25		0.25		V	
V_{OL}	RESET, PCLK Output LOW Voltage		0.45		0.45	V	I_{OL} = 5 mA
V_{OH}	RESET, PCLK Output HIGH Voltage	2.4		2.4		V	I_{OH} = –1 mA
V_{OLR}	$\overline{READY}$, Output LOW Voltage		0.45		0.45	V	I_{OL} = 9 mA
V_{OLC}	CLK Output LOW Voltage		0.45		0.45	V	I_{OL} = 5 mA
V_{OHC}	CLK Output HIGH Voltage	4.0		4.0		V	I_{OH} = –800μA
I_{CC}	Power Supply Current		75.0		75.0	mA	at 25 MHz Output CLK Frequency
I_{LI}	Input Leakage Current		±10.0		±10.0	μA	$0 \leqslant V_{IN} \leqslant V_{CC}$
C_I	Input Capacitance		10.0		10.0	pF	F_C = 1 MHz

AC Characteristics

(T_A = 0°C to 70°C, V_{DD} = 5V, ±10%)

AC timings are referenced to 0.8V and 2.0V points of signals as illustrated in data sheet waveforms, unless otherwise noted.

Symbol	Parameter	10 MHz		12.5 MHz		Unit	Conditions
		Min.	Max.	Min.	Max.		
1	EFI to CLK Delay		25		25	ns	at 1.5V Note 1
2	EFI LOW Time	22.5		14		ns	at 0.8V Note 1
3	EFI HIGH Time	22.5		22		ns	at 2.0V Note 1
4	CLK Period	50	500	40	500	ns	
5	CLK LOW Time	12		11		ns	at 0.6V Note 1, Note 2
6	CLK HIGH Time	16		13		ns	at 3.8V Note 1, Note 2
7	CLK Rise Time		8		8	ns	1.0V to 3.5V Note 1
8	CLK Fall Time		8		8	ns	3.5 V to 1.0V Note 1
9	Status Setup Time for Status Going Active	20		22		ns	Note 1
	Status Setup Time for Status Going Inactive	20		20			
10	Status Hold Time	1		3		ns	Note 1
11	$\overline{SRDY}$ or $\overline{SRDYEN}$ Setup Time	15		15		ns	Note 1
12	$\overline{SRDY}$ or $\overline{SRDYEN}$ Hold Time	2		2		ns	Note 1
13	$\overline{ARDY}$ or $\overline{ARDYEN}$ Setup Time	0		0		ns	Note 1, Note 3
14	$\overline{ARDY}$ or $\overline{ARDYEN}$ Hold Time	30		25		ns	Note 1, Note 3
15	$\overline{RES}$ Setup Time	20		18		ns	Note 1, Note 3
16	$\overline{RES}$ Hold Time	10		8		ns	Note 1, Note 3
17	$\overline{READY}$ Active Delay	5		5		ns	at 0.8V Note 4
18	$\overline{READY}$ Active Delay	0	24	0	18	ns	at 0.8V Note 4
19	PCLK Delay	0	35	0	23	ns	Note 5
20	RESET Delay	5	27	3	22	ns	Note 5
21	PCLK LOW Time	t4-20		t4-20		ns	Note 5, Note 6
22	PCLK HIGH Time	t4-20		t4-20		ns	Note 5, Note 6

Note 1: CLK Loading: C_L = 100pF.

Note 2: With the internal crystal oscillator using recommended crystal and capacitive loading, or with the EFI input meeting specifications t2, and t3. Use a parallel-resonant, fundamental mode crystal. The recommended crystal loading for CLK frequencies of 8-25 MHz are 25pF from pin X_1 to ground, and 15pF from pin X_2 to ground. These recommended values are ±5pF and include all stray capacitance. Decouple V_{DD} and V_{SS} as close to the UM82C284-10/-12 as possible.

Note 3: This is an asynchronous input. This specification is given for testing purposes only, to assure recognition at specific CLK edge.

Note 4: $\overline{READY}$ loading: I_{OL} = 7 mA, C_L = 150pF. In system application, use 910 ohm ±5% pullup resistor to meet 80286, 80286-6 and 80286-4 timing requirements.

Note 5: PCLK and RESET loading: C_L = 75pF.

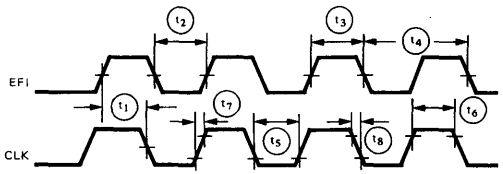
Note 6: t4 refers to any allowable CLK period.

$\overline{READY}$ loading:

CPU Frequency	10 MHz	12.5 MHz
Resistor	700 Ω	600 Ω
CL	150 pF	150 pF
I_{OL}	7 mA	9 mA

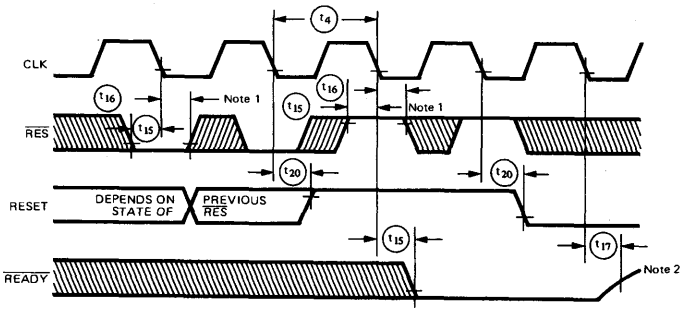
Timing Waveforms

CLK as a FUNCTION of EFI



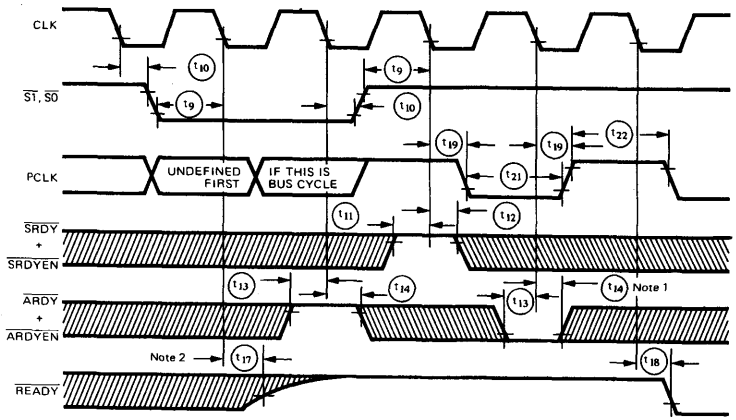
Note: The EFI input LOW and HIGH times as shown are required to guarantee the CLK LOW and HIGH times shown.

RESET and $\overline{READY}$ TIMING as a FUNCTION of $\overline{RES}$ with $\overline{S1}$ and $\overline{S0}$ HIGH



Note 1: This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.
Note 2: Tie 700 ohm ±5% pullup resistor to the $\overline{READY}$ output.

$\overline{READY}$ and PCLK Timing with $\overline{RES}$ HIGH



Note 1: This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.
Note 2: Tie 700 ohm ±5% pullup resistor to the $\overline{READY}$ output.

Ordering Information

Product	Frequency
UM82C284-10	10 MHZ
UM82C284-12	12.5 MHz

UM82C288-10/-12

Bus Controller

Features

- Provides commands and control for local and system bus.
- Offers wide flexibility in system configurations.
- Flexible command timing.
- Optional Multibus* compatible timing.
- Single +5V supply.
- 10 MHz and 12.5 MHz versions

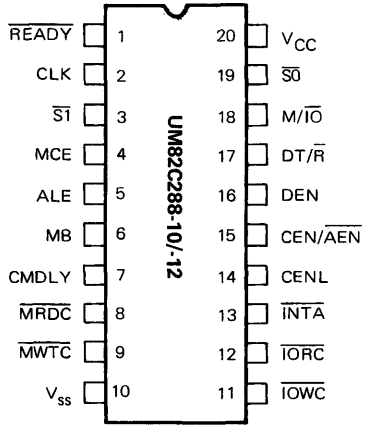
General Description

The UM82C288 Bus Controller is a 20-pin Si-Gate CMOS component for use in 80286 microsystems. The bus controller provides command and control outputs with flexible timing options. Separate command outputs are used for memory and I/O devices. The data bus is controlled with separate data enable and direction control signals.

Two modes of operation are possible via a strapping option: Multibus* compatible bus cycles, and high speed bus cycles.

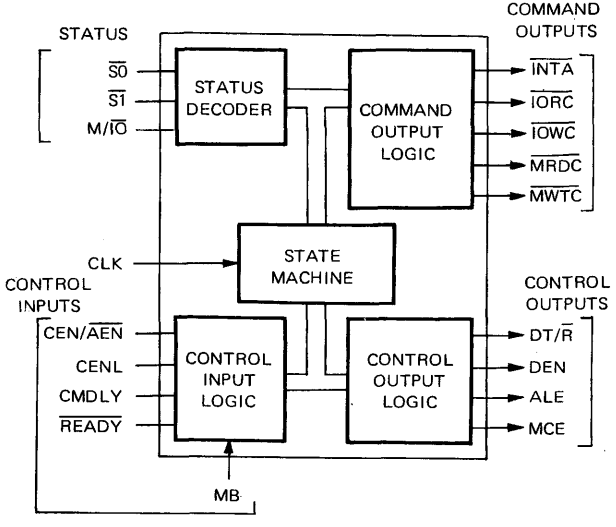
*Multibus is a patented bus of INTEL CORP.

Pin Configuration



* Multibus is an Intel Trademark

Block Diagram



Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . 0°C to 70°C

Storage Temperature . . . . . −65°C to +150°C

Voltage on Any Pin with Respect to GND . . . . . −0.5V to +7V

Power Dissipation . . . . . 1 Watt

Comments*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC Characteristics (T_A = 0°C to 70°C, V_{DD} = 5V, ±10%)

AC timings are referenced to 0.8V and 2.0V points of signals as illustrated in data sheet waveforms, unless otherwise noted.

Symbol	Parameter	10 MHz		12.5 MHz		Unit	Conditions
		Min.	Max.	Min.	Max.		
1	CLK Period	50	250	40	250	ns	
2	CLK HIGH Time	16	238	13	239	ns	at 3.8V
3	CLK LOW Time	12	234	11	237	ns	at 0.6V
4	CLK Rise Time		8		8	ns	1.0V to 3.5V
5	CLK Fall Time		8		8	ns	3.5V to 1.0V
6	M/IO and Status Setup Time	18		15		ns	
7	M/IO and Status Hold Time	1		1		ns	
8	CENL Setup Time	15		15		ns	
9	CENL Hold Time	1		1		ns	
10	READY Setup Time	26		18		ns	
11	READY Hold Time	25		20		ns	
12	CMDLY Setup Time	15		15		ns	
13	CMDLY Hold Time	1		1		ns	
14	$\overline{AEN}$ Setup Time	15		15		ns	Note 1
15	$\overline{AEN}$ Hold Time	0		0		ns	Note 1
16	ALE, MCE Active Delay from CLK	3	16	3	16	ns	Note 2
17	ALE, MCE Inactive Delay from CLK		19		19	ns	Note 2
18	DEN (Write) Inactive from CENL		23		23	ns	Note 2
19	DT/R LOW from CLK		23		23	ns	Note 2
20	DEN (Read) Active from DT/R	5	21	5	21	ns	Note 2
21	DEN (Read) Inactive Delay from CLK	3	21	3	19	ns	Note 2
22	DT/R HIGH from DEN Inactive	5	20	5	18	ns	Note 2
23	DEN (Write) Active Delay from CLK		23		23	ns	Note 2
24	DEN (Write) Inactive Delay from CLK	3	19	3	19	ns	Note 2
25	DEN Inactive from CEN		25		25	ns	Note 2

(Cont.)

DC Electrical Characteristics

(T_A = 0°C to 70°C, V_{DD} = 5V, ±10%)

Symbol	Parameter		10 MHz		12.5 MHz		Units	Conditions
			Min.	Max.	Min.	Max.		
V_{IL}	Input LOW Voltage		−0.5	.8	−0.5	.8	V	
V_{IH}	Input HIGH Voltage		2.0	V_{CC} +0.5	2.0	V_{CC} +0.5	V	
V_{ILC}	CLK Input LOW Voltage		−0.5	.6	−0.5	.6	V	
V_{IHC}	CLK Input HIGH Voltage		3.8	V_{CC} +0.5	3.5	V_{CC} +0.5	V	
V_{OL}	Output LOW Voltage	Command Output		.45		.45	V	
		Control Output		.45		.45	V	
V_{OH}	Output HIGH Voltage	Command Outputs	2.4		2.4		V	
		Control Outputs	2.4		2.4		V	
I_{IL}	Input Leakage Current (all other inputs)			±10		±10	μA	$0V \leqslant VI_{IN} \leqslant V_{DD}$
I_{LO}	Output Leakage Current			±10		±10	μA	$45V \leqslant V_{OUT} \leqslant V_{DD}$
I_{CC}	Power Supply Current			100		100	mA	
C_{CLK}	CLK Input Capacitance			12		12	pF	F_C = 1 MHz
C_I	Input Capacitance			10		10	pF	F_C = 1 MHz
C_O	Input /Output Capacitance			20		20	pF	F_C = 1 MHz

Notes: 1. Command Outputs are $\overline{INTA}$, $\overline{IORC}$, $\overline{IOWC}$, $\overline{MRDC}$, $\overline{MWRC}$,
2. Control Outputs are DT/$\overline{R}$, DEN, ALE and MCE.

AC Characteristics (Continued)

Symbol	Parameter	10 MHz		12.5 MHz		Units	Conditions
		Min.	Max.	Min.	Max.		
26	DEN Active from CEN		24		24	ns	Note 2
27	DT/$\overline{R}$ HIGH from CLK (when CEN = LOW)		25		25	ns	Note 2
28	DEN Active from $\overline{AEN}$		26		26	ns	Note 2
29	$\overline{CMD}$ Active Delay from CLK	3	21	3	21	ns	Note 3
30	$\overline{CMD}$ Inactive Delay from CLK	5	20	5	20	ns	Note 3
31	$\overline{CMD}$ Inactive from CEN		25		25	ns	Note 3
32	$\overline{CMD}$ Active from CEN		25		25	ns	Note 3
33	$\overline{CMD}$ Inactive Enable from $\overline{AEN}$		40		40	ns	Note 3
34	$\overline{CMD}$ Float Delay from $\overline{AEN}$		40		40	ns	Note 4
35	MB Setup Time	20		20		ns	Note 1
36	MB Hold Time	0		0		ns	Note 1
37	Command Inactive Enable from MB↓		40		40	ns	Note 3
38	Command Float Time from MB↑		40		40	ns	Note 4
39	DEN Inactive from MB↑		26		26	ns	Note 2
40	DEN Active from MB↓		30		30	ns	Note 2

Note: 1. $\overline{AEN}$ and MB are asynchronous inputs. This specification is for testing purposes only, to assure recognition at a specific CLK edge.
2. Control output load: CI = 150 pF.
3. Command output load: CI = 300 pF.
4. Float condition occurs when output current is less then I_{LO} in magnitude.

Pin Description

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>CLK</td><td>I</td><td>System Clock provides the basic timing control for the UM82C288-10/-12 and 80286 microsystem. Its frequency is twice the internal processor clock frequency. The falling edge of this input signal establishes when inputs are sampled and command and control outputs change.</td></tr>
<tr><td>$\overline{S0}$, $\overline{S1}$</td><td>I</td><td>Bus Cycle Status starts a bus cycle and, along with M/$\overline{IO}$, defines the type of bus cycle. These inputs are active LOW. A bus cycle is started when either $\overline{S1}$ or $\overline{S0}$ is sampled LOW at the falling edge of CLK. These inputs have pullups sufficient to hold them HIGH when nothing drives them. Setup and hold times must be met for proper operation.
<table>
<tr><th colspan="4">80286 Bus Cycle Status Definition</th></tr>
<tr><th>M/$\overline{IO}$</th><th>$\overline{S1}$</th><th>$\overline{S0}$</th><th>Type of Bus Cycle</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Interrupt acknowledge MCE O/P</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>I/O Read</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>I/O Write</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>None; idle</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Halt or shutdown</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Memory read</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Memory write</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>None; idle</td></tr>
</table></td></tr>
<tr><td>M/$\overline{IO}$</td><td>I</td><td>Memory or I/O Select determines whether the current bus cycle is in the memory space or I/O space. When LOW, the current bus cycle is in the I/O space. Setup and hold times must be met for proper operation.</td></tr>
<tr><td>MB</td><td>I</td><td>Multibus Mode Select determines timing of the command and control outputs. When HIGH, the bus controller operates with Multibus-compatible timings. When LOW, the bus controller optimizes the command and control output timing for short bus cycles. The function of the CEN/$\overline{AEN}$ input pin is selected by this signal. This input is intended to be a strapping option and not dynamically changed. This input may be connected to V_{DD} or GND.</td></tr>
<tr><td>CENL</td><td>I</td><td>Command Enable Latched is a bus controller select signal which enables the bus controller to respond to the current bus cycle being initiated. CENL is an active HIGH input latched internally at the end of each T_S cycle. CENL is used to select the appropriate bus controller for each bus cycle in a system where the CPU has more than one bus it can use. This input may be connected to V_{CC} to select this UM82C288-10/-12 for all transfers. No control inputs affect the CENL. Setup and hold times must be met for proper operation.</td></tr>
<tr><td>CMDLY</td><td>I</td><td>Command Delay allows delaying the start of a command. CMDLY is an active HIGH input. If sampled HIGH, the command output is not activiated and CMDLY is again sampled at the next CLK cycle. When sampled LOW the selected command is enabled. If READY is detected LOW before the command output is activated, the UM82C288-10/-12 will terminate the bus cycle, even if no command was issued. Setup and hold times must be satisfied for proper operation. This input may be connected to GND if no delays are required before starting a command. This input has no effect on UM82C288-10/-12 control outputs.</td></tr>
<tr><td>$\overline{READY}$</td><td>I</td><td>Ready indicates the end of the current bus cycle. $\overline{READY}$ is an active LOW input. Multibus mode requires at least one wait state to allow the command outputs to become active. $\overline{READY}$ must be LOW during reset, to force the UM82C288-10/-12 into the idle state. Setup and hold times must be met for proper operation. The 82C284 drives $\overline{READY}$ LOW during RESET.</td></tr>
</table>

(Cont.)

Pin Description (Continued)

Symbol	I/O	Description
CEN/$\overline{AEN}$	I	Command Enable/Address Enable controls the command and DEN outputs of the bus controller. CEN/$\overline{AEN}$ inputs may be asynchronous to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs. This input may be connected to V_{CC} or GND. When MB is HIGH, this pin has the $\overline{AEN}$ function. $\overline{AEN}$ is an active LOW input which indicates that the CPU has been granted use of a shared bus and the bus controller command outputs may exit 3-state OFF and become inactive (HIGH). $\overline{AEN}$ HIGH indicates that the CPU does not have control of the shared bus and forces the command outputs into 3-state OFF and DEN inactive (LOW). $\overline{AEN}$ would normally be controlled by a bus arbiter which activates $\overline{AEN}$ when that arbiter owns the bus to which the bus controller is attached. When MB is LOW this pin has the CEN function. CEN is an unlatched active HIGH input which allows the bus controller to activate its command and DEN outputs. With MB LOW, CEN LOW forces the command and DEN outputs inactive but does not tristate them.
ALE	O	Address Latch Enable controls the address latches used to hold an address stable during a bus cycle. This control output is active HIGH. ALE will not be issued for the halt bus cycle and is not affected by any of the control inputs.
MCE	O	Master Cascade Enable signals that a cascade address from a master 8259A interrupt controller may be placed onto the CPU address bus for latching by the address latches under ALE control. The CPU's address bus may then be used to broadcast the cascade address to slave interrupt controllers so only one of them will respond to the interrupt acknowledge cycle. This control output is active HIGH. MCE is only active during interrupt acknowledge cycles and is not affected by any control input. Using MCE to enable cascade address drivers requires latches which save the cascade address on the falling edge of ALE.
DEN	O	Data Enable controls when data transceivers connected to the local data bus should be enabled. DEN is an active HIGH control output. DEN is delayed for write cycles in the Multibus mode.
DT/$\overline{R}$	O	Data Transmit/Receive establishes the direction of data flow to or from the local data bus. When HIGH, this control output indicates that a write bus cycle is being performed. A LOW indicates a read bus cycle. DEN is always inactive when DT/$\overline{R}$ changes states. This output is HIGH when no bus cycle is active. DT/$\overline{R}$ is not affected by any of the control inputs.
$\overline{IOWC}$	O	I/O Write Command instructs an I/O device to read the data on the data bus. This command output is active LOW. The MB and CMDLY inputs control when this output becomes active. $\overline{READY}$ controls when it becomes inactive.
$\overline{IORC}$	O	I/O Read Command instructs an I/O device to place data onto the data bus. This command output is active LOW. The MB and CMDLY inputs control when this output becomes active. $\overline{READY}$ controls when it becomes inactive.
$\overline{MWTC}$	O	Memory Write Command instructs a memory device to read the data on the data bus. This command output is active LOW. The MB and CMDLY inputs control when this output becomes active. $\overline{READY}$ controls when it becomes inactive.
$\overline{MRDC}$	O	Memory Read Command instructs the memory device to place data onto the data bus. This command output is active LOW. The MB and CMDLY inputs control when this output becomes active. $\overline{READY}$ controls when it becomes inactive.
$\overline{INTA}$	O	Interrupt Acknowledge tells an interrupting device that its interrupt request is being acknowledged. This command output is active LOW. The MB and CMDLY inputs control when this output becomes active. $\overline{READY}$ controls when it becomes inactive.
V_{DD}		System Power. +5V power supply
V_{SS}		System Ground: 0 volts

Functional Description

Introduction

The UM82C288-10/-12 bus controller is used in 80286 systems to provide address latch control, data transceiver control, and standard level-type command outputs. The command outputs are timed and have sufficient drive capabilities for large TTL buses and meet all IEEE-796 requirements for Multibus. A special Multibus mode is provided to statisfy all address/data setup and hold time requirements. Command timing may be tailored to special needs using a CMDLY input to determine the start of a command and $\overline{\text{READY}}$ to determine the end of a command.

Connections to multiple buses is supported with a latched enable input (CENL). An address decoder can determine which, if any, bus controller should be enabled for the bus cycle. This input is latched to allow an address decoder to take full advantage of the pipelined timing on the 80286 local bus.

Buses shared by several bus controllers are supported. An $\overline{\text{AEN}}$ input prevents the bus controller from driving the shared bus command and data signals, except when enabled by an external bus arbiter such as the 82289.

Separate DEN and DT/$\overline{\text{R}}$ outputs control the data transceivers for all buses. Bus contention is eliminated by disabling DEN before changing DT/$\overline{\text{R}}$. The DEN timing allows sufficient time for tristate bus drivers to enter 3-state OFF before enabling other drivers onto the same bus.

The term CPU refers to any 80286 processor or 80286 support component which may become an 80286 local bus master and thereby drive the UM82C288-10/-12 status inputs.

Processor Cycle Definition

Any CPU which drives the local bus uses an internal clock which is one-half the frequency of the system clock (CLK) (see Figure 3). Knowledge of the phase of the local bus master's internal clock is required for proper operation of the 80286 local bus. The local bus master informs the bus controller of its internal clock phase when it asserts the status signals. Status signals are always asserted beginning in Phase 1 of the local bus master's internal clock.

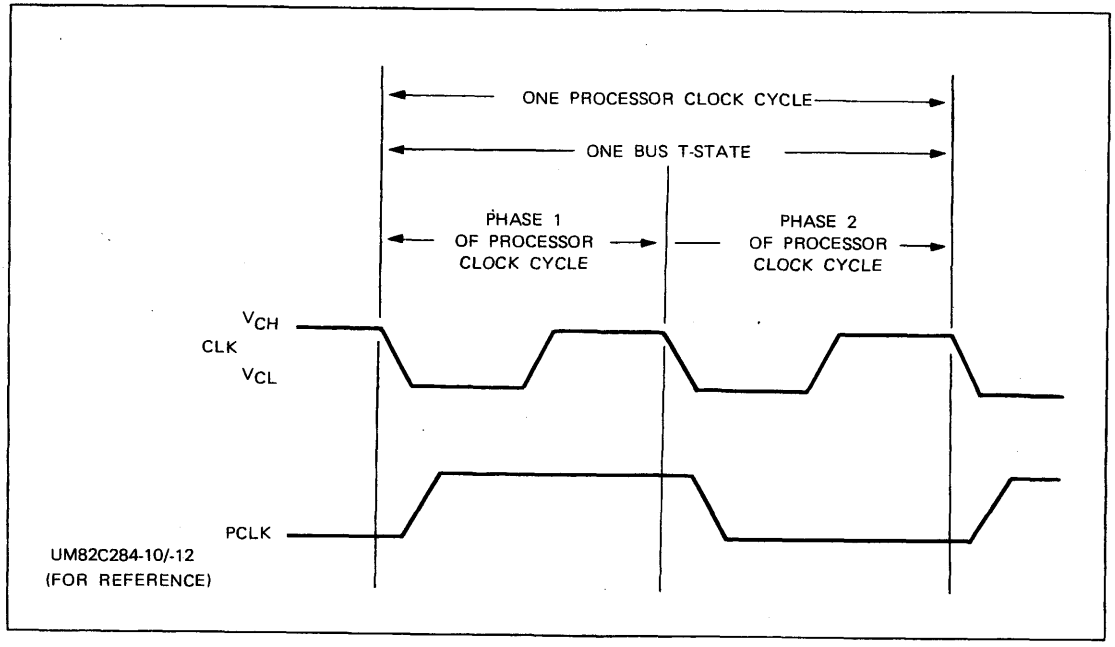


Figure 1. CLK Relationship to the Processor Clock and Bus T-States.

Bus State Definition

The UM82C288-10/-12 bus controller has three bus states (see Figure 2): Idle (T_I), Status (T_S) and Command (T_C). Each bus state is two CLK cycles long. Bus state phases correspond to the internal CPU processor clock phases.

The T_I bus state occurs when no bus cycle is currently active on the 80286 local bus. This state may be repeated indefinitely. When control of the local bus is being passed between masters, the bus remains in the T_I state.

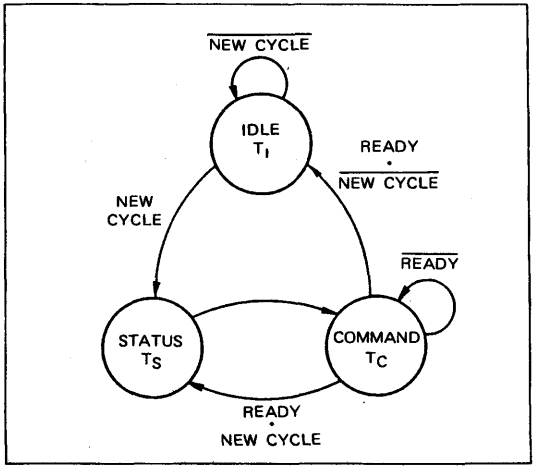


Figure 2. UM82C288-10/-12 Bus States.

Bus Cycle Definition

The $\overline{S1}$ and $\overline{S0}$ inputs signal the start of a bus cycle. When either input becomes LOW, a bus cycle is started. The T_S bus state is defined to be the two CLK cycles during which either $\overline{S1}$ or $\overline{S0}$ is active (see Figure 3). These inputs are sampled by the UM82C288-10/-12 at every falling edge of CLK. When either $\overline{S1}$ or $\overline{S0}$ are sampled LOW, the next CLK cycle is considered the second phase of the internal CPU clock cycle.

The local bus enters the T_C bus state after the T_S state. The shortest bus cycle may have one T_S state and one T_C state. Longer bus cycles are formed by repeating T_C states. A repeated T_C bus state is called a wait state.

The $\overline{READY}$ input determines whether the current T_C bus state is to be repeated. The $\overline{READY}$ input has the same timing and effect for all bus cycles. $\overline{READY}$ is sampled at the end of each T_C bus state to see if it is active. If sampled HIGH, the T_C bus state is repeated. This is called inserting a wait state. The control and command outputs do not change during wait states.

When $\overline{READY}$ is sampled LOW, the current bus cycle is terminated. Note that the bus controller may enter the T_S bus state directly from T_C if the status lines are sampled active at the next falling edge of CLK.

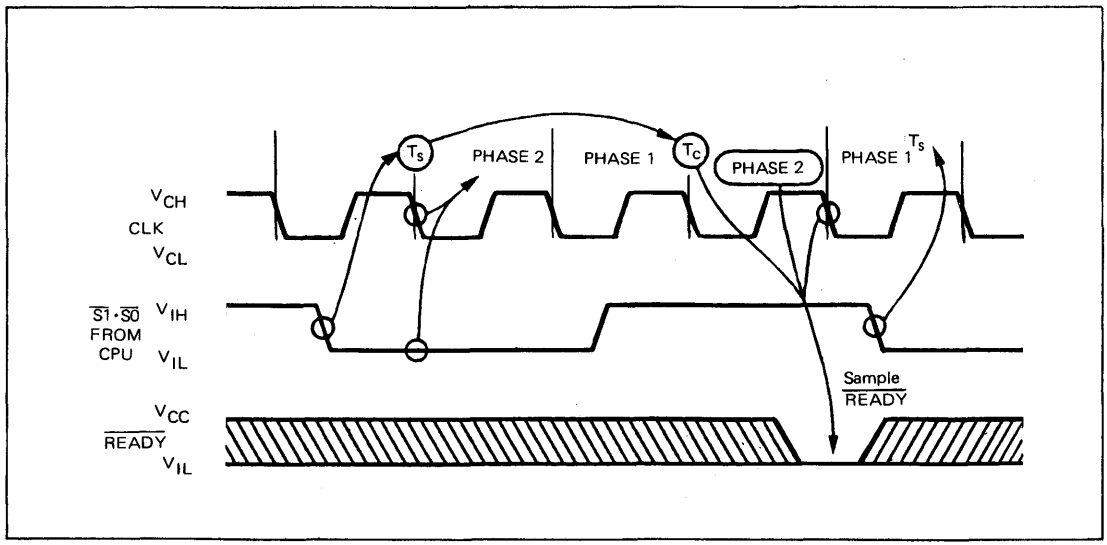


Figure 3. Bus Cycle Definition.

Table 1. Command and Control Outputs for Each Type of Bus Cycle

Type of Bus Cycle	M/IO	S1	S0	Command Activated	DT/$\overline{R}$ State	ALE, DEN Issued?	MCE Issued?
Interrupt Acknowledge	0	0	0	$\overline{INTA}$	LOW	YES	YES
I/O Read	0	0	1	$\overline{IORC}$	LOW	YES	NO
I/O Write	0	1	0	$\overline{IOWC}$	HIGH	YES	NO
None; Idle	0	1	1	None	HIGH	NO	NO
Halt/Shutdown	1	0	0	None	HIGH	NO	NO
Memory Read	1	0	1	$\overline{MRDC}$	LOW	YES	NO
Memory Write	1	1	0	$\overline{MWTC}$	HIGH	YES	NO
None; Idle	1	1	1	None	HIGH	NO	NO

Operating Modes

Two types of buses are supported by the UM82C288-10/-12: Multibus and non-Multibus. When the MB input is strapped HIGH, Multibus timing is used. In Multibus mode, the UM82C288-10/-12 delays command and data activation to meet IEEE-796 requirements on address to command active and write data to command active setup timing. Multibus mode requires at least one wait state in the bus cycle since the command outputs are delayed. The non-Multibus mode does not delay any outputs and does not require wait states. The MB input affects the timing of the command and DEN outputs.

Command and Control Outputs

The type of bus cycle performed by the local bus master is encoded in the M/$\overline{IO}$, $\overline{S1}$, and $\overline{S0}$ inputs. Different command and control outputs are activated, depending on the type of bus cycle. Table 1 indicates the cycle decode done by the UM82C288-10/-12 and the effect on command, DT/$\overline{R}$; ALE, DEN, and MCE outputs.

Bus cycles come in three forms: read, write, and halt. Read bus cycles include memory read, I/O read, and interrupt acknowledge. The timing of the associated read command outputs ($\overline{MRDC}$, $\overline{IORC}$, and $\overline{INTA}$), control outputs (ALE, DEN, DT/$\overline{R}$) and control inputs (CEN/$\overline{AEN}$, CENL, CMDLY, MB, and $\overline{READY}$) are identical for all read bus cycles. Read cycles differ only in which command output is activated. The MCE control output is only asserted during interrupt acknowledge cycles.

Write bus cycles activate different control and command outputs with different timing than read bus cycles. Memory write and I/O write are write bus cycles whose timing for command outputs ($\overline{MWTC}$ and $\overline{IOWC}$), control outputs (ALE, DEN, DT/$\overline{R}$) and control inputs (CEN/$\overline{AEN}$, CENL, CMDLY, MB, and $\overline{READY}$) are identical. They differ only in which command output is activated.

Halt bus cycles are different because no command or control output is activated. All control inputs are ignored until the next bus cycle is started via S1 and S0.

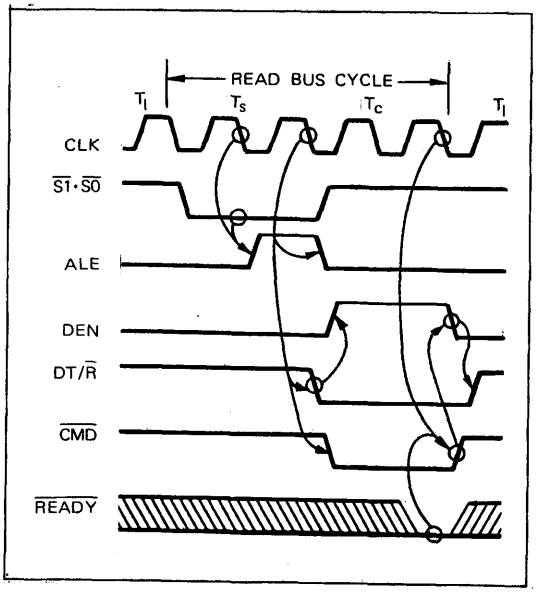


Figure 4. Idle-Read-Idle Bus Cycles with MB = "0".

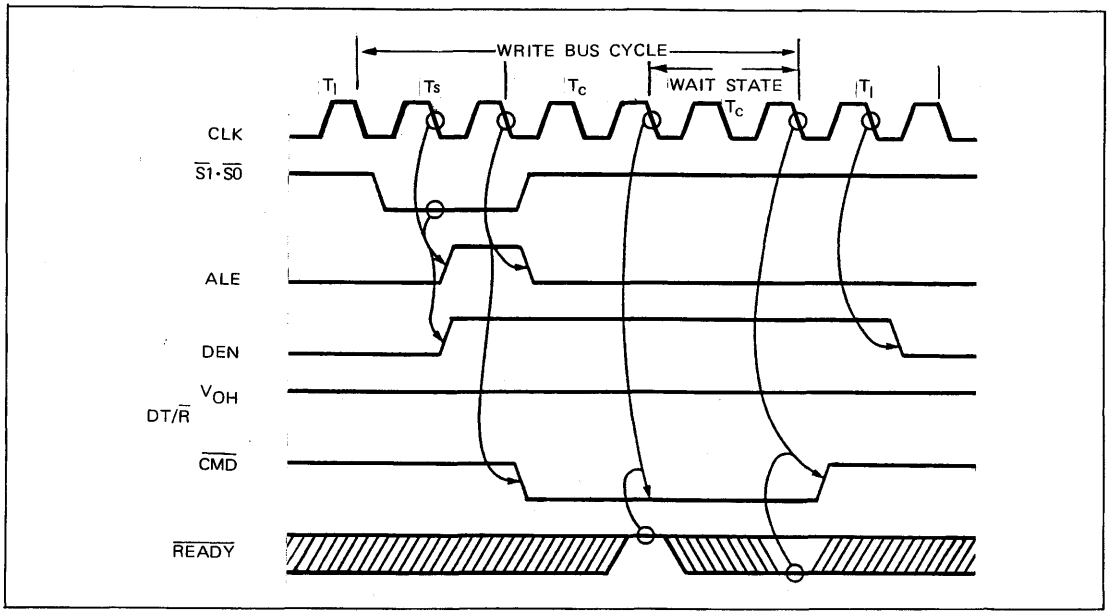


Figure 5. Idle-Write-Idle Bus Cycles with MB = "0".

Figures 4–8, show the basic command and control output timing for read and write bus cycles. Halt bus cycles are not shown since they activate no outputs. The basic idle-read-idle and idle-write-idle bus cycles are shown. The signal label CMD represents the appropriate command output for the bus cycle. For Figures 4–8, the CMDLY input is connected to V_{SS} and CENL to V_{DD}. The effects of CENL and CMDLY are described later in the section on control inputs.

Figures 4 and 6 show non-Multibus cycles. MB is connected to V_{SS} while CEN is connected to V_{DD}. Figure 4 shows a read cycle with no wait states, while Figure 5 shows a write cycle with one wait state. The $\overline{READY}$ input is shown to illustrate how wait states are added.

Bus cycles can occur back-to-back with no T_I bus states between T_C and T_S. Back-to-back cycles do not affect the timing of the command and control outputs. Command and control outputs always reach the states shown for the same clock edge (within T_S, T_C, or following bus state) of a bus cycle.

A special case in control timing occurs for back-to-back write cycles with MB = "0". In this case, DT/R and DEN remain HIGH between the bus cycles (see Figure 6). The command and ALE output timing does not change.

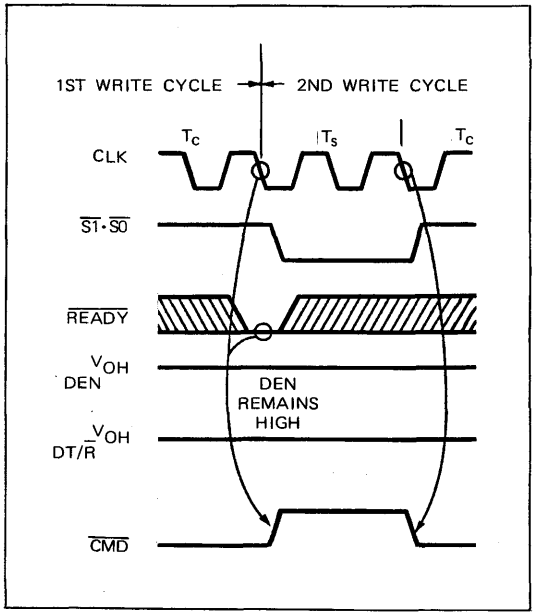


Figure 6. Write-Write Bus Cycles with MB = "0".

Figures 7 and 8 show a Multibus cycle with MB = "1". AEN and CMDLY are connected to V_{SS}. The effects of CMDLY and $\overline{AEN}$ are described later in the section

on control inputs. Figure 7 shows a read cycle with one wait state and Figure 8 shows a write cycle with two wait states. The second wait state of the write cycle is shown only for example purposes and is not required. The READY input is shown to illustrate how wait states are added.

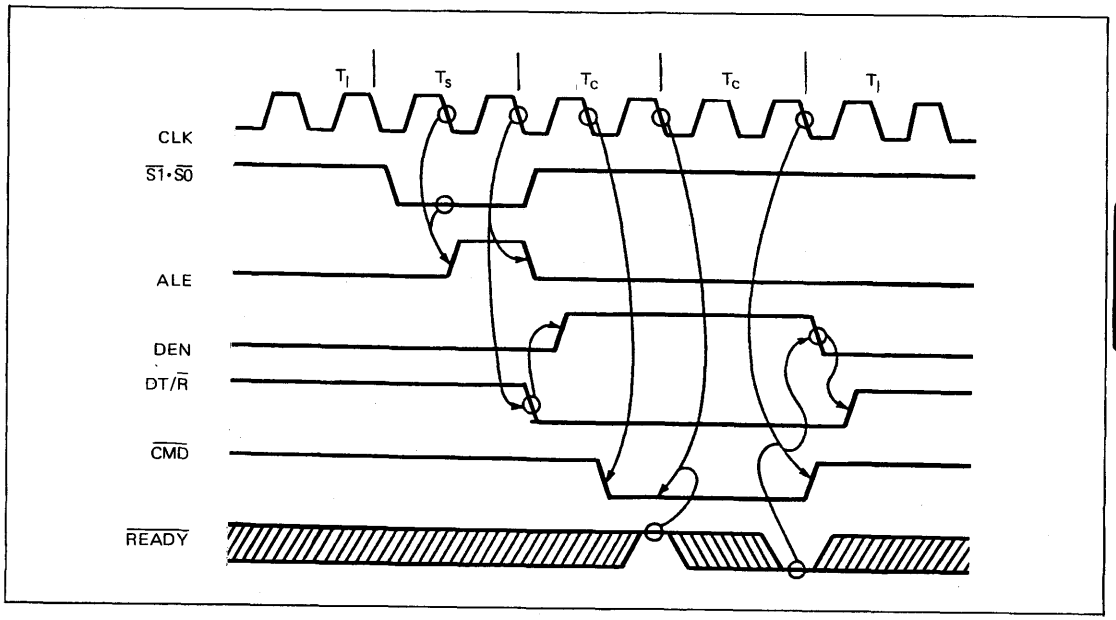


Figure 7. Idle-Read-Idle Bus Cycles with MB = "1".

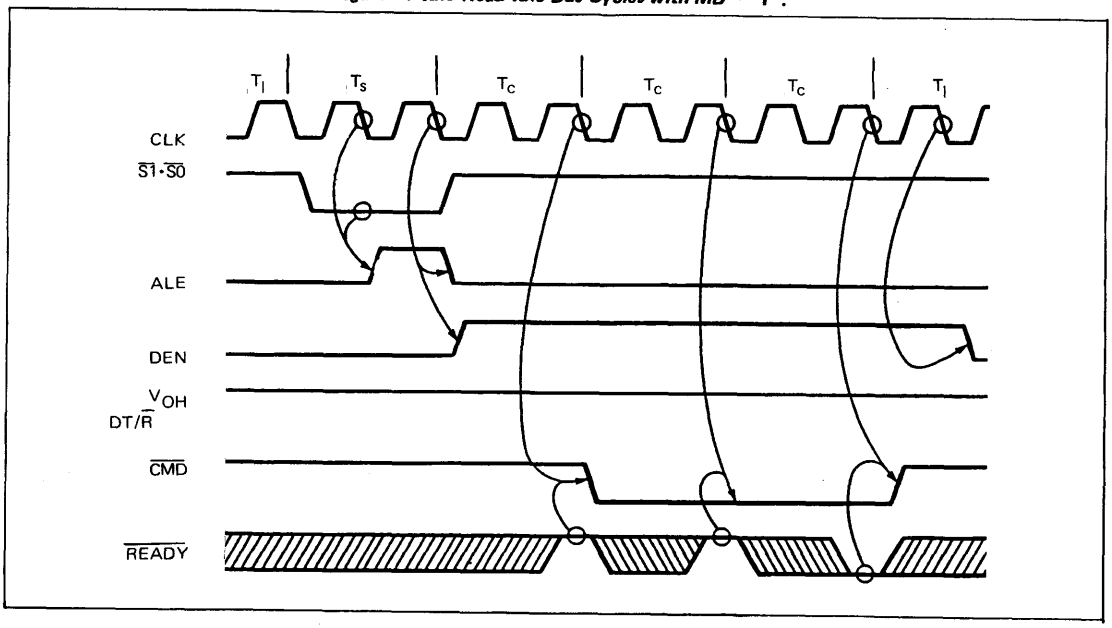


Figure 8. Idle-Write-Idle Bus Cycles with MB = "1".

The MB control input affects the timing of the command and DEN outputs. These outputs are automatically delayed in Multibus mode to satisfy three requirements:

1. 50 ns minimum setup time for valid address before any command output becomes active.
2. 50 ns minimum setup time for valid write data before any write command output becomes active.
3. 65 ns maximum time from when any read command becomes inactive until the slave's read data drivers reach 3-state OFF.

Three signal transitions are delayed by MB = "1" as compared to MB = "0".

1. The HIGH to LOW transition of the read command outputs ($\overline{IORC}$, $\overline{MRDC}$, and $\overline{INTA}$) are delayed one CLK cycle.
2. The HIGH to LOW transition of the write command outputs ($\overline{IOWC}$ and $\overline{MWTC}$) are delayed two CLK cycles.
3. The LOW to HIGH transition of DEN for write cycles is delayed one CLK cycle.

Back-to-back bus cycles with MB = "1" do not change the timing of any of the command or control outputs. DEN always becomes inactive between bus cycles with MB = "1".

Except for a halt or shutdown bus cycle, ALE will be issued during the second half of T_S for any bus cycle. ALE becomes inactive at the end of the T_S to allow latching the address to keep it stable during the entire bus cycle. The address outputs may change during Phase 2 of any T_C bus state. ALE is not affected by any control input.

Figure 9 shows how MCE is timed during interrupt acknowledge (INTA) bus cycles. MCE is one CLK cycle longer than ALE to hold the cascade address from a master 8259A valid after the falling edge of ALE. With the exception of the MCE control output, an INTA bus cycle is identical in timing to a read bus cycle. MCE is not affected by any control input.

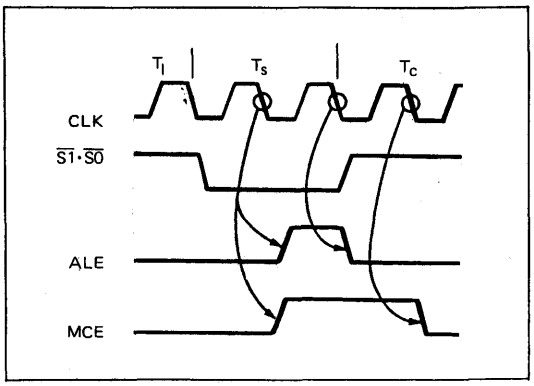


Figure 9. MCE Operation for an INTA Bus Cycle.

Control Inputs

The control inputs can alter the basic timing of command outputs, allow interfacing to multiple buses, and share a bus between different masters. For many 80286 systems, each CPU will have more than one bus which may be used to perform a bus cycle. Normally, a CPU will only have one bus controller active for each bus cycle. Some buses may be shared by more than one CPU (i.e. Multibus), requiring only one of them use the bus at a time.

Systems with multiple and shared buses use two control input signals of the UM82C288-10/-12 bus controller, CENL and $\overline{AEN}$ (see Figure 10). CENL enables the bus controller to control the current bus cycle. The $\overline{AEN}$ input prevents a bus controller from driving its command outputs. $\overline{AEN}$ HIGH means that another bus controller may be driving the shared bus.

In Figure 10, two buses are shown: a local bus and a Multibus. Only one bus is used for each CPU bus cycle. The CENL inputs of the bus controllers select which bus controller is to perform the bus cycle. An address decoder determines which bus to use for each bus cycle. The UM82C288-10/-12 connected to the shared Multibus must be selected by CENL and be given access to the Multibus by $\overline{AEN}$ before it will begin a Multibus operation.

CENL must be sampled HIGH at the end of the T_S bus state (see waveforms) to enable the bus controller to activate its command and control outputs. If sampled LOW, the commands and DEN will not go active and DT/$\overline{R}$ will remain HIGH. The bus controller will ignore the CMDLY, CEN, and $\overline{READY}$ inputs until another bus cycle is started via $\overline{S1}$ and $\overline{S0}$. Since an address decoder is commonly used to identify which bus is required for each bus cycle, CENL is latched to avoid the need for latching its input.

The CENL input can affect the DEN control output. When MB = "0", DEN normally becomes active during Phase 2 of T_S in write bus cycles. This transition occurs before CENL is sampled. If CENL is sampled LOW, the DEN output will be forced LOW during T_C as shown in the timing waveforms.

When MB = "1", CEN/$\overline{AEN}$ becomes $\overline{AEN}$. $\overline{AEN}$ controls when the bus controller command outputs enter and exit 3-state OFF. $\overline{AEN}$ is intended to be driven by a bus arbiter, like the 82289, which assures only one bus controller is driving the shared bus at any time. When $\overline{AEN}$ makes a LOW to HIGH transition, the command outputs immediately enter 3-state OFF and DEN is forced inactive. An inactive DEN should force the local data transceivers connected to the shared data bus into 3-state OFF (see Figure 10). The LOW to HIGH transition of $\overline{AEN}$ should only occur during T_I or T_S bus states.

The HIGH to LOW transition of $\overline{AEN}$ signals that the bus controller may now drive the shared bus command signals. Since a bus cycle may be active or be in the process of starting, $\overline{AEN}$ can become active during any T-state. $\overline{AEN}$ LOW immediately allows DEN to go to the appropriate state. Three CLK edges later, the command outputs will go active (see timing waveforms). The Multibus requires this delay for the address and data to be valid on the bus before the commands become active.

When MB = "0", CEN/$\overline{AEN}$ becomes CEN. CEN is an asynchronous input which immediately affects the command

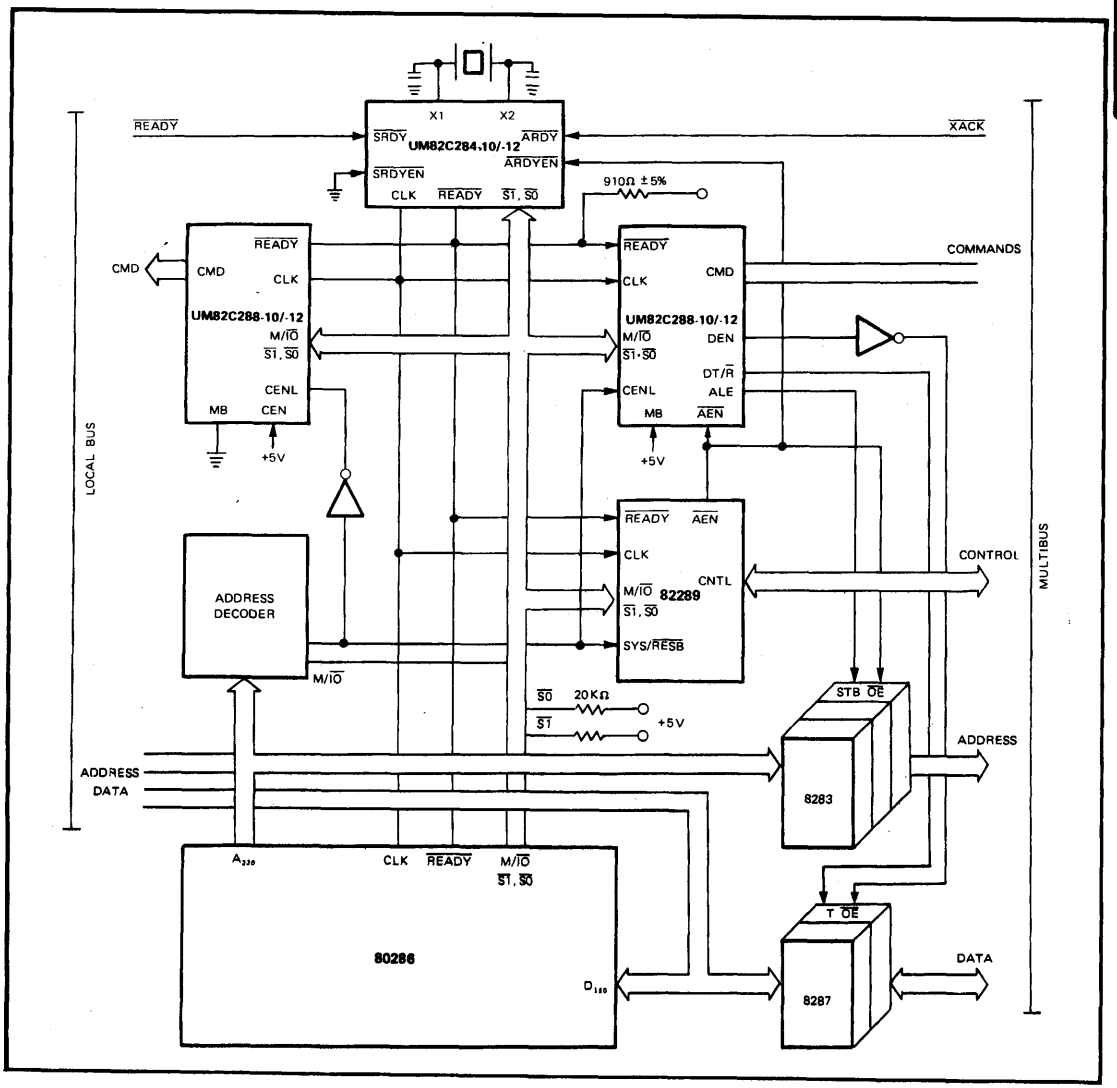


Figure 10. System Use of AEN and CENL.

and DEN outputs. When CEN makes a HIGH to LOW transition, the commands and DEN are immediately forced inactive. When CEN makes a LOW to HIGH transition, the Commands and DEN outputs immediately go to the appropriate state (see timing waveforms). $\overline{\text{READY}}$ must still become active to terminate a bus cycle if CEN remains LOW for a selected bus controller (CENL was latched HIGH).

Some memory or I/O systems may require more address or write data setup time to command active than provided by the basic command output timing. To provide flexible command timing, the CMDLY input can delay the activation of command outputs. The CMDLY input must be sampled LOW to activate the command outputs. CMDLY does not affect the control outputs ALE, MCE, DEN, and DT/$\overline{\text{R}}$.

CMDLY is first sampled on the falling edge of the CLK ending T_S. If sampled HIGH, the command output is not activated, and CMDLY is again sampled on the next falling edge of CLK. Once sampled LOW, the proper command output becomes active immediately, if MB = "0". If MB = "1", the proper command goes active no earlier than shown in Figures 7 and 8.

$\overline{\text{READY}}$ can terminate a bus cycle before CMDLY allows a command to be issued. In this case no commands are issued and the bus controller will deactivate DEN and DT/$\overline{\text{R}}$ in the same manner as if a command had been issued.

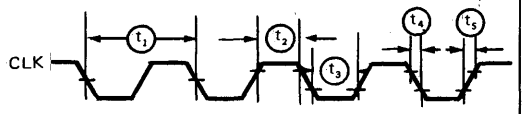
Waveform Discussion

The waveforms show the timing relationships of inputs and outputs and do not show all possible transitions of all signals in all modes. Instead, all signal timing relationships are shown via general cases. Special cases are shown when needed. The waveforms provide some functional descriptions of the UM82C288-10/-12, however, most functional descriptions are provided in Figures 3 through 9.

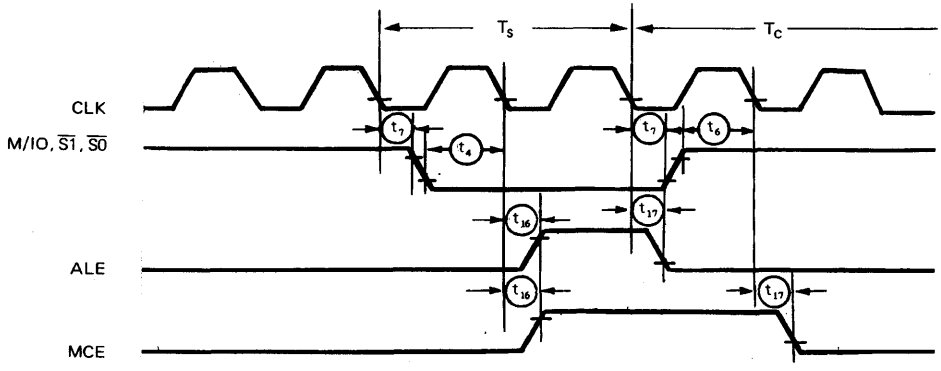
To find the timing specification for a signal transition in a particular mode, first look for a special case in the waveforms. If no special case applies, then use a timing specification for the same or related function in another mode.

Waveforms

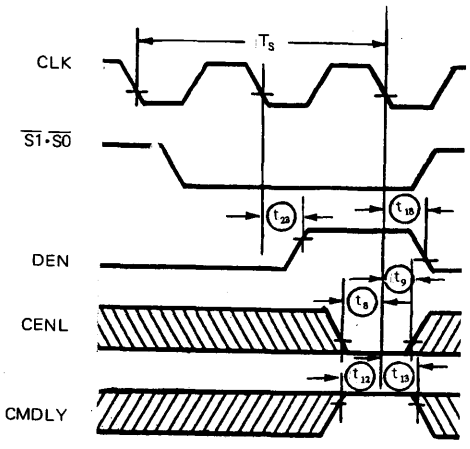
CLK CHARACTERISTICS



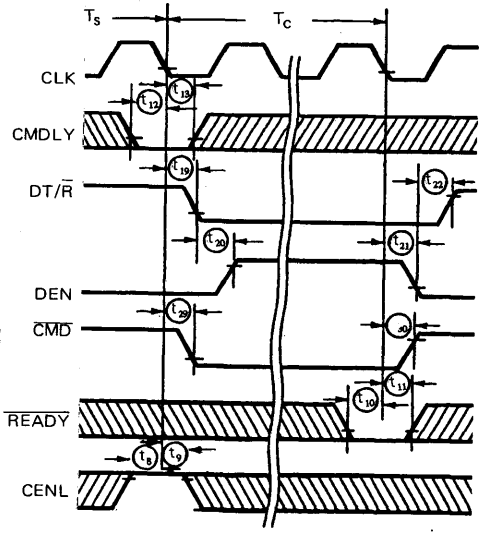
STATUS, ALE, MCE, CHARACTERISTICS



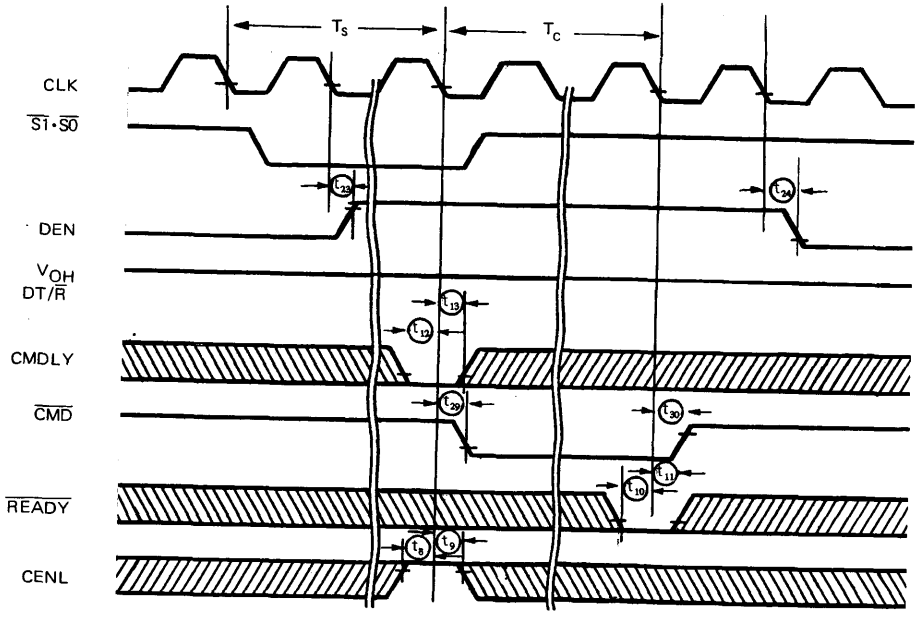
CENL, CMDLY, DEN CHARACTERISTICS WITH MB = "0" AND CEN = "1" DURING WRITE CYCLE



READ CYCLE CHARACTERISTICS WITH MB = "0" AND CEN = "1"

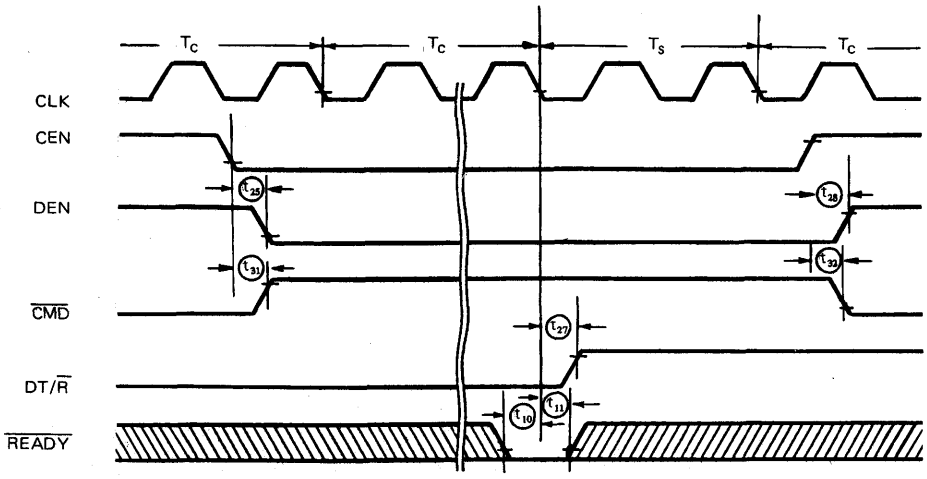


WRITE CYCLE CHARACTERISTICS WITH MB = "0" AND CEN = "1"

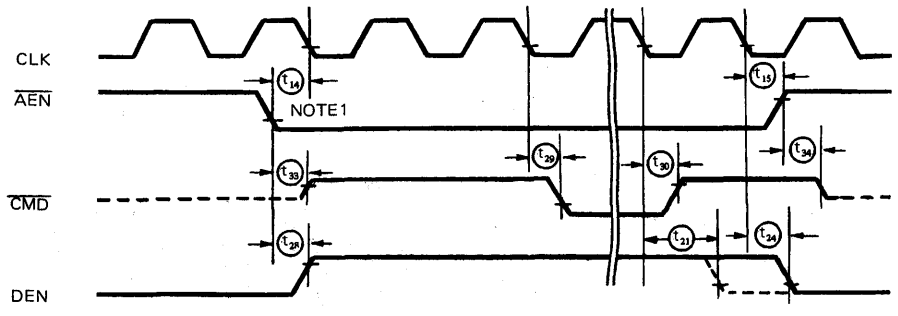


PC Mainboard

CEN CHARACTERISTICS WITH MB = "0"



AEN CHARACTERISTICS WITH MB = "1"



Note: $\overline{AEN}$ is an asynchronous input. $\overline{AEN}$ setup and hold time is specified to guarantee the response shown in the waveforms.

Ordering Information

Product	Frequency
UM82C288-10	10 MHz
UM82C288-12	12.5 MHz

UM82C54/-2

CMOS Programmable Interval Timer

Features

- Compatible with other microprocessors
- High speed, "zero wait state" operation with 8 MHz 8086/88 and 80186/188
- Three independent 16-bit counters
- Handles inputs from DC to 8 MHz – 10 MHz for UM82C54-2
- Low power CMOS – I_{CC} = 10 mA @ 8 MHz count frequency
- Completely TTL compatible
- Six programmable counter modes
- Binary or BCD counting
- Status read back command

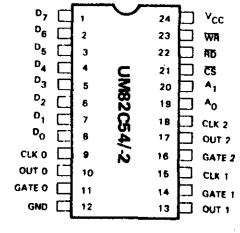
General Description

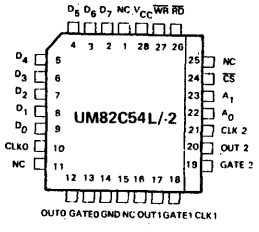
The UM82C54/-2 is a high-performance, CMOS version of the industry standard 8254 counter/timer which is designed to solve the timing control problems common in microcomputer system design. It provides three independent 16-bit counters, each capable of handling clock inputs up to 10 MHz. All modes are software programmable. The UM82C54/-2 is pin compatible with the HMOS 8254, and is a superset of the 8253.

Six programmable timer modes allow the UM82C54/-2 to be used as an event counter, elapsed time indicator, programmable one-shot, and in many other applications.

The UM82C54/-2 is available in 24-pin DIP and 28-pin plastic leaded chip carrier (PLCC) packages.

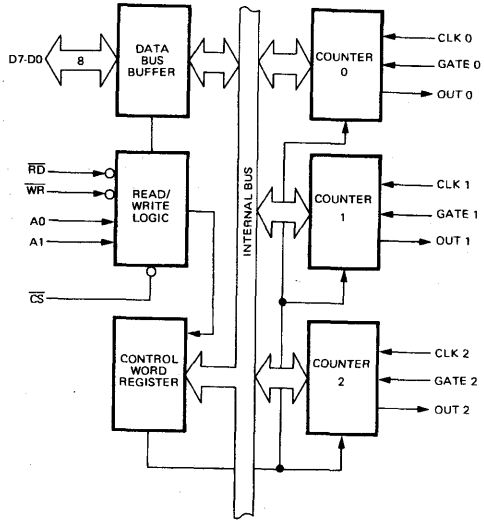
Pin Configurations





Diagrams are for pin reference only.
Package sizes are not to scale.

Block Diagram



Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . −65°C to +150°C
Supply Voltage . . . . . −0.5 to +8.0V
Operating Voltage . . . . . +4V to +7V
Voltage on any Input . . . . . GND −2V to +6.5V
Voltage on any Output . . . GND −0.5V to V_{CC} +0.5V
Power Dissipation . . . . . 1 Watt

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, GND = 0V)

Symbol	Parameter	Min.	Max.	Units	Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5V	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA
I_{IL}	Input Load Current		± 10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Float Leakage Current		± 10	μA	V_{OUT} = V_{CC} to 0.45V
I_{CC}	V_{CC} Supply Current		10	mA	CLK Freq = 8MHz 82C54 10MHz 82C54-2
I_{CCSB}	V_{CC} Supply Current-Standby		10	μA	CLK Freq = DC

Capacitance (T_A = 25°C, V_{CC} = GND = 0V)

Symbol	Parameter	Min.	Max.	Units	Conditions
C_{IN}	Input Capacitance		10	pF	f_C = 1 MHz Unmeasured pins returned to GND
$C_{I/O}$	I/O Capacitance		20	pF	
C_{OUT}	Output Capacitance		20	pF	

AC Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, GND = 0V)

BUS Parameters (Note 1)

READ CYCLE

Symbol	Parameter	UM82C54		UM82C54-2		Unit
		Min.	Max.	Min.	Max.	
t_{AR}	Address Stable Before $\overline{RD}$ ↓	45		30		ns
t_{SR}	$\overline{CS}$ Stable Before $\overline{RD}$ ↓	0		0		ns
t_{RA}	Address Hold Time After $\overline{RD}$ ↓	0		0		ns
t_{RR}	$\overline{RD}$ Pulse Width	150		95		ns
t_{RD}	Data Delay from $\overline{RD}$ ↓		120		85	ns
t_{AD}	Data Delay from Address		220		185	ns
t_{DF}	$\overline{RD}$ ↑ to Data Floating	5	90	5	65	ns
t_{RV}	Command Recovery Time	200		165		ns

Note: AC timing
1. AC timing measured at V_{OH} = 2.0V, V_{OL} = 0.8V.

AC Characteristics (Continued)

WRITE CYCLE

Symbol	Parameter	UM82C54		UM82C54-2		Unit
		Min.	Max.	Min.	Max.	
t_{AW}	Address Stable Before $\overline{WR}$ ↓	0		0		ns
t_{SW}	$\overline{CS}$ Stable Before $\overline{WR}$ ↓	0		0		ns
t_{WA}	Address Hold Time After $\overline{WR}$ ↑	0		0		ns
t_{WW}	$\overline{WR}$ Pulse Width	150		95		ns
t_{DW}	Data Setup Time Before $\overline{WR}$ ↑	120		95		ns
t_{WD}	Data Hold Time After $\overline{WR}$ ↑	0		0		ns
t_{RV}	Command Recovery Time	200		165		ns

CLOCK AND GATE

Symbol	Parameter	UM82C54		UM82C54-2		Unit
		Min.	Max.	Min.	Max.	
t_{CLK}	Clock Period	125	DC	100	DC	ns
t_{PWH}	High Pulse Width	60[3]		30[3]		ns
t_{PWL}	Low Pulse Width	60[3]		50[3]		ns
T_R	Clock Rise Time		25		25	ns
t_F	Clock Fall Time		25		25	ns
t_{GW}	Gate Width High	50		50		ns
t_{GL}	Gate Width Low	50		50		ns
t_{GS}	Gate Setup Time to CLK ↑	50		40		ns
t_{GH}	Gate Hold Time After CLK ↑	50[2]		50[2]		ns
T_{OD}	Output Delay from CLK ↓		150		100	ns
t_{ODG}	Output Delay from Gate ↓		120		100	ns
t_{WC}	CLK Delay for Loading	0	55	0	55	ns
t_{WG}	Gate Delay for Sampling	–5	50	–5	40	ns
t_{WO}	OUT Delay from Mode Write		260		240	ns
t_{CL}	CLK Set Up for Count Latch	–4	45	–40	40	ns

Notes:

2. In Modes 1 and 5 triggers are sampled on each rising clock edge. A second trigger within 120 ns (70 ns for the UM82C54/-2 of the rising clock edge may not be detected.
3. Low-going glitches that violate t_{PWH}, t_{PWL} may cause errors requiring counter reprogramming.

Pin Description

Pin Number	Symbol	I/O	Description
1-8	D_7-D_0	I/O	Data: Bi-directional three state data bus lines, connected to system data bus.
9	CLK 0	I	Clock 0: Clock input of Counter 0.
10	OUT 0	O	Output 0: Output of Counter 0.
11	GATE 0	I	Gate 0: Gate input of Counter 0.
12	GND		Ground: Power supply connection.
13	OUT 1	O	Out 1: Output of Counter 1.
14	GATE 1	I	Gate 1: Gate input of Counter 1.
15	CLK 1	I	Clock 1: Clock input of Counter 1.
16	GATE 2	I	Gate 2: Gate input of Counter 2.
17	OUT 2	O	Out 2: Output of Counter 2.
18	CLK 2	I	Clock 2: Clock input of Counter 2.
19-20	A_0, A_1	I	Address: Select inputs for one of the three counters or Control Word Register for read/write operations, Normally connected to the system address bus.
21	$\overline{CS}$	I	Chip Select: A low on this input enables the UM82C54/-2 to respond to $\overline{RD}$ and $\overline{WR}$ signals. $\overline{RD}$ and $\overline{WR}$ are ignored otherwise.
22	$\overline{RD}$	I	Read: This input is low during CPU read operations.
23	$\overline{WR}$	I	Write: This input is low during CPU write operations.
24	V_{CC}		Power: +5V power supply connection.

A1	A0	Selects
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Word Register

Functional Description

General

The UM82C54/-2 is a programmable interval timer/counter designed for use with microcomputer systems. It is a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.

The UM82C54/-2 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in software, the programmer configures the UM82C54/-2 to match his requirements and programs one of the counters for the desired delay. After the desired delay, the UM82C54/-2 will interrupt the CPU. Software overhead is minimal and variable length delays can easily be accommodated.

Some of the other computer/timer functions common to microcomputers which can be implemented with the UM82C54/-2 are:

- Real time clock
- Event counter
- Digital one-shot
- Programmable rate generator
- Square wave generator
- Binary rate multiplier
- Complex waveform generator
- Complex motor controller

Data Bus Buffer

This 3-state, bi-directional, 8-bit buffer is used to interface the UM82C54/-2 to the system bus (see Figure 1).

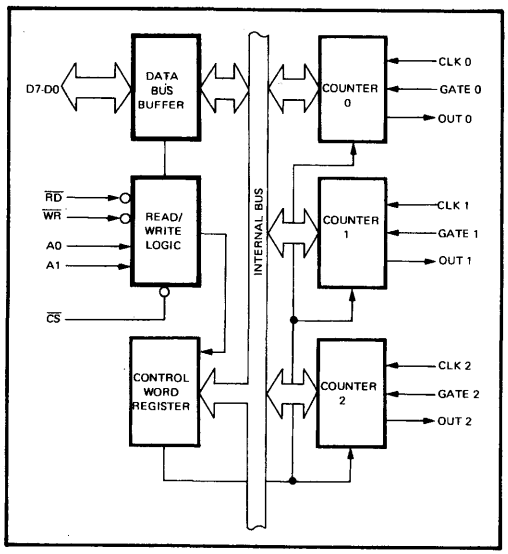


Figure 1. Data Bus Buffer and Read/Write Logic Function

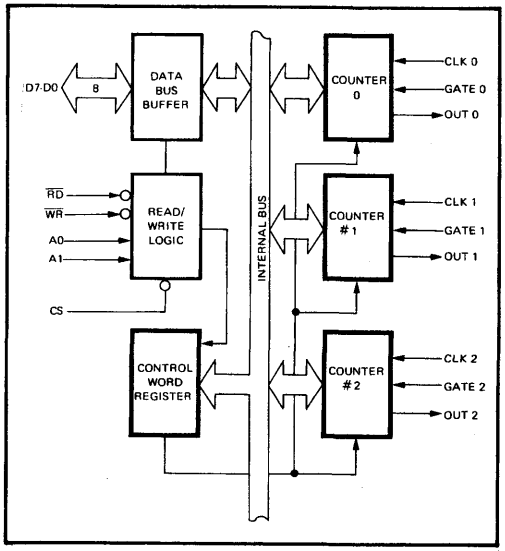


Figure 2. Control Word Register and Counter Functions

Read/Write Logic

The Read/Write Logic accepts inputs from the system bus and generates control signals for the other functional blocks of the UM82C54/-2. A_1 and A_0 select one of the three counters or the Control Word Register to be read from/written into. A "low" on the $\overline{RD}$ input tells the UM82C54/-2 that the CPU is reading one of the counters. A "low" on the $\overline{WR}$ input tells the UM82C54/-2 that the CPU is writing either a Control Word or an initial count. Both $\overline{RD}$ and $\overline{WR}$ are qualified by $\overline{CS}$; $\overline{RD}$ and $\overline{WR}$ are ignored unless the UM82C54/-2 has been selected by holding $\overline{CS}$ low.

Control Word Register

The Control Word Register (Figure 2) is selected by the Read/Write Logic when A_1, A_0 = 11. If the CPU then does a write operation to the UM82C54/-2, the data is stored in the Control Word Register and is interpreted as a Control Word used to define the Counter operation.

The Control Word Register can only be written to; status information is available with the Read-Back Command.

Counter 0, Counter 1, Counter 2

These three functional blocks are identical in operation, so only a single Counter will be described. The internal block diagram of a single counter is shown in Figure 3.

The Counters are fully independent. Each Counter may operate in a different Mode.

The Control Word Register is shown in the figure; it is not part of the Counter itself, but its contents determine how the Counter operates.

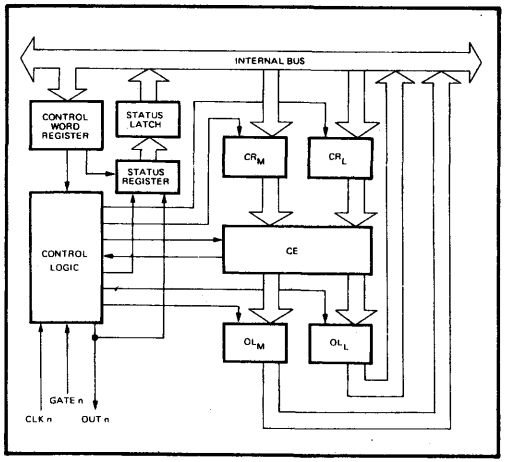


Figure 3. Counter Internal Block Diagram

The status register, when latched, contains the current contents of the Control Word Register and status of the output and null count flag. (See detailed explanation of the Read-Back command.)

The actual counter is labeled CE (for "Counting Element). It is a 16-bit presettable synchronous down counter.

OL_M and OL_L are two 8-bit latches. OL stands for "Output Latch"; the subscripts M and L for "Most significant byte" and "Least significant byte" respectively. Both are normally referred to as one unit and called just OL. These latches normally "follow" the CE, but if a suitable Counter Latch Command is sent to the UM82C54/-2, the latches "latch" the present count until read by the CPU and then return to "following" the CE. One latch at a time is enabled by the counter's Control Logic to drive the internal bus. This is how the 16-bit Counter communicated over the 8-bit internal bus. Note that the CE itself cannot be read; whenever you read the count, it is the OL that is being read.

Similarly, there are two 8-bit registers called CR_M and CR_L (for "Count Register"). Both are normally referred to as one unit and called just CR. When a new count is written to the Counter, the count is stored in the CR and later transferred to the CE. The Control Logic allows one register at a time to be loaded from the internal bus. Both bytes are transferred to the CE simultaneously. CR_M and CR_L are cleared when the Counter is programmed for one byte count (either most significant byte only or least significant byte only) the other byte will be zero. Note that the CE cannot be written into; whenever a count is written, it is written into the CR.

The Control Logic is also shown in the diagram. CLK n, GATE n, and OUT n are all connected to the outside world through the Control Logic.

UM82C54/-2 System Interface

The UM82C54/-2 is treated by the system software as an array of peripheral I/O ports; three are counters and the fourth is a control register for MODE programming.

Basically, the select inputs A_0, A_1 connect to the A_0, A_1 address bus signals of the CPU. The CS can be derived directly from the address bus using a linear select method or it can be connected to the output of a decoder.

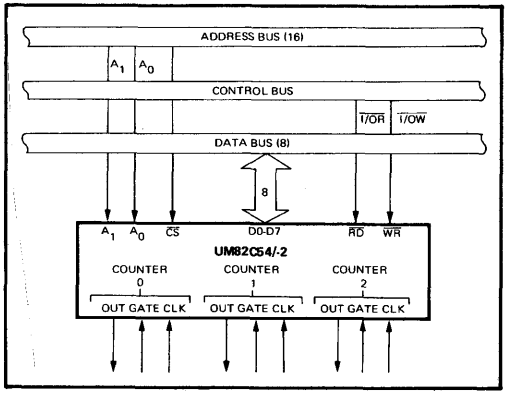


Figure 4. UM82C54/-2 System Interface

Operational Description

General

After power-up, the state of the UM82C54/-2 is undefined. The Mode, count value, and output of all Counters is undefined.

How each Counter operates is determined when it is programmed. Each Counter must be programmed before it can be used. Unused counters need not be programmed.

Programming the UM82C54/-2

Counters are programmed by writing a Control Word and then an initial count.

All Control Words are written into the Control Word Register, which is selected when A_1, A_0 = 11. The Control Word specifies which Counter is being programmed.

By contrast, initial counts are written into the Counters, not the Control Word Register. The A_1, A_0 inputs are used to select the Counter to be written. The format of the initial count is determined by the Control Word used.

Control Word Format

A_1, A_0 = 11; $\overline{CS}$ = 0; $\overline{RD}$ = 1; $\overline{WR}$ = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC – Select Counter:

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (See Read Operations)

RW – Read/Write:

RW1	RW0	
0	0	Counter Latch Command (See Read Operations)
0	1	Read/Write least significant byte only.
1	0	Read/Write most significant byte only.
1	1	Read/Write least significant byte first, then most significant byte

M – MODE:

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
x	1	0	Mode 2
x	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD:

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

Figure 5. Control Word Format

Write Operations

The programming procedure for the UM82C54/-2 is very flexible. Only two conventions need to be remembered:

1. For each Counter, the Control Word must be written before the initial count is written.

2. The initial count must follow the count format specified in the Control Word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

Since the Control Word Register and the three Counters have separate addresses (selected by the A_1, A_0 inputs), and each Control Word specifies the Counter it applies to (SC0, SC1 bits), no special instruction sequence is required. Any programming sequence that follows the conventions above is acceptable.

A new initial count may be written to a Counter at any time without affecting the Counter's programmed Mode in any way. Counting will be affected as described in the Mode definitions. The new count must follow the programmed count format.

If a Counter is programmed to read/write two-byte counts, the following precaution applies: A program must not transfer control between writing the first and second byte to another routine which also writes into that same Counter. Otherwise, the Counter will be loaded with an incorrect count.

Read Operations

It is often desirable to read the value of a Counter without disturbing the count in progress. This is easily done in the UM82C54/-2.

There are three possible methods for reading the Counters. The first is through the Read-Back command, which is explained later. The second is a simple read operation of the Counter, which is selected with the A_1, A_0 inputs. The only requirement is that the CLK input of the selected Counter must be inhibited by using either the GATE input or external logic. Otherwise, the count may be in process of changing when it is read, giving an undefined result.

	A_1	A_0
Control Word – Counter 0	1	1
LSB of count – Counter 0	0	0
MSB of count – Counter 0	0	0
Control Word – Counter 1	1	1
LSB of count – Counter 1	0	1
MSB of count – Counter 1	0	1
Control Word – Counter 2	1	1
LSB of count – Counter 2	1	0
MSB of count – Counter 2	1	0

	A_1	A_0
Control Word – Counter 2	1	1
Control Word – Counter 1	1	1
Control Word – Counter 0	1	1
LSB of count – Counter 2	1	0
MSB of count – Counter 2	1	0
LSB of count – Counter 1	0	1
MSB of count – Counter 1	0	1
LSB of count – Counter 0	0	0
MSB of count – Counter 0	0	0

	A_1	A_0
Control Word – Counter 0	1	1
Control Word – Counter 1	1	1
Control Word – Counter 2	1	1
LSB of count – Counter 2	1	0
LSB of count – Counter 1	0	1
LSB of count – Counter 0	0	0
MSB of count – Counter 0	0	0
MSB of count – Counter 1	0	1
MSB of count – Counter 2	1	0

	A_1	A_0
Control Word – Counter 1	1	1
Control Word – Counter 0	1	1
LSB of count – Counter 1	0	1
Control Word – Counter 2	1	1
LSB of count – Counter 0	0	0
MSB of count – Counter 1	0	1
LSB of count – Counter 2	1	0
MSB of count – Counter 0	0	0
MSB of count – Counter 2	1	0

Note: In all four examples, all counters are programmed to read/write two-byte counts.
These are only four of many possible programming sequences.

Figure 6. A Few Possible Programming Sequences

Counter Latch Command

The other method involves a special software command called the "Counter Latch Command". Like a Control Word, this command is written to the Control Word Register, which is selected when A_1, A_0 = 11. Also, like a Control Word, the SC0, SC1 bits select one of the three Counters, but two other bits, D_5 and D_4, distinguish this command from a Control Word.

A_1, A_0 = 11; CS = 0; RD = 1; WR = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	0	0	x	x	x	x

SC1, SC0 – specify counter to be latched

SC1	SC0	Counter
0	0	0
0	1	1
1	0	2
1	1	Read-Back Command

D_5, D_4 – 00 designates Counter Latch Command
x – don't care

Figure 7. Counter Latch Command Format

The selected Counter's output latch (OL) latches the count when the Counter Latch Command is received. This count is held in the latch until it is read by the CPU (or until the Counter is reprogrammed). The count is then unlatched automatically and the OL returns to "following" reading the contents of the Counters "on the fly" without affecting counting in progress. Multiple Counter Latch Commands may be used to latch more than one Counter. Each latched Counter's OL holds its count until read. Counter Latch Commands do not affect the programmed Mode of the Counter in any way.

If a Counter is latched and then, some time later, latched again before the count is read, the second Counter Latch Command is ignored. The count read will be the count at the time the first Counter Latch Command was issued.

With either method, the count must be read according to the programmed format; specifically, if the Counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other; read or write or programming operations of other Counters may be inserted between them.

Another feature of the UM82C54/-2 is that reads and writes of the same Counter may be interleaved; for example, if the Counter is programmed for two byte counts, the following sequence is valid.

1. Read least significant byte.
2. Write new least significant byte.
3. Read most significant byte.
4. Write new most significant byte.

If a Counter is programmed to read or write two-byte counts, the following precaution applies: A program MUST NOT transfer control between reading the first and second byte to another routine which also reads from that same Counter. Otherwise, an incorrect count will be read.

Read-Back Command

The read-back command allows the user to check the count value, programmed mode, and current state of the OUT pin and Null Count flag of the selected counter(s).

The command is written into the Control Word Register and has the format shown in Figure 8. The command applies to the counters selected by setting their corresponding bits D_3, D_2, D_1 = 1.

$A_0, A_1 = 11$ $\overline{CS} = 0$ $\overline{RD} = 1$ $\overline{WR} = 0$

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	$\overline{COUNT}$	$\overline{STATUS}$	CNT2	CNT1	CNT0	0

D_5: 0 = Latch count of selected counter(s)
D_4: 0 = Latch status of selected counter(s)
D_3: 1 = Select counter 2
D_2: 1 = Select counter 1
D_1: 1 = Select counter 0
D_0: Reserved for future expansion: Must be 0

Figure 8. Read Back Command Format

The read-back command may be used to latch multiple counter output latches (OL) by setting the COUNT bit D_5 = 0 and selecting the desired counter(s). This single command is functionally equivalent to several counter latch commands, one for each counter latches. Each counter's latched count is held until it is read (or the counter is reprogrammed). That counter is automatically unlatched when read, but other counters remain latched until they are read. If multiple count read-back commands are issued to the same counter without reading the count, all but the first are ignored; i.e., the count which will be read is the count at the time the first read-back command was issued.

The read-back command may also be used to latch status information of selected counter(s) by setting STATUS bit D_4 = 0. Status must be latched to be read; status of a counter is accessed by a read from that counter.

The counter status format is shown in Figure 9. Bits D_5 through D_0 contain the counter's programmed Mode exactly as written in the last Mode Control Word. OUTPUT bit D_7 contains the current state of the OUT pin. This allows the user to monitor the counter's output via software, possibly eliminating some hardware from a system.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
OUTPUT	NULL COUNT	RW1	RW0	M2	M1	M0	BCD

D_7 1 = Out pin is 1
0 = Out pin is 0
D_6 1 = Null count
0 = Count available for reading
D_5-D_0 = Counter programmed mode (see figure 7)

Figure 9. Status Byte

NULL COUNT bit D_6 indicates when the last count written to the counter register (CR) has been loaded into the counting element (CE). The exact time this happens depends on the Mode of the counter and is described in the Mode Definitions, but until the count is loaded into the counting element (CE), it can't be read from the counter. If the count is latched or read before this time, the count value will not reflect the new count just written. The operation of Null Count is shown in Figure 10.

This Action:	Causes:
A. Write to the control word register;[1]	Null count=1
B. Write to the count register (CR);[2]	Null count=1
C. New count is loaded into CE(CR→CE);	Null count=0

[1] Only the counter specified by the control word will have its null count set to 1. Null count bits of other counters are unaffected.

[2] If the counter is programmed for two-byte counts (least significant byte then most significant byte) null count goes to 1 when the second byte is written.

Figure 10. Null Count Operation

If multiple status latch operations of the counter(s) are performed without reading the status, all but the first are ignored; i.e., the status that will be read is the status of the counter at the time the first status read-back command was issued.

Both count and status of the selected counter(s) may be latched simultaneously by setting both COUNT and status bits D_5, D_4 = 0. This is functionally the same as issuing two separate read-back commands at once, and the above discussions apply here also. Specifically, if multiple count and/or status read-back commands are issued to the same counter(s) without any intervening reads, all but the first are ignored. This is illustrated in Figure 11.

If both count and status of a counter are latched, the first read operation of that counter will return latched status, regardless of which was latched first. The next one or two reads (depending on whether the counter is programmed for one or two type counts) return latched count. Subsequent reads return unlatched count.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	
0	1	0	0	0	Write into Counter 0
0	1	0	0	1	Write into Counter 1
0	1	0	1	0	Write into Counter 2
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read from Counter 0
0	0	1	0	1	Read from Counter 1
0	0	1	1	0	Read from Counter 2
0	0	1	1	1	No-Operation (3-State)
1	x	x	x	x	No-Operation (3-State)
0	1	1	x	x	No-Operation (3-State)

Figure 12. Read/Write Operations Summary

Mode Definitions

The following are defined for use in describing the operation of the UM82C54/-2.

CLK PULSE: a rising edge, then a falling edge, in that order, of a Counter's CLK input.

TRIGGER: a rising edge of a Counter's Gate input.

COUNTER LOADING: the transfer of a count from the CR to the CE (See "Functional Description")

Mode 0: Interrupt on Terminal Count

Mode 0 is typically used for event counting. After the Control Word is written, OUT is initially low, and will remain low until the Counter reaches zero. OUT then goes high and remains high until a new count or a new Mode 0 Control Word is written to the Counter.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

After the Control Word and initial count are written to a Counter, the initial count will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an intial count of N, OUT does not go high until N + 1 CLK pulses after the initial count is written.

If a new count is written to the Counter it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

1 – Writing the first byte disables counting. Out is set low immediately (no clock pulse required).

2 – Writing the second byte allows the new count to be loaded on next CLK pulse.

This allows the counting sequence to be synchronized by software. Again OUT does not go high until N + 1 CLK pulses after the new count of N is written.

If an initial count is written while GATE = 0, it will still be loaded on the next CLK pulse. When GATE goes high, OUT will go high N CLK pulses later; no CLK pulse is needed to load the Counter as this has already been done.

Command								Description	Result
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1	1	0	0	0	0	1	0	Read back count and status of Counter 0	Count and status latched for Counter 0
1	1	1	0	0	1	0	0	Read back status of Counter 1	Status latched for Counter 1
1	1	1	0	1	1	0	0	Read back status of Counters 2, 1	Status latched for Counter 2, but not Counter 1
1	1	0	1	1	0	0	0	Read back count of Counter 2	Count latched for Counter 2
1	1	0	0	0	1	0	0	Read back count and status of Counter 1	Count latched for Counter 1, but not status
1	1	1	0	0	0	1	0	Read back status of Counter 1	Command ignored, status already latched for Counter 1

Figure 11. Read-Back Command Example

Mode 1: Hardware Retriggerable One-Shot

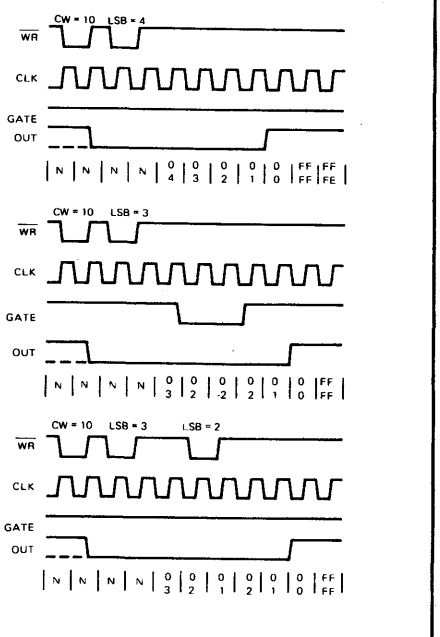
OUT will be initially high. OUT will go low on the CLK pulse following a trigger to begin the one-shot pulse, and will remain low until the Counter reaches zero. OUT will then go high and remain high until the CLK pulse after the next trigger.

After writing the Control Word and initial count, the Counter is armed. A trigger results in loading the Counter and setting OUT low on the next CLK pulse, thus starting the one-shot pulse N CLK cycles in duration. The one-shot is retriggerable, hence OUT will remain low for N CLK pulses after any trigger. The one-shot pulse can be repeated without rewriting the same count into the counter. GATE has no effect on OUT.

If a new count is written to the Counter during a one-shot pulse, the current one-shot is not affected unless the Counter is retriggered. In that case, the Counter is loaded with the new count and the one-shot pulse continues until the new count expires.

Mode 2: Rate Generator

This Mode functions like a divide-by-N counter. It is typically used to generate a Real Time Clock interrupt. OUT will initially be high. When the initial count has decremented to 1, OUT goes low for one CLK pulse. OUT then goes high again, the Counter reloads the initial count and the process is repeated. Mode 2 is periodic; the same sequence is repeated indefinitely. For an initial count of N, the sequence repeats every N CLK cycles.



Note: THE FOLLOWING CONVENTIONS APPLY TO ALL MODE TIMING DIAGRAMS.
1. COUNTERS ARE PROGRAMMED FOR BINARY (NOT BCD) COUNTING AND FOR READING/WRITING LEAST SIGNIFICANT BYTE(LSB) ONLY.
2. THE COUNTER IS ALWAYS SELECTED ($\overline{CS}$ ALWAYS LOW).
3. CW STANDS FOR "CONTROL WORD". CW=10 MEANS A CONTROL WORD OF 10 HEX IS WRITTEN TO THE COUNTER.
4. LSB STANDS FOR "LEAST SIGNIFICANT BYTE" OF COUNT.
5. NUMBERS BELOW DIAGRAMS ARE COUNT VALUES.
   THE LOWER NUMBER IS THE LEAST SIGNIFICANT BYTE.
   THE UPPER NUMBER IS THE MOST SIGNIFICANT BYTE. SINCE THE COUNTER IS PROGRAMMED TO READ/WRITE LSB ONLY, THE MOST SIGNIFICANT BYTE CANNOT BE READ.
   N STANDS FOR AN UNDEFINED COUNT.
   VERTICAL LINES SHOW TRANSITIONS BETWEEN COUNT VALUES.

Figure 13. Mode 0

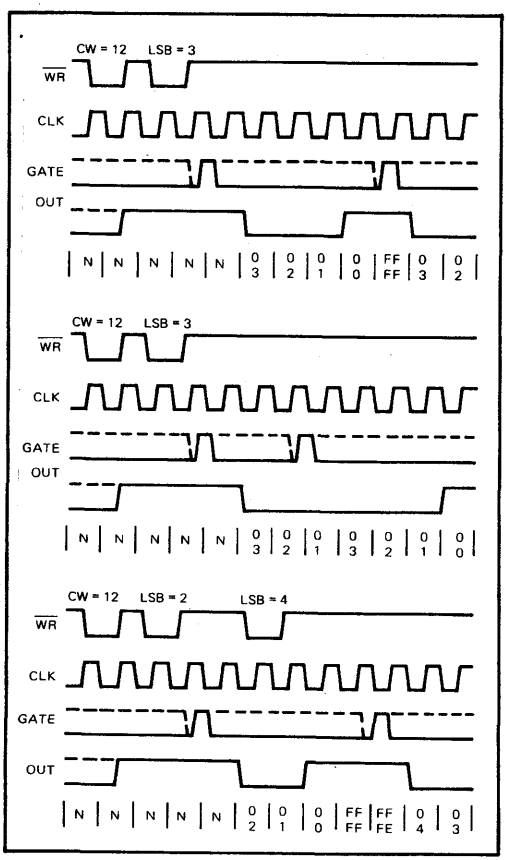
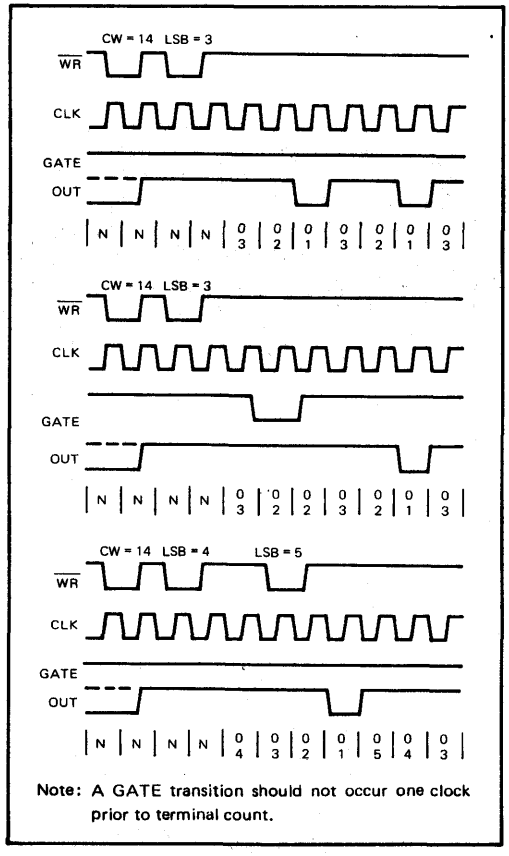


Figure 14. Mode 1

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low during an output pulse, OUT is set high immediately. A trigger reloads the Counter with the initial count on the next CLK pulse; OUT goes low N CLK pulses after the trigger. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. OUT goes low N CLK pulses after the initial count is written. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current period, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current counting cycle.



Note: A GATE transition should not occur one clock prior to terminal count.

Figure 15. Mode 2

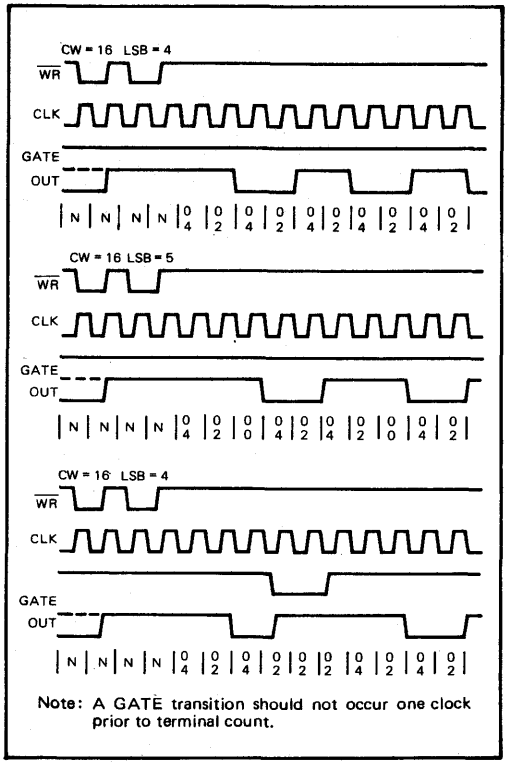
Mode 3: Square Wave Mode

Mode 3 is typically used for Baud rate generation. Mode 3 is similar to Mode 2 except for the duty cycle of OUT. OUT will initially be high. When half the inital count has expired, OUT goes low for the remainder of the count. Mode 3 is periodic; the sequence above is repeated indefinitely. An initial count of N results in a square wave with a period of N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low while OUT is low, OUT is set high immediately; no CLK pulse is required. A trigger reloads the Counter with the initial count on the next CLK pulse. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. OUT goes low N CLK pulses after the initial count is written. This allows the Counter to be synchronized by software.

Writing a new count while counting does not affect the



Note: A GATE transition should not occur one clock prior to terminal count.

Figure 16. Mode 3

current counting sequence. If a trigger is received after writing a new count but before the end of the current half-cycle of the square wave, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current half-cycle.

Mode 3 is implemented as follows:

EVEN COUNTS: OUT is initially high. The initial count is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. When the count expires OUT changes value and the Counter is reloaded with the initial count. The above process is repeated indefinitely.

ODD COUNTS: OUT is initially high. The initial count minus one (an even number) is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. One CLK pulse after the count expires, OUT goes low and the Counter is reloaded with the initial count minus one. Succeeding CLK pulses decrement the count by two. When the count expires, OUT goes high again and the Counter is reloaded with the initial count minus one. The above process is repeated indefinitely. So for odd counts, OUT will be high for (N + 1)/2 counts and low for (N – 1)/2 counts.

Mode 4: Software Triggered Mode

OUT will be initially high. When the initial count expires, OUT will go low for one CLK pulse and then go high again. The counting sequence is "Triggered" by writing the initial count.

GATE = 1 enables counting; GATE = 0 disables counting. GATE going low freezes OUT in current logic state.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after the initial count is written.

If a new count is written during counting, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

1. Writing the first byte has no effect on counting.
2. Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the sequence to be "retriggered" by software. OUT strobes low N + 1 CLK pulses after the new count of N is written.

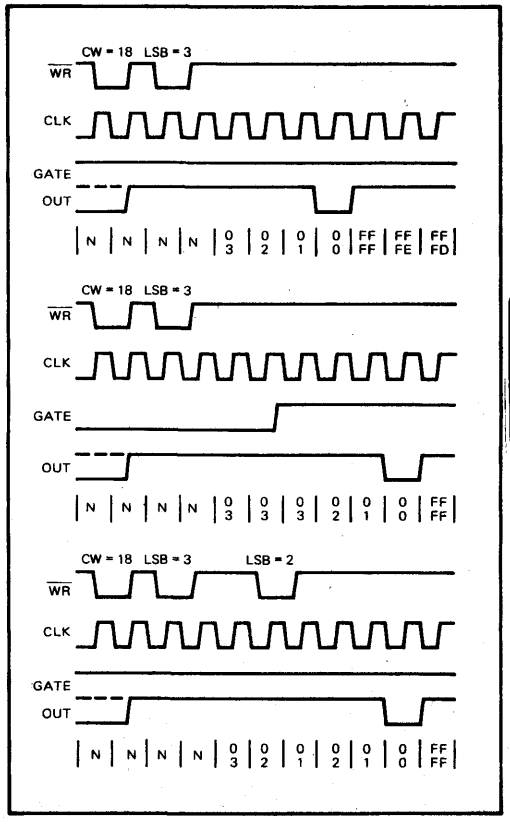


Figure 17. Mode 4

Mode 5: Hardware Triggered Strobe (Retriggerable)

OUT will initially be high. Counting is triggered by a rising edge of GATE. When the initial count has expired, OUT will go low for one CLK pulse and then go high again.

After writing the Control Word and initial count, the counter will not be loaded until the CLK pulse after a trigger. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after trigger.

A trigger results in the Counter being loaded with the initial count on the next CLK pulse. The counting sequence is triggerable. OUT will not strobe low for N + 1 CLK pulses after any trigger. GATE has no effect on OUT.

If a new count is written during counting, the current counting sequence will not be affected. If a trigger occurs after the new count is written but before the

current count expires, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from there.

Operations Common to all Modes

Programming

When a Control Word is written to a Counter, all Control Logic is immediately reset and OUT goes to a known initial state; no CLK pulses are required for this.

Gate

The GATE input is always sampled on the rising edge of CLK. In Modes 0, 2, 3, and 4 the Gate input is level sensitive, and the logic level is sampled on the rising edge of CLK. In Modes 1, 2, 3, and 5 the GATE input is rising-edge sensitive. In these Modes, a rising edge of Gate (trigger) sets an edge-sensitive flip-flop in the Counter. This flip-flop is reset immediately after it is sampled. In this way, a trigger will be detected no matter when it occurs — a high logic level does not have to be maintained until the next rising edge of CLK. Note that in Modes 2 and 3, the GATE input is both edge- and level-sensitive.

Counter

New counts are loaded and Counters are decremented on the falling edge of CLK.

The largest possible initial count is 0; this is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

The Counter does not stop when it reaches zero. In Modes 0, 1, 4, and 5 the Counter "wraps around" to the highest count, either FFFF hex for binary counting or 9999 for BCD counting, and continues counting. Modes 2 and 3 are periodic; the Counter reloads itself with the initial count and continues counting from there.

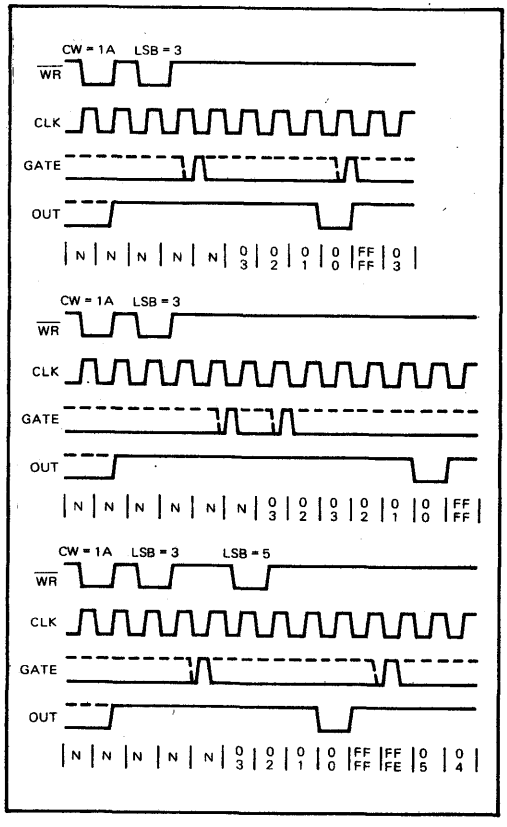


Figure 18. Mode 5

Signal Status Modes	Low or Going Low	Rising	High
0	Disable counting	–	Enables counting
1	–	1) Initiates counting 2) Resets output after next clock	–
2	1) Disable counting 2) Sets output immediately high	Initiates counting	Enables counting
3	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
4	Disables counting	–	Enables counting
5	–	Initiates counting	–

Figure 19. Gate Pin Operations Summary

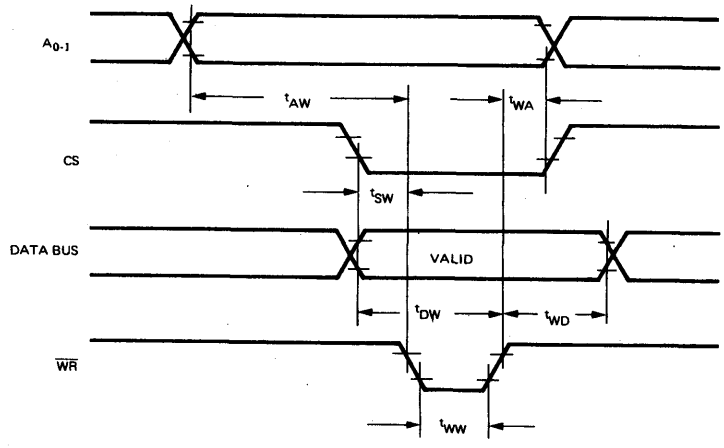
Mode	Min Count	Max Count
0	1	0
1	1	0
2	2	0
3	3	0
4	1	0
5	1	0

Note: 0 is equivalent to 2^{16} for binary counting and 10^4 for BCD counting

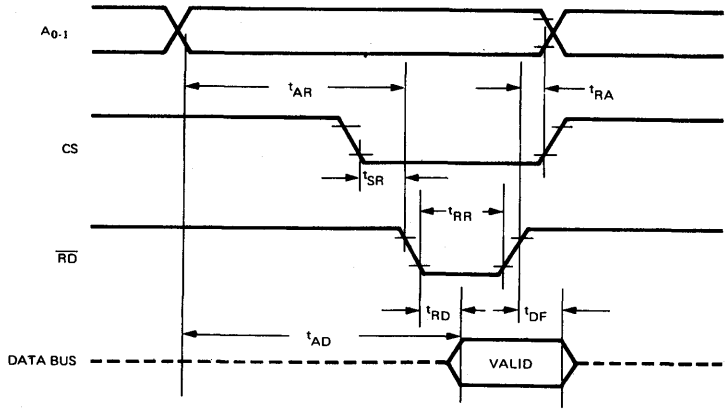
Figure 20. Minimum and Maximum Initial Counts

Timing Waveforms

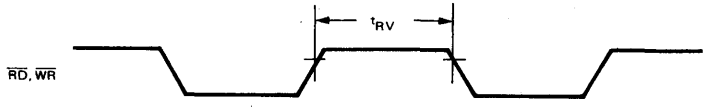
WRITE



READ

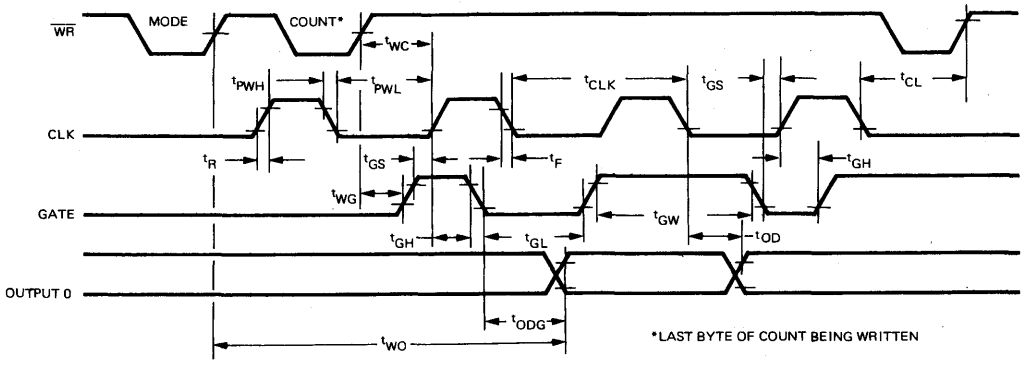


RECOVERY



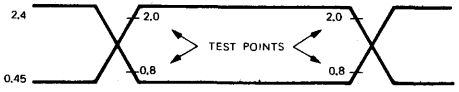
Timing Waveforms (Continued)

CLOCK AND GATE



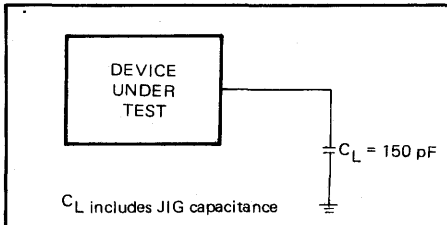
A.C. Testing Input, OUTPUT Waveform

INPUT/OUTPUT



A.C. testing: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

A.C. Testing Load Circuit



Ordering Information

Part No.	Count Frequency	Package Type
UM82C54	8 MHz	24L DIP
UM82C54-2	10 MHz	24L DIP
UM82C54L	8 MHz	28L PLCC
UM82C54L/-2	10 MHz	28L PLCC

UMC

UM82C55A

CMOS Programmable Peripheral Interface

Features

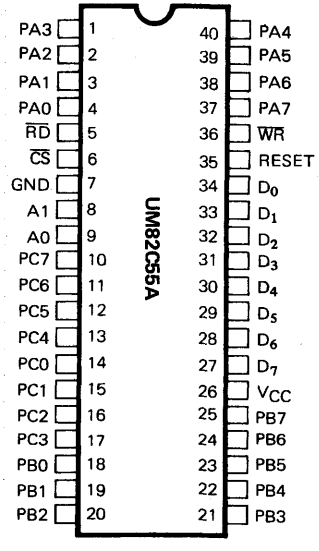
- Pin compatible with NMOS 8255A
- 24 programmable I/O pins
- Fully TTL compatible
- Bus-hold circuitry on all I/O ports eliminates pull-up resistors
- High speed, no "wait state" operation with 8MHz 80C86
- Direct bit set/reset capability
- Enhanced control word read capability
- Single 5V power supply
- 2.5mA drive capability on all I/O port outputs
- Low standby current – I_{CCSB} = 10μA

General Description

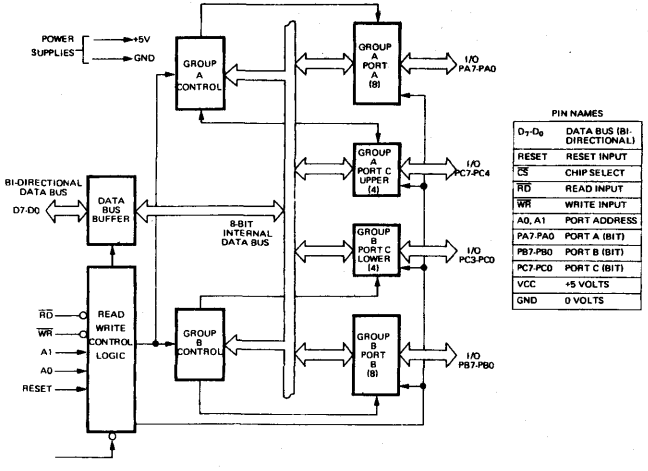
The UM82C55A is a high performance CMOS version of the industry standard 8255A and is manufactured using a self aligned silicon gate CMOS process. It is a general purpose programmable I/O device which may be used with many different microprocessors. There are 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. The high performance of the UM82C55A makes it compatible with microprocessors such as the 8086, 8048, 8051.

Static CMOS circuit design ensures low operating power. TTL compatibility of V_{IH}=2.0 volts over the industrial temperature range and bus hold circuitry eliminates the need for pull-up resistors.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Supply Voltage . . . . . +8.0 VOLTS
Operating Voltage Range . . . . . +4V to +7V
Input Voltage Applied . . . . . GND–2.0V to 6.5V
I/O Pin Voltage Applied . . . . . GND–0.5V to VCC+0.5V
Storage Temperature Range . . . . . –65°C to +150°C
Operating Temperature Range . . . . . 0°C to +70°C
Maximum Power Dissipation . . . . . 1 Watt

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(VCC = 5.0V+/–5%; T_A = 0°C to +70°C)

Symbol	Parameter	Min.	Max.	Units	Conditions
V_{IH}	Logical One Input Voltage	2.0		V	
V_{IL}	Logical Zero Input Voltage		0.8	V	
V_{OH}	Logical One Output Voltage	3.0 VCC–0.4		V V	I_{OH} = –2.5mA I_{OH} = –100 μA
V_{OL}	Logical Zero Output Voltage		0.4	V	I_{OL} = +2.5 mA
I_{IL}	Input Leakage Current	–1.0	1.0	μA	$0V \leqslant V_{IN} \leqslant V_{CC}$
I_O	I/O Pin Leakage Current	–10.0	10.0	μA	$0V \leqslant V_O \leqslant V_{CC}$
I_{BHH}	Bus Hold High Leakage Current	–50	–300	μA	V_O = 3.0V Ports A, B, C
I_{BHL}	Bus Hold Low Leakage Current	+50	+300	μA	V_O = 1.0V Port A only
I_{DAR}	Darlington Drive Current	–2.0		mA	Ports A, B, C Test Condition 3
I_{CC}	Power Supply Current		10	μA	V_{CC} = 5.5V V_{IN} = V_{CC} or G_{ND} Outputs Open

Capacitance

(T_A = 25°C; V_{CC} = GND = 0V; V_{IN} = +5V or GND)

Symbol	Parameter	Min.	Max.	Units	Conditions
C_{IN}*	Input Capacitance		5	pF	FREQ = 1 MHZ Unmeasured Pins Returned to GND
$C_{I/O}$*	I/O Pin Capacitance		20	pF	

*Guaranteed and sampled, but not 100% tested

AC Characteristics

(V_{CC} = +5V ±5%, GND = 0V; T_A = 0°C to +70°C)

READ

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{AR}	Address Stable Before READ	0		ns	
t_{RA}	Address Stable After READ	0		ns	
t_{RR}	READ Pulse Width	150		ns	
t_{RD}	Data Valid From READ		100	ns	1
t_{DF}	Data Float After READ	10	75	ns	2
t_{RV}	Time Between READs and/or WRITEs	300		ns	

WRITE

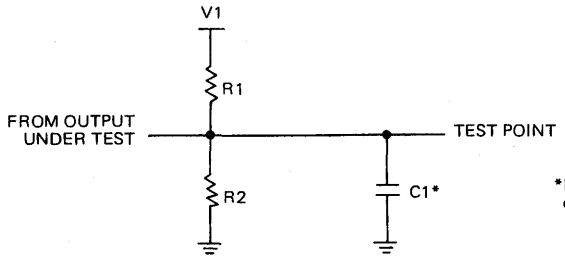
Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{AW}	Address Stable Before WRITE	0		ns	
t_{WA}	Address Stable After WRITE	20		ns	Ports A & B
		60		ns	Port C
t_{WW}	WRITE Pulse Width	100		ns	
t_{DW}	Data Valid to WRITE High	100		ns	
t_{WD}	Data Valid After WRITE High	30		ns	Ports A & B
		60		ns	Port C

OTHER TIMING

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{WB}	WR = 1 to Output		350	ns	1
t_{IR}	Peripheral Data Before RD	0		ns	
t_{HR}	Peripheral Data After RD	0		ns	
t_{AK}	ACK Pulse Width	100		ns	
t_{ST}	STB Pulse Width	100		ns	
t_{PS}	Per. Data Before STB High	20		ns	
t_{PH}	Per. Data After STB High	50		ns	
t_{AD}	ACK = 0 to Output		175	ns	1
t_{KD}	ACK = 1 to Output Float	20	250	ns	2
t_{WOB}	WR = 1 to OBF = 0		150	ns	1
t_{AOB}	ACK = 0 to OBF = 1		150	ns	1
t_{SIB}	STB = 0 to IBF = 1		150	ns	1
t_{RIB}	RD = 1 to IBF = 0		150	ns	1
t_{RIT}	RD = 0 to INTR = 0		200	ns	1
t_{SIT}	STB = 1 to INTR = 1		150	ns	1
t_{AIT}	ACK = 1 to INTR = 1		150	ns	1
t_{WIT}	WR = 0 to INTR = 0		200	ns	1
t_{RES}	Reset Pulse Width	500		ns	see note 1

Note: Period of initial Reset pulse after power-on must be at least 50usec. Subsequent Reset pulses may be 500 ns minimum.

AC Test Circuits

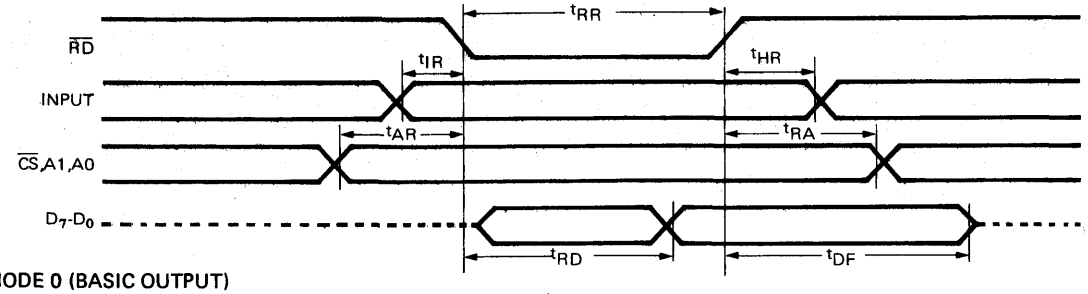


Test Condition	V1	R1	R2	C1
1	1.7V	523Ω	Open	150 pf
2	5.0V	2kΩ	1.7kΩ	50 pf
3	1.5V	750Ω	Open	Open

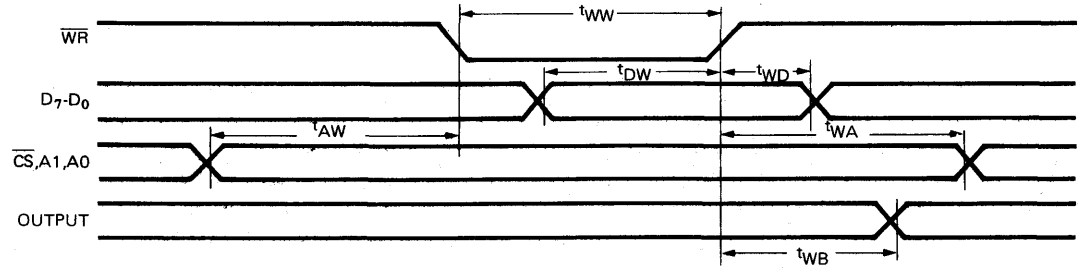
TEST CONDITION DEFINITION TABLE

Timing Waveforms

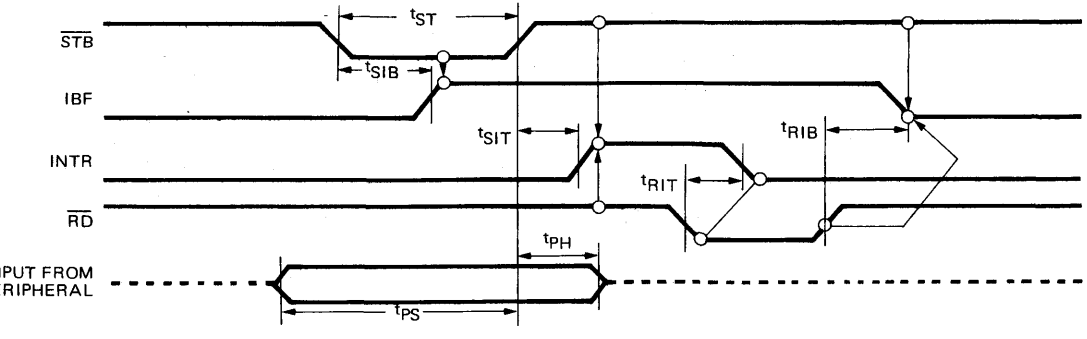
MODE 0 (BASIC INPUT)



MODE 0 (BASIC OUTPUT)

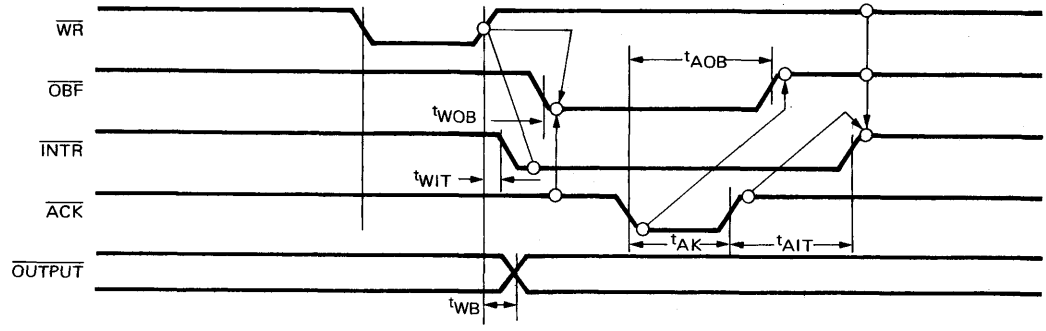


MODE 1 (STROBED INPUT)

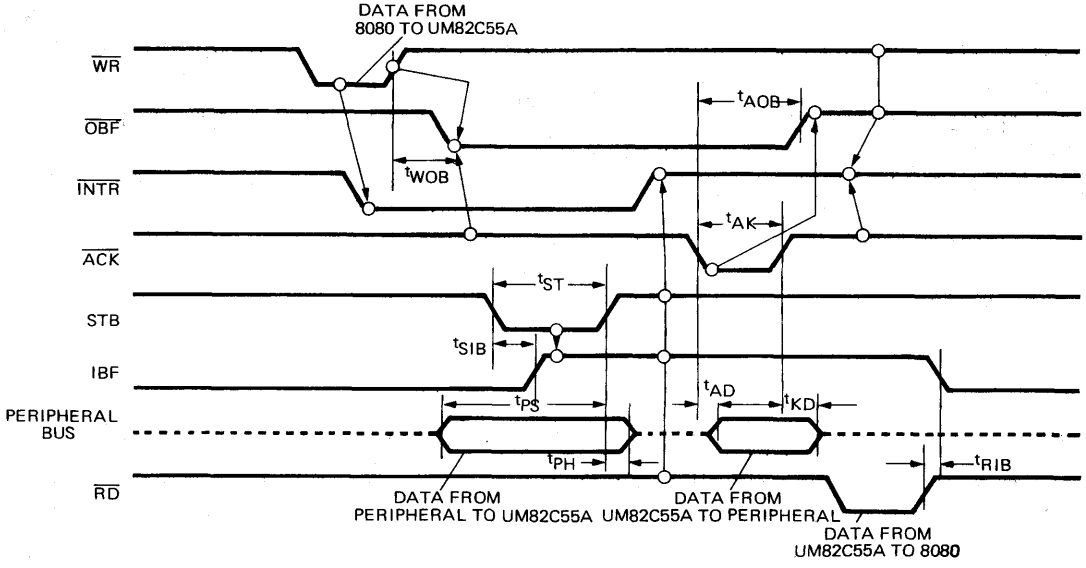


Timing Waveforms (Continued)

MODE 1 (Strobe Output)

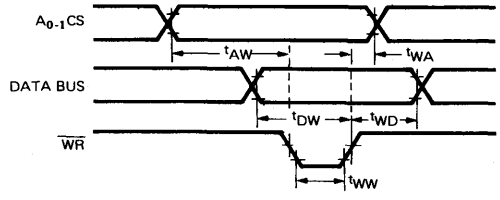


MODE 2 (BIDIRECTIONAL)

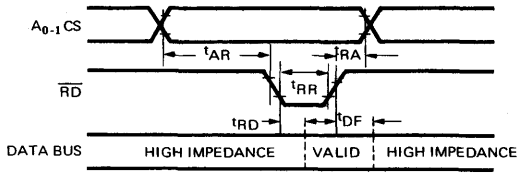


Note: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible. (INTR = IBF · $\overline{MASK}$ · $\overline{STB}$ · $\overline{RD}$ + $\overline{OBF}$ · $\overline{MASK}$ · $\overline{ACK}$ · $\overline{WR}$)

WRITE TIMING



READ TIMING



PC Mainboard

Pin Description

Data Bus Buffer
This 3-state bidirectional 8-bit buffer is used to interface the UM82C55A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic
The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control buses and in turn, issues commands to both of the Control Groups.

($\overline{CS}$)
Chip Select. A "low" on this input pin enables the communication between the UM82C55A and the CPU.

($\overline{RD}$)
Read. A "low" on this input pin enables the UM82C55A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the UM82C55A.

($\overline{WR}$)
Write. A "low" on this input pin enables the CPU to write data or control words into the UM82C55A.

(A_0 and A_1)
Port Select 0 and Port Select 1. These input signals, in conjunction with the $\overline{RD}$ and $\overline{WR}$ inputs, control the selection of one of the three ports or the control word registers. They are normally connected to the least significant bits of the address bus (A_0 and A_1).

UM82C55A BASIC OPERATION

A_0	A_1	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Input Operation (Read)
0	0	0	1	0	Port A → Data Bus
0	1	0	1	0	Port B → Data Bus
1	0	0	1	0	Port C → Data Bus
1	1	0	1	0	Control Word → Data Bus
					Output Operation (Write)
0	0	1	0	0	Data Bus → Port A
0	1	1	0	0	Data Bus → Port B
1	0	1	0	0	Data Bus → Port C
1	1	1	0	0	Data Bus → Control
					Disable Function
x	x	x	x	1	Data Bus → 3-State
x	x	1	1	0	Data Bus → 3-State

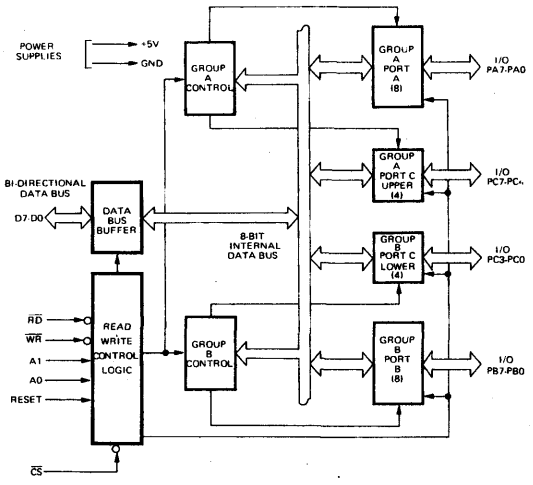


Figure 1. UM82C55A Block Diagram Data Bus Buffer and Read/Write Control Logic Functions

(Reset)
Reset. A "high" on this input clears the control register and all ports (A, B, C) are set to the input mode. "Bus hold" devices internal to the UM82C55A will hold the I/O port inputs to a logic "1" state with a maximum hold current of 300 μA.

Group A and Group B Controls
The functional configuration of each port is programmed by the system software. In essence, the CPU "outputs" a control word to the UM82C55A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the UM82C55A.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A– Port A and Port C upper (C7-C4)
Control Group B–Port B and Port C lower (C3-C0)

The control word register can be both written and read as shown in the "Basic Operation" table. Figure 4 shows the control word format for both Read and Write operations. When the control word is read, bit D7 will always be a logic "1", as this implies control word mode information.

Ports A, B and C
The UM82C55A contains three 8-bit ports (A, B, and C). All can be configured to a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the UM82C55A.

Port A One 8-bit data output latch/buffer and one 8-bit data input latch. Both "pull-up" and "pull-down" bus-hold devices are present on Port A.

Port B One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input) This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.

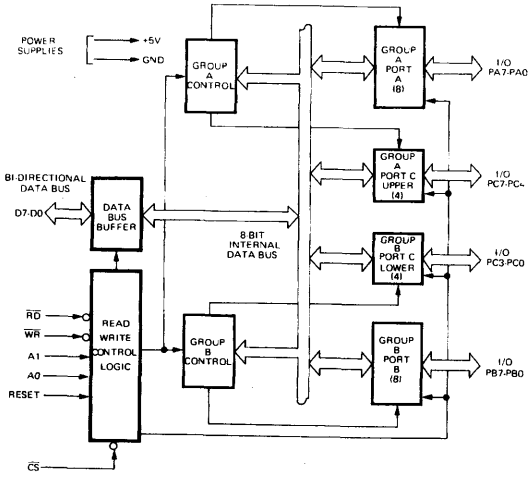


Figure 2. UM82C55A Block Diagram Showing Group A and Group B Control Functions

Operational Description

Mode Selection

There are three basic modes of operation that can be selected by the system software:

Mode 0 – Basic Input/Output
Mode 1 – Strobed Input/Output
Mode 2 – Bi-Directional Bus

When the reset input goes "high", all ports will be set to the input mode with all 24 port lines held at a logic "one" level by internal bus hold devices. After the reset is removed, the UM82C55A can remain in the input mode with no additional initialization required. This eliminates the need for pullup or pulldown resistors in all-CMOS designs. During the execution of the system program, any of the other modes may be selected using a single output instruction. This allows a single UM82C55A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance: Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

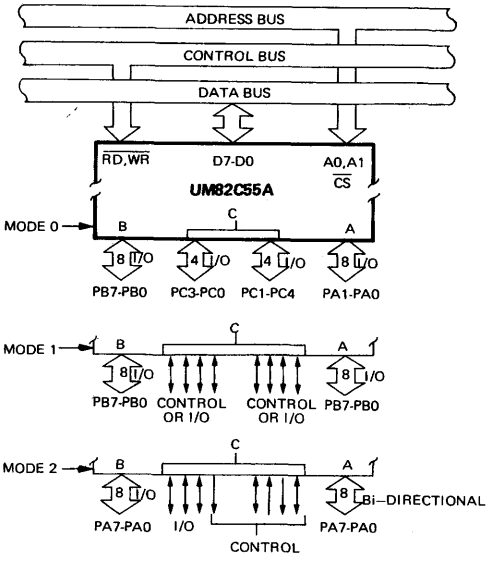


Figure 3. Basic Mode Definitions and Bus Interface

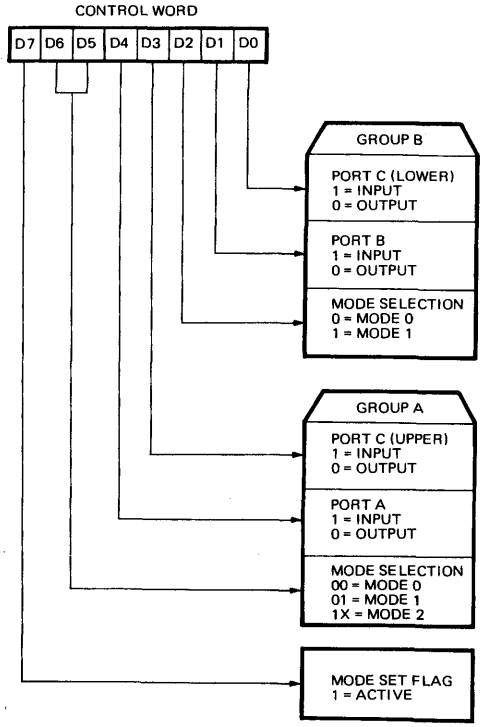


Figure 4. Mode Definition Format

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the UM82C55A has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

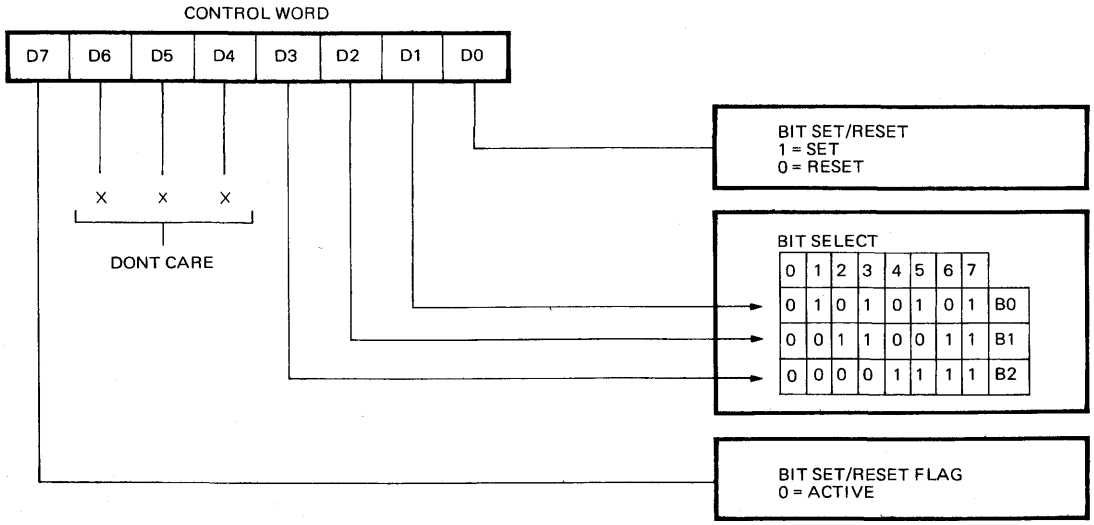


Figure 5. Bit Set/Reset Format

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUT put instruction. This feature reduces software requirements in control-based applications.

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

Interrupt Control Functions

When the UM82C55A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the programmer to enable or disable a CPU interrupt by a specific I/O device without affecting any other device in the interrupt structure.

INTE Flip-flop Definition

(BIT-SET) – INTE is SET – Interrupt enable.
(BIT–RESET) – INTE is RESET – Interrupt disable.

Note: All Mask flip-flops are automatically reset during mode selection and device Reset.

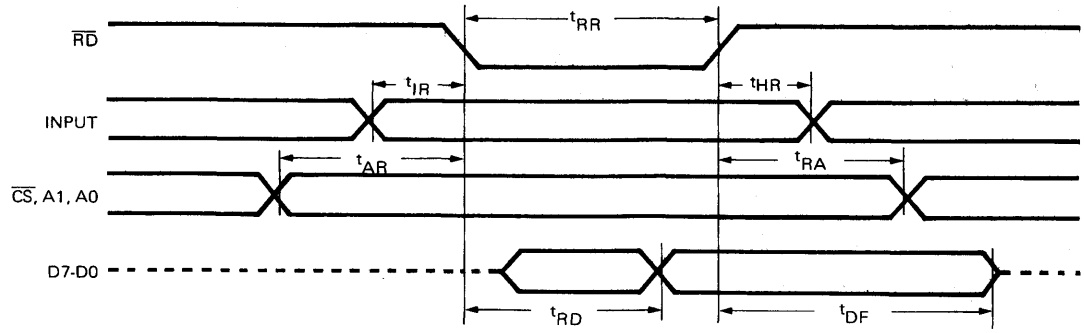
Operating Modes

Mode O (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No handshaking is required, data is simply written to or read from a specific port.

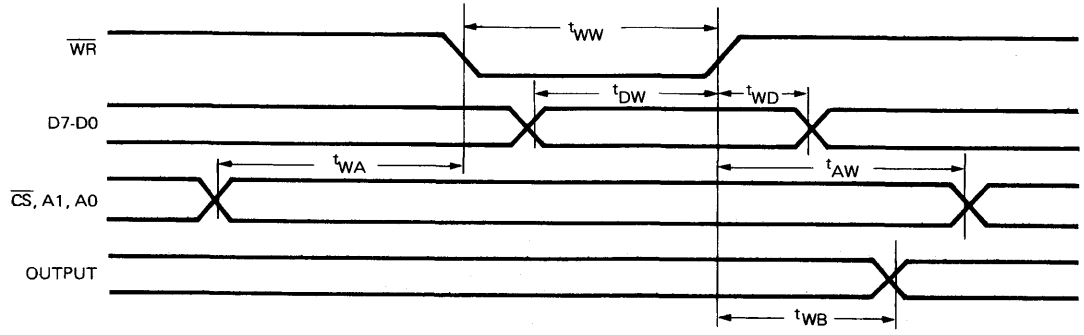
Mode O Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports
- Any port can be input or output
- Outputs are latched
- Inputs are not latched
- 16 different Input/Output configurations possible.

MODE 0 (BASIC INPUT)



MODE 0 (BASIC OUTPUT)



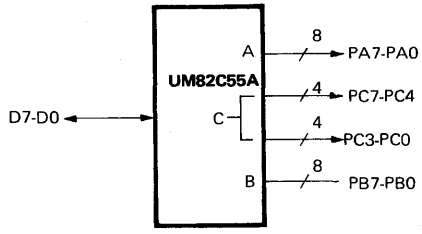
Mode 0 Port Definition

A		B		Group A			Group B	
D_4	D_3	D_1	D_0	Port A	Port C (Upper)	#	Port B	Port C (Lower)
0	0	0	0	Output	Output	0	Output	Output
0	0	0	1	Output	Output	1	Output	Input
0	0	1	0	Output	Output	2	Input	Output
0	0	1	1	Output	Output	3	Input	Input
0	1	0	0	Output	Input	4	Output	Output
0	1	0	1	Output	Input	5	Output	Input
0	1	1	0	Output	Input	6	Input	Output
0	1	1	1	Output	Input	7	Input	Input
1	0	0	0	Input	Output	8	Output	Output
1	0	0	1	Input	Output	9	Output	Input
1	0	1	0	Input	Output	10	Input	Output
1	0	1	1	Input	Output	11	Input	Input
1	1	0	0	Input	Input	12	Output	Output
1	1	0	1	Input	Input	13	Output	Input
1	1	1	0	Input	Input	14	Input	Output
1	1	1	1	Input	Input	15	Input	Input

Mode 0 Configurations

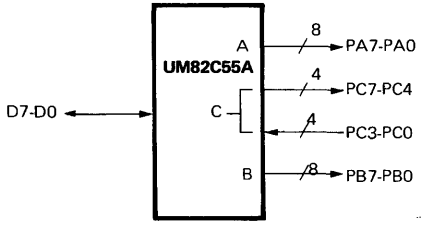
CONTROL WORD #0

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0



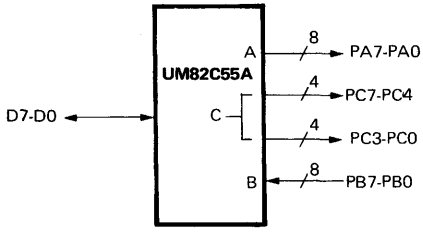
CONTROL WORD #1

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	1



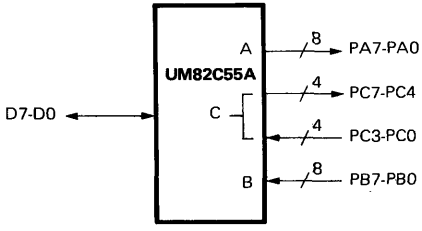
CONTROL WORD #2

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	1	0



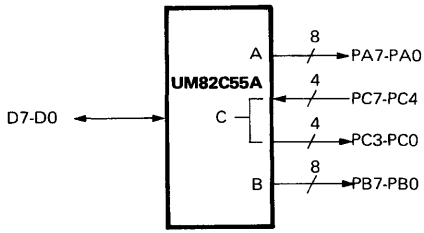
CONTROL WORD #3

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	1	1



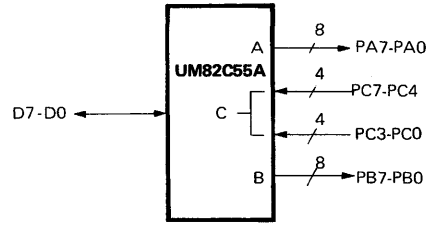
CONTROL WORD #4

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	0	0



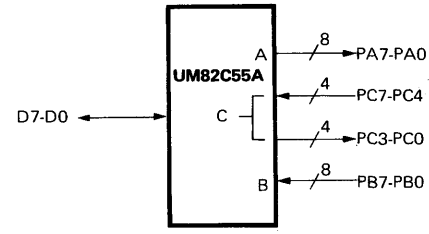
CONTROL WORD #5

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	0	1



CONTROL WORD #6

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	1	0



CONTROL WORD #7

D7	D6	D5	D4	D3	D2	D1	D0
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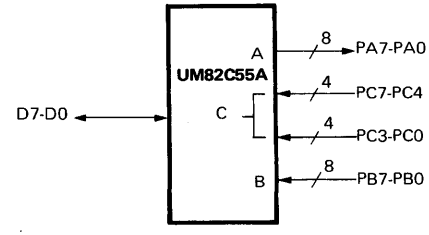
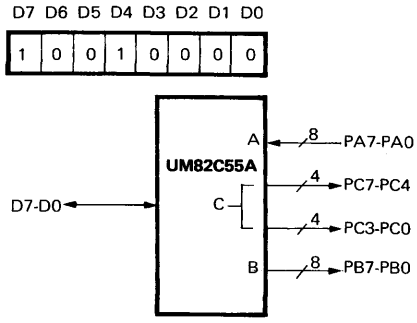
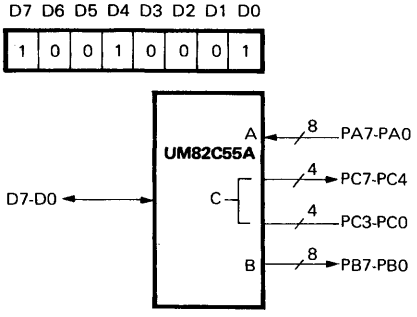


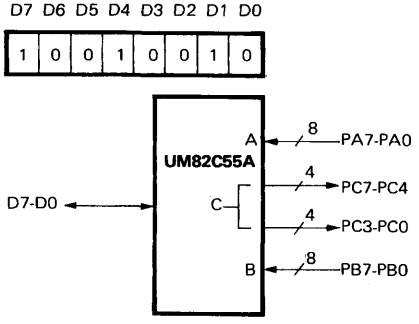
CONTROL WORD #8



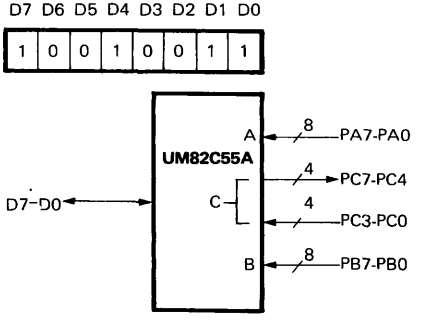
CONTROL WORD #9



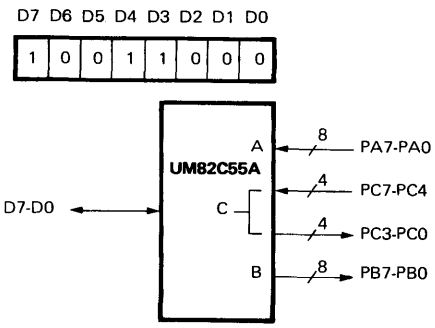
CONTROL WORD #10



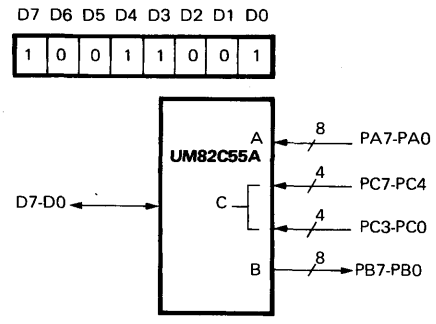
CONTROL WORD #11



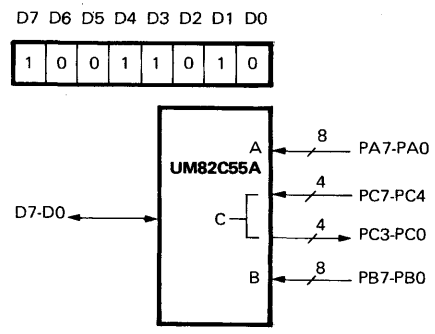
CONTROL WORD #12



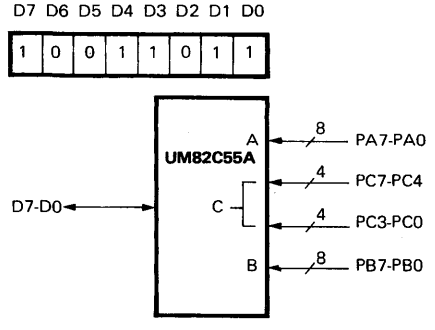
CONTROL WORD #13



CONTROL WORD #14



CONTROL WORD #15



Operating Modes

Mode 1 (Strobed Input/Output). This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In mode 1, port A and port B use the lines on port C to generate or accept these "handshaking" signals.

Mode 1 Basic Functional Definitions

- Two Groups (Group A and Group B)
- Each group contains one 8-bit port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit port.

Input Control Signal Definition

$\overline{STB}$ (Strobe Input)
A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. IBF is set by $\overline{STB}$ input being low and is reset by the rising edge of the $\overline{RD}$ input.

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the condition; STB is a "one", IBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

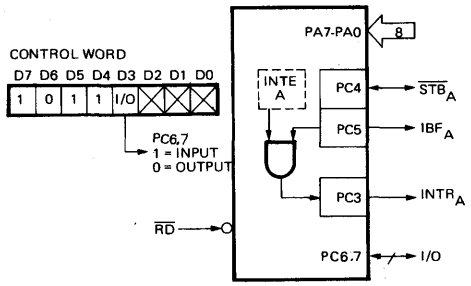
INTE A

Controlled by bit set/reset of PC_4.

INTE B

Controlled by bit set/reset of PC_2.

MODE 1 (PORT A)



MODE 1 (PORT B)

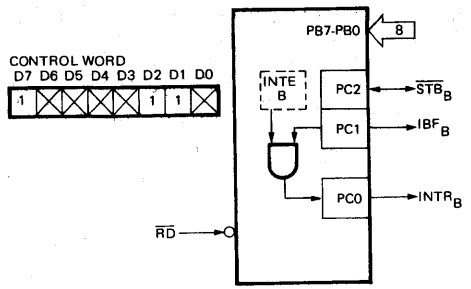


Figure 6. MODE 1 Input

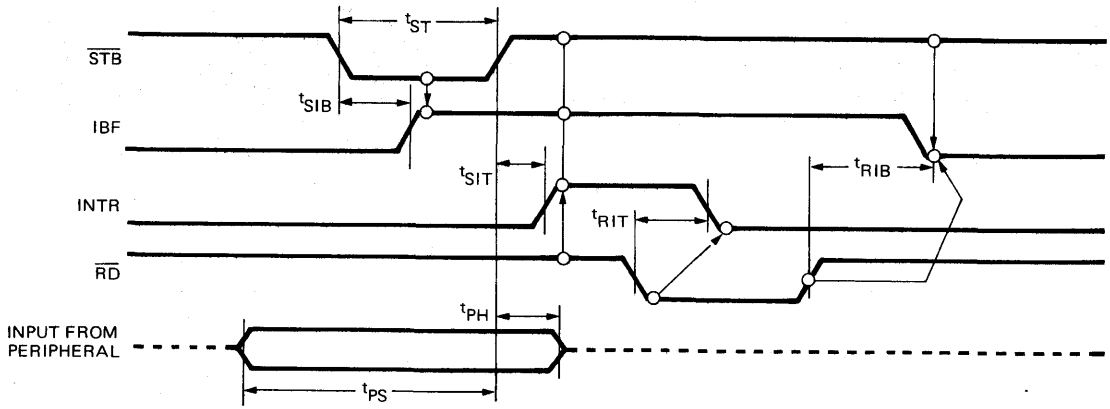


Figure 7. MODE 1 (Strobed Input)

Output Control Signal Definition

$\overline{OBF}$ (Output Buffer Full F/F). The OBF output will go "low" to indicate that the CPU has written data out to the specified port. The $\overline{OBF}$ F/F will be set by the rising edge of the $\overline{WR}$ input and reset by $\overline{ACK}$ Input being low.

$\overline{ACK}$ (Acknowledge Input). A "low" on this input informs the UM82C55A that the data from port A or port B has been accepted. In essence, a response from the peripheral device indicating that it has received the data output by the $\overline{CPU}$.

INTR (Interrupt Request). A "high" on this output can be used to interrupt the $\overline{CPU}$ when an output device has accepted data transmitted by the CPU. INTR is set when $\overline{ACK}$ is a "one", OBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{WR}$.

INTE A

Controlled by Bit Set/Reset of PC_6.

INTE B

Controlled by Bit Set/Reset of PC_2.

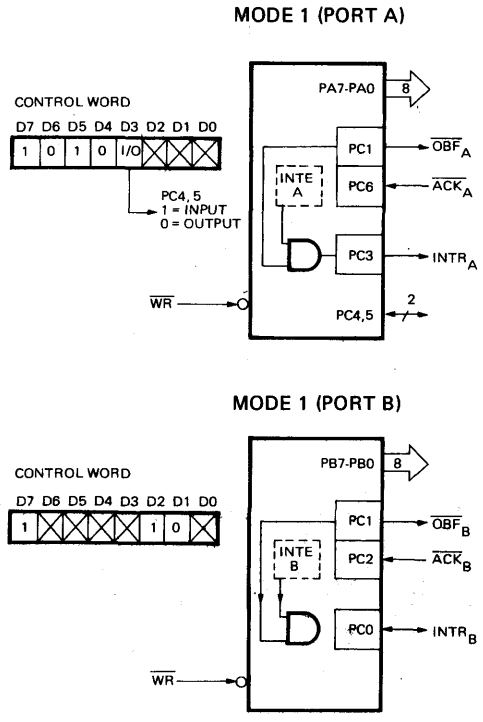


Figure 8. MODE 1 Output

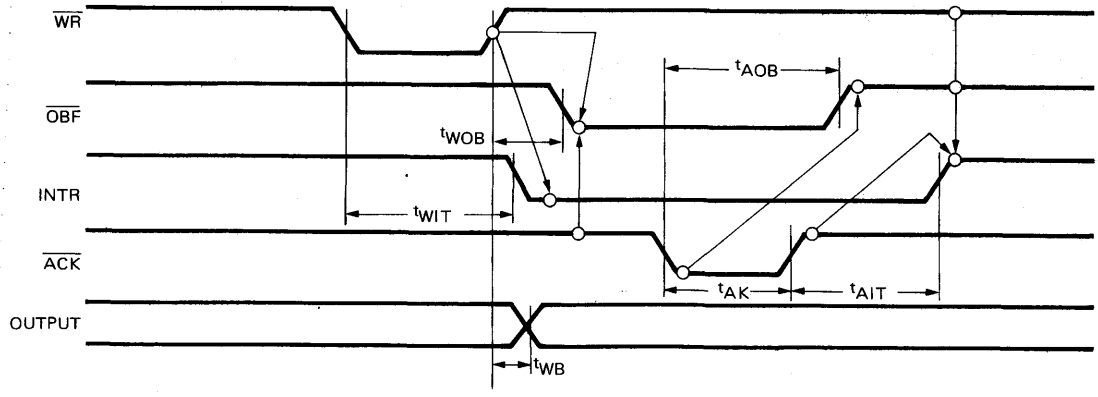


Figure 9. MODE 1 (Strobed Output)

Combinations of MODE 1; Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications:

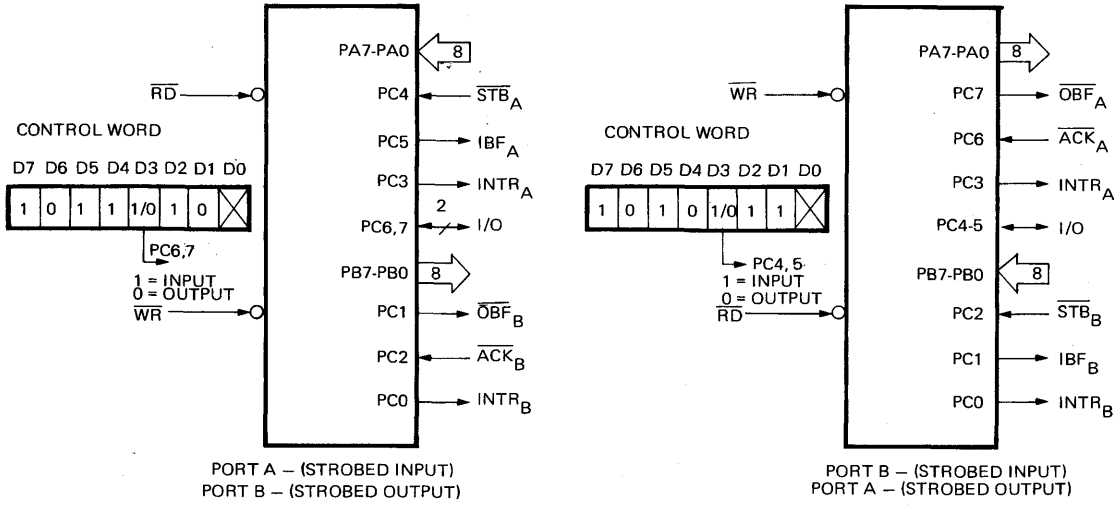


Figure 10. Combinations of MODE 1

Operating Modes

MODE 2 (Strobed Bidirectional Bus I/O)

The functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline similar to MODE 1. Interrupt generation and enable/disable functions are also available.

MODE 2 Basic Function Definitions:

- Used in Group A only.
- One 8-bit, bi-directional bus Port (Port A) and a 5-bit control Port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A).

Bidirectional Bus I/O Control Signal Definition

INTR (Interrupt Request). A high on this output can be used to interrupt the CPU for both input or output operations.

Output Operations

$\overline{OBF}$ (Output Buffer Full). The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to port A.

$\overline{ACK}$ (Acknowledge). A "Low" on this input enables the tri-state output buffer of port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 (The INTE Flip-Flop Associated with $\overline{OBF}$). Controlled by bit set/reset of PC_6.

Input Operations

$\overline{STB}$ (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F). A "high" on this output indicates that data has been loaded into the input latch.

INTE 2 (The INTE Flip-Flop Associated with IBF). Controlled by bit set/reset of PC_4.

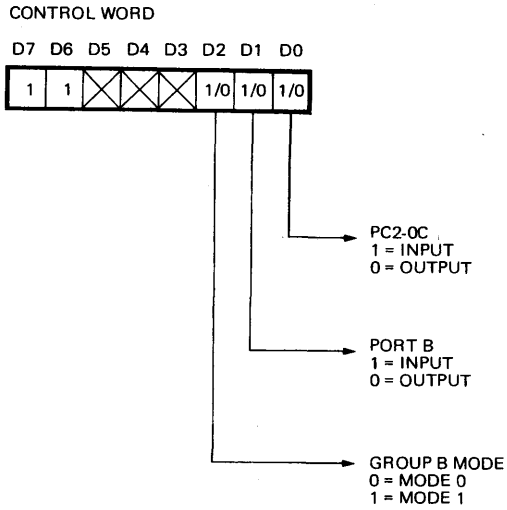


Figure 11. MODE Control Word

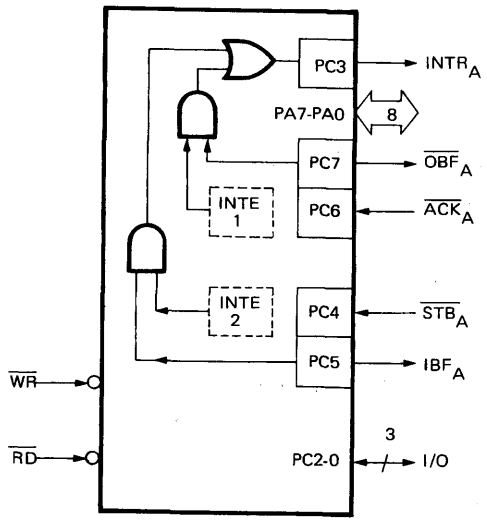


Figure 12. MODE 2

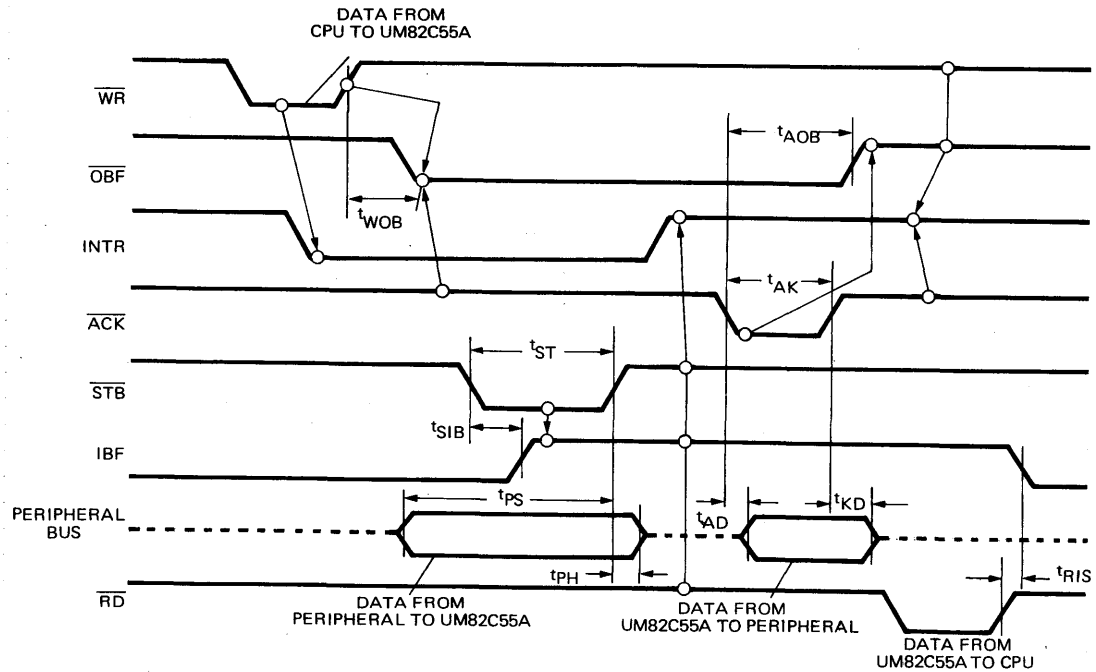
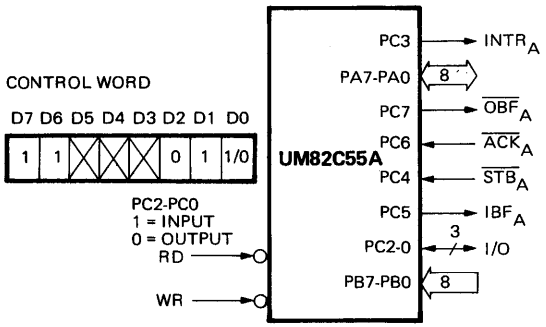


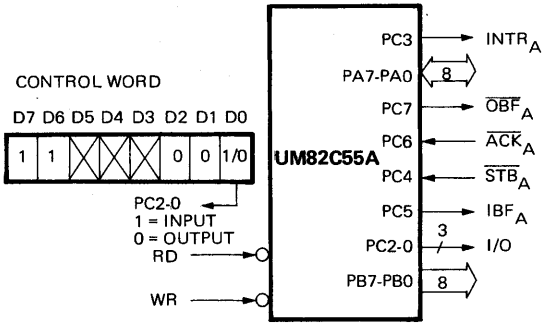
Figure 13. MODE 2 (Bidirectional)

Note: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before RD is permissible. (INTR = IBF · MASK · $\overline{STB}$ · $\overline{RD}$ + $\overline{OBF}$ · MASK · $\overline{ACK}$ · $\overline{WR}$)

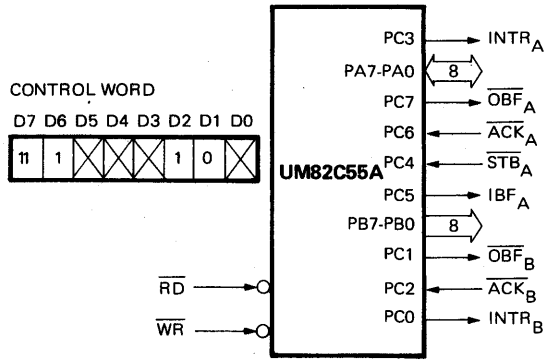
MODE 2 AND MODE 0 (INPUT)



MODE 2 AND MODE 0 (OUTPUT)



MODE 2 AND MODE 1 (OUTPUT)



MODE 2 AND MODE 1 (INPUT)

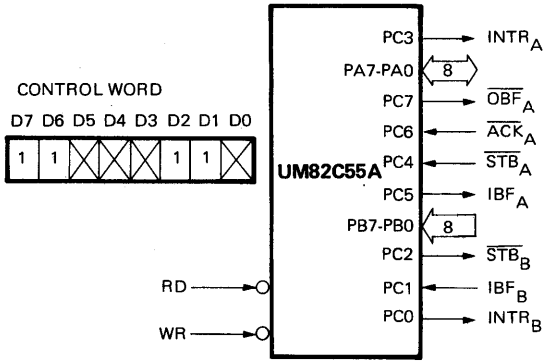


Figure 14. MODE 2 Combinations

Mode Definition Summary

	MODE 0		MODE 1		MODE 2
	IN	OUT	IN	OUT	Group A Only
PA_0	IN	OUT	IN	OUT	←
PA_1	IN	OUT	IN	OUT	←
PA_2	IN	OUT	IN	OUT	←
PA_3	IN	OUT	IN	OUT	←
PA_4	IN	OUT	IN	OUT	←
PA_5	IN	OUT	IN	OUT	←
PA_6	IN	OUT	IN	OUT	←
PA_7	IN	OUT	IN	OUT	←
PB_0	IN	OUT	IN	OUT	—
PB_1	IN	OUT	IN	OUT	—
PB_2	IN	OUT	IN	OUT	—
PB_3	IN	OUT	IN	OUT	—
PB_4	IN	OUT	IN	OUT	—
PB_5	IN	OUT	IN	OUT	—
PB_6	IN	OUT	IN	OUT	—
PB_7	IN	OUT	IN	OUT	—
PC_0	IN	OUT	$INTR_B$	$INTR_B$	I/O
PC_1	IN	OUT	IBF_B	$\overline{OBF}_B$	I/O
PC_2	IN	OUT	$\overline{STB}_B$	ACK_B	I/O
PC_3	IN	OUT	$INTR_A$	$INTR_A$	INTRA
PC_4	IN	OUT	$\overline{STB}_A$	I/O	$\overline{STB}_A$
PC_5	IN	OUT	IBF_A	I/O	IBF_A
PC_6	IN	OUT	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$
PC_7	IN	OUT	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$

MODE 0 OR MODE 1 ONLY

Special Mode Combination Considerations:

There are several combinations of modes possible. For any combination, some or all of Port C lines are used for control or status. The remaining bits are either inputs or outputs as defined by a "Set Mode" command.

During a read of Port C, the state of all the Port C lines except the $\overline{ACK}$ and $\overline{STB}$ lines, will be placed on the data bus. In place of the $\overline{ACK}$ and $\overline{STB}$ line states, flag status will appear on the data bus in the PC2, PC4, and PC6 bit positions as illustrated by Figure 17.

Through a "Write Port C" command, only the Port C pins programmed as outputs in a Mode 0 group can be written. No other pins can be affected by a "Write Port C" command, nor can the interrupt enable flags be accessed. To write to any Port C output programmed as an output in a Mode 1 group or to change an interrupt enable flag, the "Set/Reset Port C Bit" command must be used.

With a "Set/Reset Port C Bit" command, any Port C line programmed as an output (including INTR, IBF and OBF) can be written, or an interrupt enable flag can be either set or reset. Port C lines programmed as inputs, including $\overline{ACK}$ and $\overline{STB}$ lines, associated with Port C are not affected by a "Set/Reset Port C Bit" command. Writing to the corresponding Port C bit positions of the $\overline{ACK}$ and $\overline{STB}$ lines with the "Set/Reset Port C Bit" command will affect the Group A and Group B interrupt enable flags, as illustrated in Figure 17.

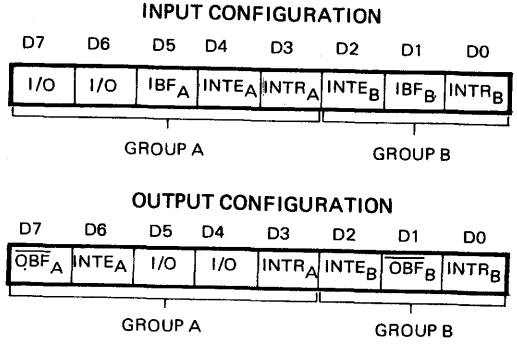


Figure 15. MODE 1 Status Word Format

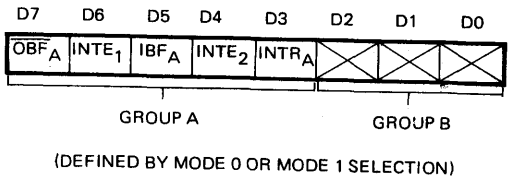


Figure 16. MODE 2 Status Word Format

Interrupt Enable Flag	Position	Alternate Port C Pin Signal (Mode)
INTE B	PC2	$\overline{ACK}_B$ (Output Mode 1) or $\overline{STB}_B$ (Input Mode 1)
INTE A2	PC4	$\overline{STB}_A$ (Input Mode 1 or Mode 2)
INTE A1	PC6	$\overline{ACK}_A$ (Output Mode 1 or Mode 2)

Figure 17. Interrupt Enable Flags in Modes 1 and 2

Current Drive Capability:

Any output on Port A, B or C can sink or source 2.5mA. This feature allows the UM82C55A to directly drive Darlington type drivers and high-voltage displays that require such sink or source current.

Reading Port C Status

In Mode 0, Port C transfers data to or from the peripheral device. When the UM82C55A is programmed to function in Modes 1 or 2, Port C generates or accepts "hand-shaking" signals with the peripheral device. Reading the contents of Port C allows that programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

Applications of the UM82C55A

The UM82C55A is a very powerful tool for interfacing peripheral equipment to the microcomputer system. It represents the optimum use of available pins and is flexible enough to interface almost any I/O device without the need for additional external logic.

Each peripheral device in a microcomputer system usually has a "service routine" associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the UM82C55A is programmed by the I/O service routine and becomes an extension of the system software. By examining the I/O devices interface characteristics for both data transfer and timing, and matching this information to the examples and tables in the detailed operational description, a control word can easily be developed to initialize the UM82C55A to exactly "fit" the application. Figures 18 through 24 present a few examples of typical applications of the UM82C55A.

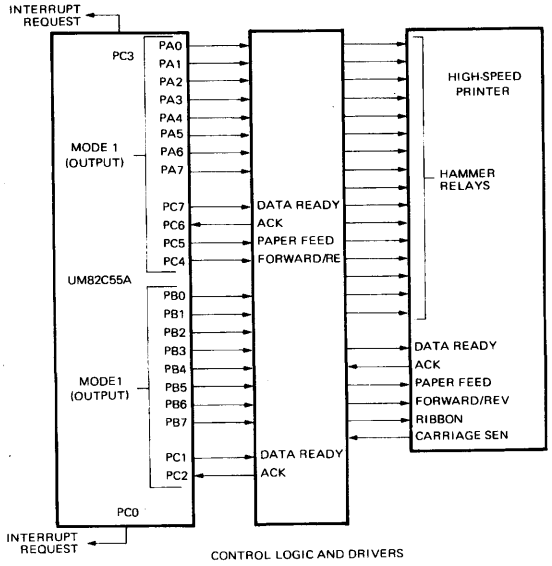


Figure 18. Printer Interface

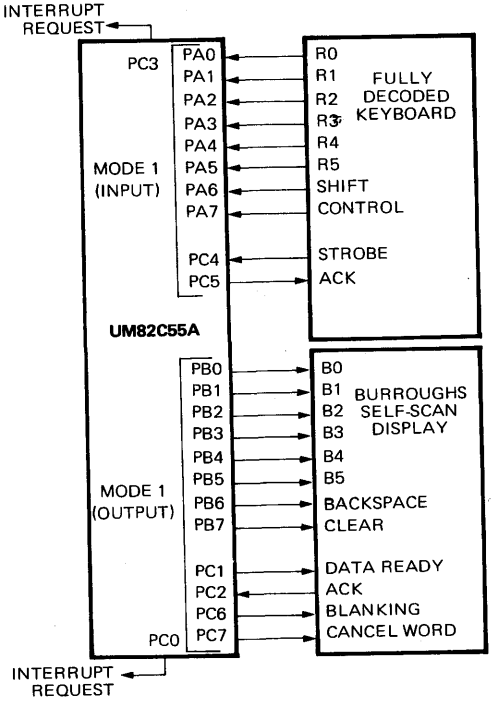


Figure 19. Keyboard and Display Interface

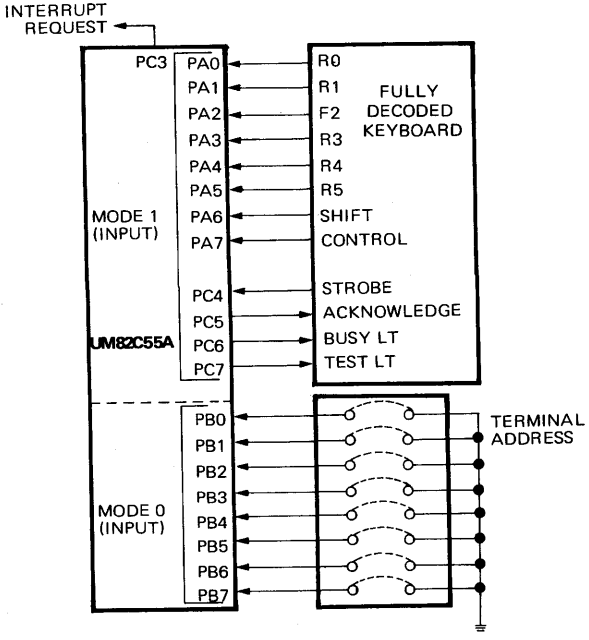


Figure 20. Keyboard and Terminal Address Interface

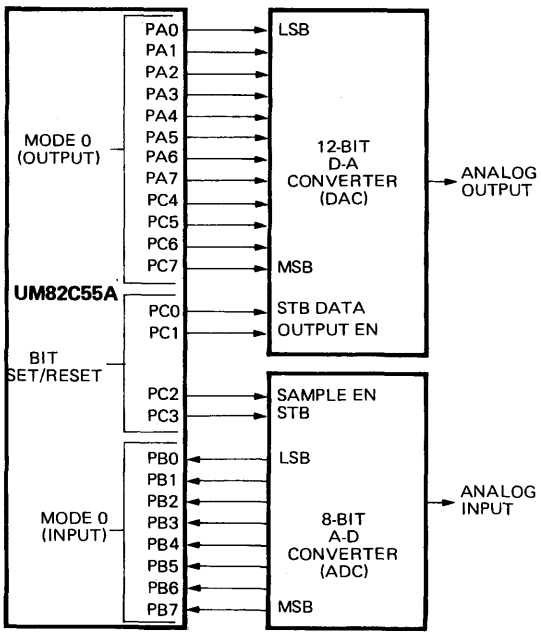


Figure 21. Digital to Analog, Analog to Digital

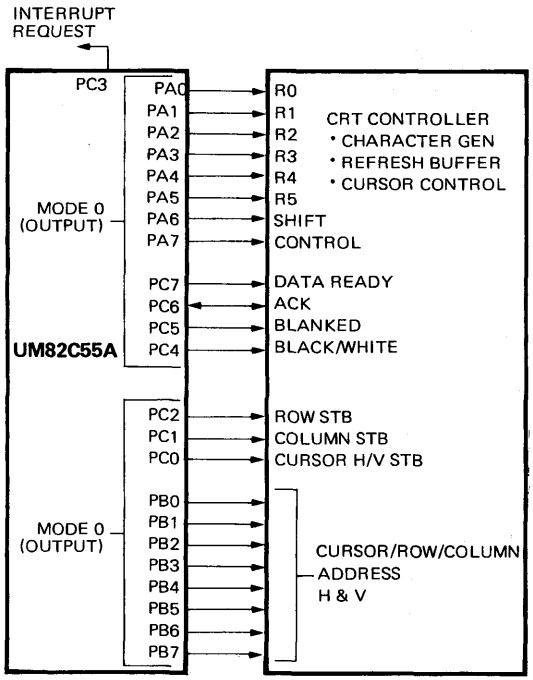


Figure 22. Basic CRT Controller Interface

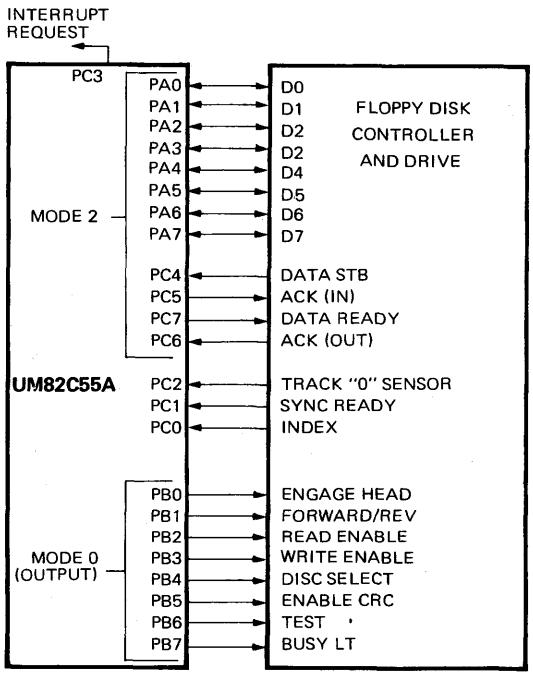


Figure 23. Basic Floppy Disk Interface

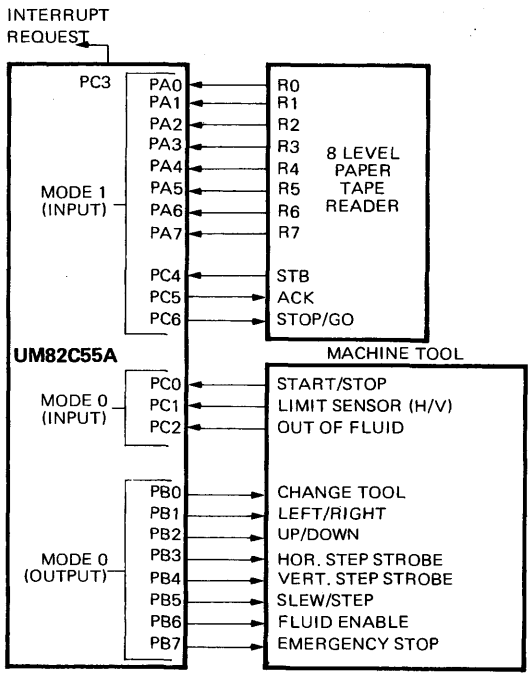


Figure 24. Machine Tool Controller Interface

UM82C59A-2

CMOS Programmable Interrupt Controller

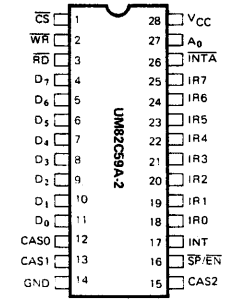
Features

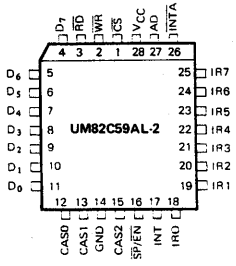
- Pin compatible with NMOS 8259A-2
- Eight-level priority controller
- Expandable to 64 levels
- Programmable interrupt modes
- Low standby current – 10 μA
- Individual request mask capability
- 80C86/88 and 8080/85/86/88 compatible
- Fully static design
- Single 5V power supply
- Available in 28-lead plastic DIP and 28-lead PLCC packages

General Description

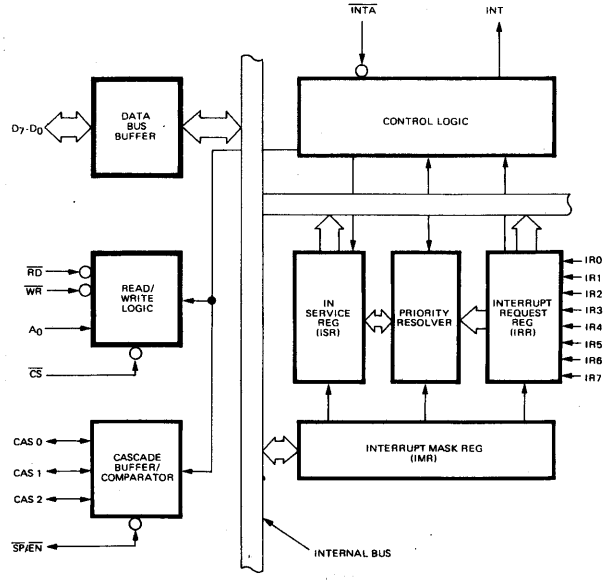
The UM82C59A-2 is a high performance CMOS version of the NMOS Priority Interrupt Controller. The UM82C59A-2 is designed to relieve the system CPU from the task of polling in a multi-level priority interrupt system. The high speed and industry standard configuration of the UM82C59A-2, make it compatible with microprocessors such as the 80C86/88, 8086/88 and 8080/85.
The UM82C59A-2 can handle up to 8 vectored priority interrupts for the CPU and is cascadable to 64 without additional circuitry. It is designed to minimize the software and real time overhead in handling multi-level priority interrupts. Two modes of operation make the UM82C59A-2 optimal for a variety of system requirements. Static CMOS circuit design, requiring no clock input, insures low operating power.

Pin Configurations





Block Diagram



Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . −65°C to + 150°C
Supply Voltage (w.r.t. ground) . . . . . −0.5 to 7.0V
Input Voltage (w.r.t. ground) . . . . . −0.5 to V_{CC} + 0.5V
Output Voltage (w.r.t. ground) . . . . . −0.5 to V_{CC} + 0.5V
Power Dissipation . . . . . 0.9 Watt

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Min	Max	Unit	Conditions
I_{CCS}	Standby Supply Current		10	μA	$V_{IN} = V_{CC}$ or GND All IR = V_{CC} Outputs Unloaded V_{CC} = 5.5V
I_{CC}	Operating Supply Current		5	mA	(Note)
V_{IH}	Input High Voltage	2.2	V_{CC} + 0.5	V	
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.5 mA
V_{OH}	Output High Voltage	3.0 V_{CC} − 0.4		V	I_{OH} = −2.5 mA I_{OH} = −100 μA
I_{LI}	Input Leakage Current		± 1.0	μA	$0V \leqslant V_{IN} \leqslant V_{CC}$
I_{LO}	Output Leakage Current		± 10	μA	$0V \leqslant V_{OUT} \leqslant V_{CC}$
I_{LIR}	IR Input Leakage Current		−300 + 10	μA	V_{IN} = 0 $V_{IN} = V_{CC}$

Note: Repeated data input with 80C86-2 timings.

Capacitance (T_A = 25°C; V_{CC} = GND = 0V)

Symbol	Parameter	Min	Max	Unit	Conditions	
C_{IN}	Input Capacitance		7	pF	fc = 1 MHz	
$C_{I/O}$	I/O Capacitance		20	pF	Unmeasured pins at GND	
C_{OUT}	Output Capacitance		15	pF		

TIMING REQUIREMENTS

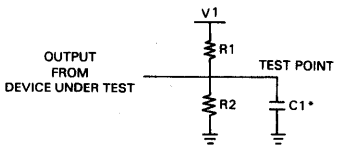
Symbol	Parameter	Min.	Max.	Unit	Conditions
T_{AHWL}	Ao/$\overline{CS}$ Setup to $\overline{WR}$	0		ns	
T_{WHAX}	Ao/$\overline{CS}$ Hold after $\overline{WR}$	0		ns	
T_{WLWH}	$\overline{WR}$ Pulse Width	190		ns	
T_{DVWH}	Data Setup to $\overline{WR}$	160		ns	
T_{WHDX}	Data Hold after $\overline{WR}$	0		ns	
T_{JLJH}	Interrupt Request Width (Low)	100		ns	See Note 1
T_{CVIAL}	Cascade Setup to Second or Third $\overline{INTA}$ (Slave Only)	40		ns	
T_{RHRL}	End of $\overline{RD}$ to next $\overline{RD}$; End of $\overline{INTA}$ to next $\overline{INTA}$ within an $\overline{INTA}$ sequence only	160		ns	
T_{WHWL}	End of $\overline{WR}$ to next $\overline{WR}$	190		ns	
*T_{CHCL}	End of Command to next Command (Not same command type) End of $\overline{INTA}$ sequence to next $\overline{INTA}$ sequence	400		ns	

*Worst case timing for T_{CHCL} in an actual microprocessor system is typically much greater than 400 ns (i.e. 8085A = 1.6μs, 8085A-2 = 1μs, 80C86 = 1μs).
Note: This is the low time required to clear the input latch in the edge triggered mode.

TIMING RESPONSES

Symbol	Parameter	Min.	Max.	Unit	Conditions
T_{RLDV}	Data Valid from $\overline{RD}$/$\overline{INTA}$		120	ns	1
T_{RHDZ}	Data Float after $\overline{RD}$/$\overline{INTA}$	10	85	ns	2
T_{JHIH}	Interrupt Output Delay		300	ns	1
T_{IALCV}	Cascade Valid from First $\overline{INTA}$ (Master Only)		360	ns	1
T_{RLEL}	Enable Active from $\overline{RD}$ or $\overline{INTA}$		100	ns	1
T_{RHEH}	Enable Inactive from $\overline{RD}$ or $\overline{INTA}$		150	ns	1
T_{AHDV}	Data Valid from Stable Address		200	ns	1
T_{CVDV}	Cascade Valid to Valid Data		200	ns	1

AC Test Circuits

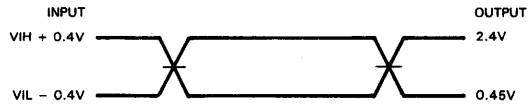


*Includes Stray and Jig Capacitance

Test Condition	V1	R1	R2	C1
1	1.7V	523Ω	Open	100 pF
2	4.5V	1.8KΩ	1.8KΩ	30 pF

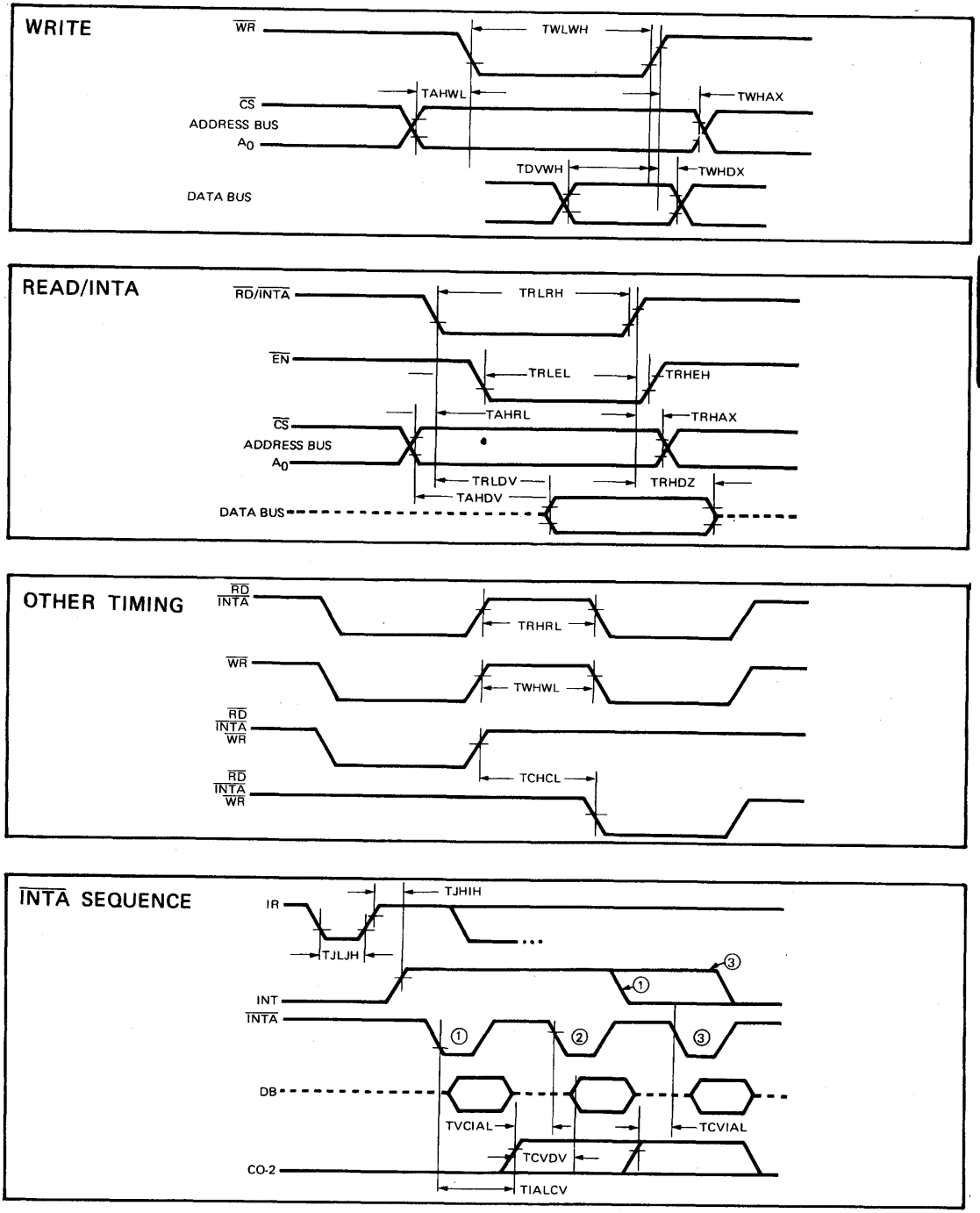
Test Condition Definition Table

AC Testing Input, Output Waveform



AC Testing: All input signals must switch between V_{IL} – 0.4V and V_{IH} + 0.4V. T_R and T_F must be less than or equal to 15 ns.

Timing Waveforms



NOTES:
Interrupt output must remain HIGH at least until leading edge of first INTA.
1. Cycle 1 in 80C86 and 80C88 systems, the Data Bus is not active.

Pin Description

Pin No.	Symbol	I/O	Description
28	V_{CC}	I	SUPPLY: +5V Supply.
14	GND	I	GROUND.
1	$\overline{CS}$	I	CHIP SELECT: A low on this pin enables $\overline{RD}$ and $\overline{WR}$ communication between the CPU and the UM82C59A-2. INTA functions are independent of CS.
2	$\overline{WR}$	I	WRITE: A low on this pin when $\overline{CS}$ is low enables the UM82C59A-2 to accept command words from the CPU.
3	$\overline{RD}$	I	READ: A low on this pin when $\overline{CS}$ is low enables the UM82C59A-2 to release status onto the data bus for the CPU.
4-11	D_7-D_0	I/O	BIDIRECTIONAL DATA BUS: Control, status and interrupt-vector information is transferred via this bus.
12, 13, 15	CAS0-CAS2	I/O	CASCADE LINES: The CAS lines form a private UM82C59A-2 bus to control a multiple UM82C59A-2 structure. These pins are outputs for a master UM82C59A-2 and inputs for a slave UM82C59A-2.
16	SP/EN	I/O	SLAVE PROGRAM/ENABLE BUFFER: This is a dual function pin. When in the Buffered Mode it can be used as an output to control buffer transceivers (EN). When not in the buffered mode it is used as an input to designate a master (SP = 1) or slave (SP = 0).
17	INT	O	INTERRUPT: This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, thus it is connected to the CPU's interrupt pin.
18-25	IR0-IR7	I	INTERRUPT REQUESTS: Asynchronous inputs. An interrupt request is executed by raising an IR input (low to high), and holding it high until it is acknowledged (Edge Triggered Mode), or just by a high level on an IR input (Level Triggered Mode). Internal pull-up resistors are implemented on IR0-7.
26	$\overline{INTA}$	I	INTERRUPT ACKNOWLEDGE: This pin is used to enable UM82C59A-2 interrupt-vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
27	A_0	I	A_0 ADDRESS LINE: This pin acts in conjunction with the $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ pins. It is used by the 82C59A-2 to decipher various Command Words the CPU writes and status the CPU wishes to read. It is typically connected to the CPU A_0 address line (A_1 for 80C86, 80C88).

Functional Description

Interrupts in Microcomputer Systems

Microcomputer system design requires that I/O devices such as keyboards, displays, sensors and other components receive servicing in an efficient manner so that large amounts of the total system tasks can be assumed by the microcomputer with little or no effect on throughput.

The most common method of servicing such devices is the Polled approach. This is where the processor must test each device in sequence and in effect "ask" each one if it needs servicing. It is easy to see that a large portion of the main program is looping through this continuous polling cycle and that such a method would have a serious, detrimental effect on system throughput, thus limiting the tasks that could be assumed by the microcomputer and reducing the cost effectiveness of using such devices.

A more desirable method would be one that would allow the microprocessor to be executing its main program and only stop to service peripheral devices when it is told to do so by the device itself. In effect, the method would provide an external asynchronous input that would inform the processor that it should complete whatever instruction that is currently being executed and fetch a new routine that will service the requesting device. Once this servicing is complete, however, the processor would resume exactly where it left off.

This method is called interrupt. It is easy to see that system throughput would drastically increase, and thus more tasks could be assumed by the microcomputer to further enhance its cost effectiveness.

The Programmable Interrupt Controller (PIC) functions as an overall manager in an Interrupt-Driven system environment. It accepts requests from the peripheral equipment, determines which of the incoming requests is of the highest importance (priority), ascertains whether the incoming request has a higher priority value than the level currently being serviced, and issues an interrupt to the CPU based on this determination.

Each peripheral device or structure usually has a special program or "routine" that is associated with its specific functional or operational requirements; this is referred to as a "service routine". The PIC, after issuing an interrupt to the CPU, must somehow input information into the CPU that can "point" the Program Counter to the service routine associated with the requesting device. This "pointer" is an address in a vectoring table and will often be referred to, in this document, as vectoring data.

The UM82C59A-2

The UM82C59A-2 is a device specifically designed for use in real time, interrupt driven microcomputer systems. It manages eight levels or requests and has built-in features for expandability to other UM82C59A-2's (up to 64 levels). It is programmed by system's software as an I/O peripheral. A selection of priority modes is available to the programmer so that the manner in which the requests are processed by the UM82C59A-2 can be configured to match system requirements. The priority modes can be changed or reconfigured dynamically at any time during the main program. This means that the complete interrupt structure can be defined as required, based on the total system environment.

Interrupt Request Register (IRR) and In-Service Register (ISR)

The interrupts at the IR input lines are handled by two registers in cascade, the Interrupt Request Register (IRR) and the In-Service Register (ISR). The IRR is used to store all the interrupt levels which are requesting service, and the ISR is used to store all the interrupt levels which are currently being serviced.

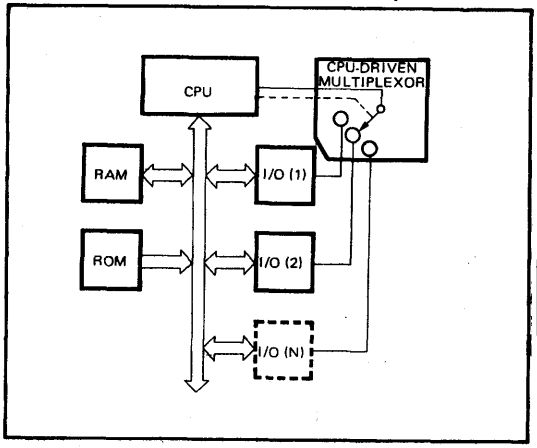


Figure a. Polled Method

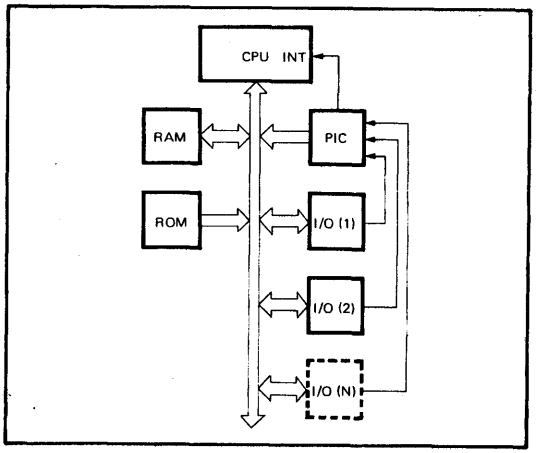


Figure b. Interrupt Method

Priority Resolver

This logic block determines the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during $\overline{INTA}$ sequence.

Interrupt Mask Register (IMR)

The IMR stores the bits which mask the interrupt lines to be masked. The IMR operates on the IRR. Masking of a higher priority input will not affect the interrupt request lines of lower priority.

INT (Interrupt)

This output goes directly to the CPU interrupt input. The V_{OH} level on this line is designed to be fully compatible with the 8080A, 8085A, 80C88 and 80C86 input levels.

$\overline{INTA}$ (Interrupt Acknowledge)

INTA pulses will cause the UM82C59A-2 to release vectoring information onto the data bus. The format of this data depends on the system mode (μPM) of the UM82C59A-2.

Data Bus Buffer

This 3-state, bidirectional 8-bit buffer is used to interface the UM82C59A-2 to the system Data Bus. Control words and status information are transferred through the Data Bus Buffer.

Read/Write Control Logic

The function of this block is to accept Output commands from the CPU. It contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers which store the various control formats for device operation. This function block also allows the status of the UM82C59A-2 to be transferred onto the Data Bus.

$\overline{CS}$ (Chip Select)

A LOW on this input enables the UM82C59A-2. No reading or writing of the device will occur unless the device is selected.

$\overline{WR}$ (Write)

A LOW on this input enables the CPU to write control words (ICWs and OCWs) to the UM82C59A-2.

$\overline{RD}$ (Read)

A LOW on this input enables the UM82C59A-2 to send the status of the Interrupt Request Register (IRR). In Service Register (ISR), the Interrupt Mask Register (IMR), or the interrupt level (in the poll mode) onto the Data Bus.

A_0

This input signal is used in conjunction with $\overline{WR}$ and $\overline{RD}$ signals to write commands into the various command registers, as well as reading the various status registers of the chip. This line can be tied directly to one of the address lines.

The Cascade Buffer/Comparator

This function block stores and compares the IDs of all UM82C59A-2's used in the system. The associated three I/O pins (CAS0-2) are outputs when the UM82C59A-2 is used as a master and are inputs when the UM82C59A-2

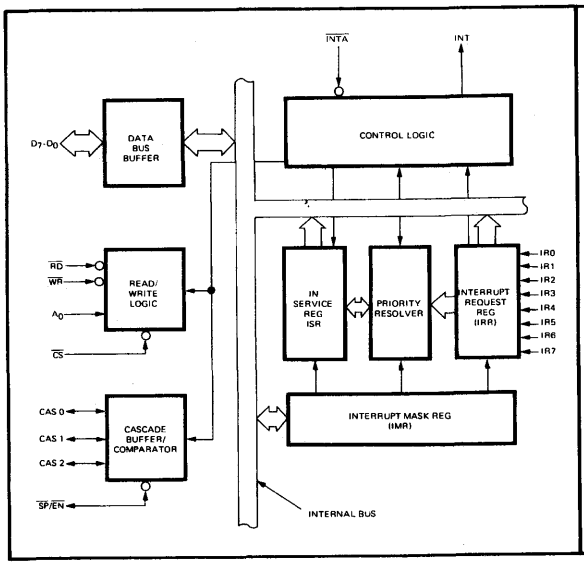


Figure 4. UM82C59A-2 Block Diagram

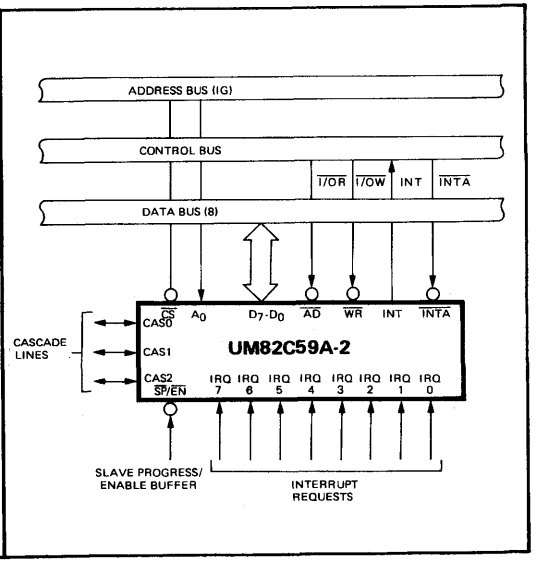


Figure 5. UM82C59A-2 Interface to Standard System Bus

is used as a slave. As a master, the UM82C59A-2 sends the ID of the interrupting slave device onto the CAS0-2 lines. The slave thus selected will send its preprogrammed subroutine address onto the Data Bus during the next one or two consecutive $\overline{INTA}$ pulses. (See section "Cascading the UM82C59A-2".)

Interrupt Sequence

The powerful features of the UM82C59A-2 in a microcomputer system are its programmability and the interrupt routine addressing capability. The latter allows direct or indirect jumping to the specified interrupt routine requested without any polling of the interrupting devices. The normal sequence of events during an interrupt depends on the type of CPU being used.

The events occur as follows in an MCS-80/85 system:

1. One or more of the INTERRUPT REQUEST lines (IR7-0) are raised high, setting the corresponding IRR bit(s).
2. The UM82C59A-2 evaluates these requests, and sends an INT to the CPU, if appropriate.
3. The CPU acknowledges the INT and responds with an $\overline{INTA}$ pulse.
4. Upon receiving an $\overline{INTA}$ from the CPU group, the highest priority ISR bit is set, and the corresponding IRR bit is reset. The UM82C59A-2 will also release a CALL instruction code (11001101) onto the 8-bit data bus through D_0-D_7 pins.
5. This CALL instruction will initiate two more $\overline{INTA}$ pulses to be sent to the UM82C59A-2 from the CPU group.
6. These two $\overline{INTA}$ pulses allow the UM82C59A-2 to release its preprogrammed subroutine address onto the Data Bus. The lower 8-bit address is released at the first $\overline{INTA}$ pulse and the higher 8-bit address is released at the second $\overline{INTA}$ pulse.
7. This completes the 3-byte CALL instruction released by the UM82C59A-2. In the AEOI mode, the ISR bit is reset at the end of the third $\overline{INTA}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt sequence.

The events occurring in an 80C86 system are the same until step 4.

4. Upon receiving an $\overline{INTA}$ from the CPU group, the highest priority ISR bit is set and the corresponding IRR bit is reset. The UM82C59A-2 does not drive the data bus during this cycle.
5. The 80C86 will initiate a second $\overline{INTA}$ pulse. During this pulse, the UM82C59A-2 releases an 8-bit pointer onto the Data Bus where it is read by the CPU.
6. This completes the interrupt cycle. In the AEOI mode, the ISR bit is reset at the end of the second $\overline{INTA}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

If no interrupt is present at step 4 of either sequence (i.e., the request was too short in duration), the UM82C59A-2 will issue an interrupt level 7. Both the vectoring bytes and the CAS lines will look like an interrupt level 7 was requested.

Interrupt Sequence Outputs

MCS®-80, MCS-85

This sequence is timed by three $\overline{INTA}$ pulses. During the first $\overline{INTA}$ pulse, the CALL opcode is enabled onto the data bus.

Content of First Interrupt Vector Byte

	D7	D6	D5	D4	D3	D2	D1	D0
CALL CODE	1	1	0	0	1	1	0	1

During the second $\overline{INTA}$ pulse, the lower address of the appropriate service routine is enabled onto the Data Bus. When interval = 4 bits, A_5-A_7 are programmed, while A_0-A_4 are automatically inserted by the UM82C59A-2. When interval = 8, only A_4 and A_7 are programmed, while A_0-A_5 are automatically inserted.

Content of Second Interrupt Vector Byte

IR	Interval = 4							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	A5	1	1	1	0	0
6	A7	A6	A5	1	1	0	0	0
5	A7	A6	A5	1	0	1	0	0
4	A7	A6	A5	1	0	0	0	0
3	A7	A6	A5	0	1	1	0	0
2	A7	A6	A5	0	1	0	0	0
1	A7	A6	A5	0	0	0	0	0
0	A7	A6	A5	0	0	0	0	0

IR	Interval = 8							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	1	1	1	0	0	0
6	A7	A6	1	1	0	0	0	0
5	A7	A6	1	0	1	0	0	0
4	A7	A6	1	0	0	0	0	0
3	A7	A6	0	1	1	0	0	0
2	A7	A6	0	1	0	0	0	0
1	A7	A6	0	0	1	0	0	0
0	A7	A6	0	0	0	0	0	0

During the third $\overline{INTA}$ pulse, the higher address of the appropriate service routine, which was programmed as byte 2 of the initialization sequence (A_5-A_{15}), is enabled onto the bus.

Content of Third Interrupt Vector Byte

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

80C86, 80C88

80C86, 80C88 mode is similar to MCS-80 mode except that only two interrupt Acknowledge cycles are issued by the processor and no CALL opcode is sent to the processor. The first interrupt acknowledge cycle is similar to that of MCS-80,85 systems in that the UM82C59A-2 uses it to internally freeze the state of the interrupts for priority resolution and as a master it issues the interrupt code on the cascade lines at the end of the $\overline{INTA}$ pulse. On this first cycle, it does not issue any data to the processor and leaves its Data Bus buffers disabled. On the second interrupt acknowledge cycle in 80C86, 80C88 mode, the master (or slave if so programmed) will send a byte of data to the processor with the acknowledged interrupt code composed as follows (note the state of the ADI mode control is ignored and A_5-A_{11} are unused in 80C86, 80C88 mode.):

Content of Interrupt Vector Byte for 80C86, 80C88 System Mode

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	T7	T6	T5	T4	T3	1	1	1
IR6	T7	T6	T5	T4	T3	1	1	0
IR5	T7	T6	T5	T4	T3	1	0	1
IR4	T7	T6	T5	T4	T3	1	0	0
IR3	T7	T6	T5	T4	T3	0	1	1
IR2	T7	T6	T5	T4	T3	0	1	0
IR1	T7	T6	T5	T4	T3	0	0	1
IR0	T7	T6	T5	T4	T3	0	0	0

Programming the UM82C59A-2

The UM82C59A-2 accepts two types of command words generated by the CPU:

1. Initialization Command Words (ICWs): Before normal operation can begin, each UM82C59A-2 in the system must be brought to a starting point – by a sequence of 2 to 4 bytes timed by $\overline{WR}$ pulses.

2. Operation Command Words (OCWs): These are the command words which command the UM82C59A-2 to operate in various interrupt modes. These modes are:
   a. Fully nested mode
   b. Rotating priority mode
   c. Special mask mode
   d. Polled mode

The OCWs can be written into the UM82C59A-2 anytime after initialization.

Initialization Command Words (ICWS)

General

Whenever a command is issued with A_0 = 0 and D_4 = 1, this is interpreted as Initialization Command Word 1 (ICW1). ICW1 starts the initialization sequence during which the following automatically occur.

a. The edge sense circuit is reset, which means that following initialization, an interrupt request (IR) input must make a low-to-high transition to generate an interrupt.
b. The Interrupt Mask Register is cleared.
c. IR7 input is assigned priority 7.
d. The slave mode address is set to 7.
e. Special Mask Mode is cleared and Status Read is set to IRR.
f. If IC4 = 0, then all functions selected in ICW4 are set to zero. (Non-Buffered mode*, no Auto-EOI, MCS-80, 85 system).

*NOTE: Master/Slave in ICW4 is only used in the buffered mode.

Initialization Command Words 1 and 2 (ICW1, ICW2)

A_5-A_{15}: Page starting address of service routines. In an MCS-80,85 system, the 8 request levels will generate CALLS to 8 locations equally spaced in memory. These can be programmed to be spaced at intervals of 4 or 8 memory locations, thus the 8 routines will occupy a page of 32 or 64 bytes, respectively.

The address format is 2 bytes long (A_0-A_{15}). When the routine interval is 4, A_0-A_4 are automatically inserted by the UM82C59A-2, while A_5-A_{15} are programmed externally. When the routine interval is 8, A_0-A_5 are automatically inserted by the UM82C59A-2 while A_6-A_{15} are programmed externally.

The 8-byte interval will maintain compatibility with current software, while the 4-byte interval is best for a compact jump table.

In an 80C86, 80C88 system, A_{15}-A_{11} are inserted in the five most significant bits of the vectoring byte and the UM82C59A-2 sets the three least significant bits according to the interrupt level. A_{10}-A_5 are ignored and ADI (Address interval) has no effect.

LTIM: If LTIM = 1, then the UM82C59A-2 will operate in the level interrupt mode. Edge detect logic on the interrupt inputs will be disabled.

ADI: CALL address interval. ADI = 1 then interval = 4; ADI = 0 then interval = 8.

SNGL: Single. Means that this is the only UM82C59A-2 in the system. If SNGL = 1, no ICW3 will be issued.

IC4: If this bit is set – ICW4 has to be issued. If ICW4 is not needed, set IC4 = 0.

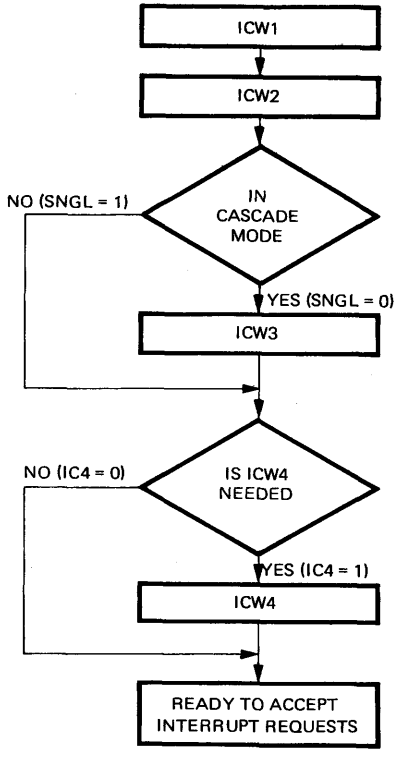
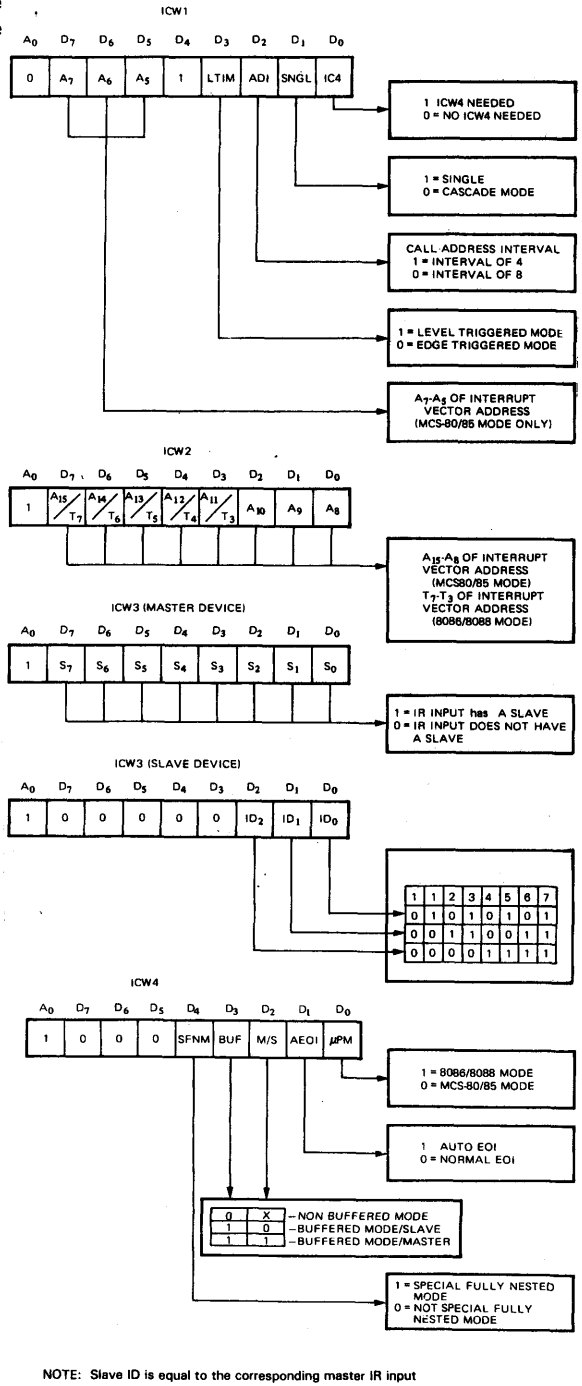


Figure 6. Initialization Sequence



NOTE: Slave ID is equal to the corresponding master IR input

Figure 7. Initialization Command Word Format

PC Mainboard

Initialization Command Word 3 (ICW3)

This word is read only when there is more than one UM82C59A-2 in the system and cascading is used, in which case SNGL = 0. It will load the 8-bit slave register. The functions of this register are:

a. In the master mode (either when SP = 1, or in buffered mode when M/S = 1 in ICW4), a "1" is set for each slave in the system. The master then will release byte 1 of the call sequence (for MCS80/85 system) and will enable the corresponding slave to release bytes 2 and 3 (for 80C86, 80C88 only byte 2) through the cascade lines.

b. In the slave mode (either when $\overline{SP}$ = 0, or if BUF = 1 and M/S = 0 in ICW4), bits 2-0 identify the slave. The slave compares its cascade input with these bits and if they are equal, bytes 2 and 3 of the call sequence (or just byte 2 for 80C86, 80C88) are released by it on the Data Bus.

Initialization Command Word 4 (ICW4)

SFNM: If SFNM = 1, the special fully nested mode is programmed.

BUF: If BUF = 1, the buffered mode is programmed. In buffered mode, $\overline{SP}/\overline{EN}$ becomes an enable output and the master/slave determination is by M/S.

M/S: If buffered mode is selected: M/S = 1 means the UM82C59A-2 is programmed to be a master, M/S = 0 means the UM82C59A-2 is programmed to be a slave. If BUF = 0, M/S has no function.

AEOI: If AEOI = 1, the automatic end of interrupt mode is programmed.

μPM: Microprocessor mode: μPM = 0 sets the UM82C59A-2 for MCS-80,85 system operation, μPM = 1 sets the UM82C59A-2 for 80C86 system operation.

Operation Command Words (OCWs)

After the initialization Command Words (ICWs) are programmed into the UM82C59A-2, the device is ready to accept interrupt requests at its input lines. However, during the UM82C59A-2 operation, a selection of algorithms can command the UM82C59A-2 to operate in various modes through the Operation control Words (OCWs).

Operation Control Words (OCWs)

	A0	D7	D6	D5	D4	D3	D2	D1	D0
OCW1	1	M7	M6	M5	M4	M3	M2	M1	M0
OCW2	0	R	SL	EOI	0	0	L2	L1	L0
OCW3	0	0	ESMM	SMM	0	1	P	RR	RIS

Operation Control Word 1 (OCW1)

OCW1 sets and clears the mask bits in the interrupt Mask Register (IMR). M_7-M_0 represent the eight mask bits. M = 1 indicates the channel is masked (inhibited), M = 0 indicates the channel is enabled.

Operation Control Word 2 (OCW2)

R, SL, EOI – These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations can be found on the Operation Command Word Format.

L_2, L_1, L_0 – These bits determine the interrupt level acted upon when the SL bit is active.

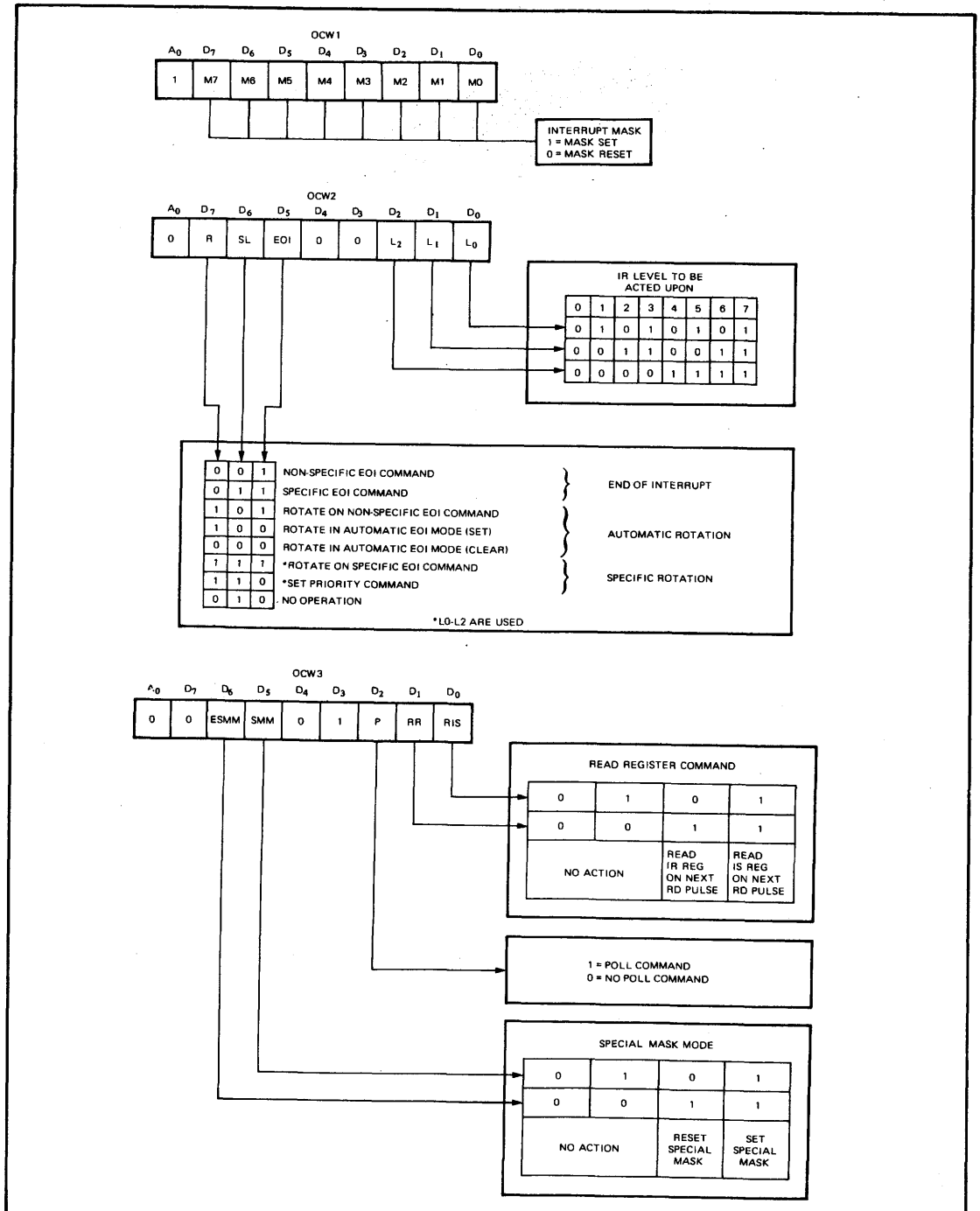


Figure 8. Operation Command Word Format

Operation Control Word 3 (OCW3)

ESMM – Enable Special Mask Mode. When this bit is set to 1 it enables the SMM bit to set or reset the Special Mask Mode. When ESMM = 0, the SMM bit becomes a "don't care".

SMM – Special Mask Mode. If ESMM = 1 and SMM = 1, the UM82C59A-2 will enter Special Mask Mode. If ESMM = 1 and SMM = 0, the UM82C59A-2 will revert to normal mask mode. When ESMM = 0, SMM has no effect.

Fully Nested Mode

This mode is entered after initialization unless another mode is programmed. The interrupt requests are ordered in priority from 0 through 7 (0 highest). When an interrupt is acknowledged the highest priority request is determined and its vector placed on the bus. Additionally, a bit of the Interrupt Service register (IS0-7) is set. This bit remains set until the microprocessor issues an End of Interrupt (EOI) command immediately before returning from the service routine, or if AEOI (Automatic End of Interrupt) bit is set, until the trailing edge of the last $\overline{INTA}$. While the IS bit is set, all further interrupts of the same or lower priority are inhibited, while higher levels will generate an interrupt (which will be acknowledged only if the microprocessor internal interrupt enable flip-flop has been re-enabled through software).

After the initialization sequence, IR0 has the highest priority and IR7 the lowest. Priorities can be changed, as will be explained, in the rotating priority mode.

End Of Interrupt (EOI)

The In Service (IS) bit can be reset either automatically following the trailing edge of the last in sequence $\overline{INTA}$ pulse (when AEOI bit in ICW4 is set) or by a command word that must be issued to the UM82C59A-2 before returning from a service routine (EOI command). An EOI command must be issued twice if in the Cascade mode, once for the master and once for the corresponding slave.

There are two forms of EOI command: Specific and Non-Specific. When the UM82C59A-2 is operated in modes which preserve the fully nested structure, it can determine which IS bit to reset on EOI. When a Non-Specific EOI command is issued the UM82C59A-2 will automatically reset the highest IS bit of those that are set, since in the fully nested mode the highest IS level was necessarily the last level acknowledged and serviced. A non-specific EOI can be issued with OCW2 (EOI = 1, SL = 0, R = 0).

When a mode is used which may disturb the fully nested structure, the UM82C59A-2 may no longer be able to determine the last level acknowledged. In this case a Specific End of Interrupt must be issued which includes as part of the command the IS level to be reset. A specific EOI can be issued with OCW2 (EOI = 1, SL = 1, R = 0, and L0-L2 is the binary level of the IS bit to be reset).

It should be noted that an IS bit that is masked by an IMR bit will not be cleared by a non-specific EOI if the UM82C59A-2 is in the Special Mask Mode.

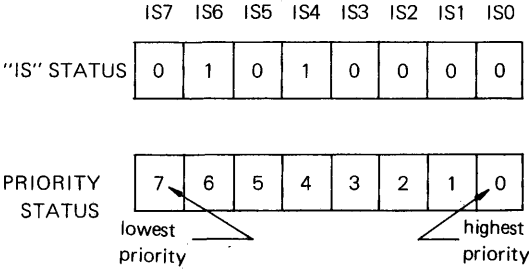
Automatic End of Interrupt (AEOI) Mode

If AEOI = 1 in ICW4, then the UM82C59A-2 will operate in AEOI mode continuously until reprogrammed by ICW4. In this mode the UM82C59A-2 will automatically perform a non-specific EOI operation at the trailing edge of the last interrupt acknowledge pulse (third pulse in MCS-80/85, second in 80C86/88). Note that from a system standpoint, this mode should be used only when a nested multi-level interrupt structure is not required within a single UM82C59A-2.

Automatic Rotation (Equal Priority Devices)

In some applications there are a number of interrupting devices of equal priority. In this mode a device, after being serviced, receives the lowest priority, so a device requesting an interrupt will have to wait, in the worst case until each of 7 other devices are serviced at most once. For example, if the priority and "in service" status is:

Before Rotate (IR4 the highest priority requiring service)



After Rotate (IR4 was serviced, all other priorities rotated correspondingly)

	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
"IS" STATUS	0	1	0	0	0	0	0	0

	2	1	0	7	6	5	4	3
PRIORITY STATUS	highest priority							lowest priority

There are two ways to accomplish Automatic Rotation using OCW2, the Rotation on Non-Specific EOI Command (R = 1, SL = 0, EOI = 1) and the Rotate in Automatic EOI Mode which is set by (R = 1, SL = 0, EOI = 0) and cleared by (R = 0, SL = 0, EOI = 0).

Specific Rotation (Specific Priority)

The programmer can change priorities by programming the bottom priority and thus fixing all other priorities; i.e., if IR5 is programmed as the bottom priority device, then IR6 will have the highest one.

The Set Priority command is issued in OCW2 where: R = 1, SL = 1; L0-L2 is the binary priority level code of the bottom priority device.

Observe that in this mode internal status is updated by software control during OCW2. However, it is independent of the End of Interrupt (EOI) command (also executed by OCW2). Priority changes can be executed during an EOI command by using the Rotate on Specific EOI command in OCW2 (R = 1, SL = 1, EOI = 1 and L0-L2 = IR level to receive bottom priority).

Interrupt Masks

Each Interrupt Request input can be masked individually by the Interrupt Mask Register (IMR) programmed through OCW1. Each bit in the IMR masks one interrupt channel if it is set (1). Bit 0 masks IR0, Bit 1 masks IR1 and so forth. Masking an IR channel does not affect the other channels operation.

Special Mask Mode

Some applications may require an interrupt service routine to dynamically alter the system priority structure during its execution under software control. For example, the routine may wish to inhibit lower priority requests for a portion of its execution but enable some of them for another portion.

The difficulty here is that if an Interrupt Request is acknowledged and an End of Interrupt command did not reset its IS bit (i.e., while executing a service routine), the UM82C59A-2 would have inhibited all lower priority requests with no easy way for the routine to enable them.

That is where the Special Mask Mode comes in. In the special Mask Mode, when a mask bit is set in OCW1, it inhibits further interrupts at that level and enables interrupts from all other levels (lower as well as higher) that are not masked.

Thus, any interrupts may be selectivity enabled by loading the mask register.

The special Mask Mode is set by OCW3 where: SSMM = 1, SMM = 1, and cleared where SSMM = 1, SMM = 0.

Poll Command

In this mode, the INT output is not used or the microprocessor internal Interrupt Enable flip-flop is reset, disabling its interrupt input. Service to devices is achieved by software using a Poll command.

The Poll command is issued by setting P ="1" in OCW3. The UM82C59A-2 treats the next $\overline{RD}$ pulse to the UM82C59A-2 (i.e., $\overline{RD}$ = 0, $\overline{CS}$ = 0) as an interrupt acknowledge, sets the appropriate IS bit if there is a request, and reads the priority level. Interrupt is frozen from $\overline{WR}$ to $\overline{RD}$.

The word enabled onto the data bus during $\overline{RD}$ is:

D7	D6	D5	D4	D3	D2	D1	D0
I	–	–	–	–	W2	W1	W0

W0-W2: Binary code of the highest priority level requesting service.

1: Equal to a "1" if there is an interrupt.

This mode is useful if there is a routine command common to several levels so that the $\overline{INTA}$ sequence is not needed (saves ROM space). Another application is to use the poll mode to expand the number of priority levels to more than 64.

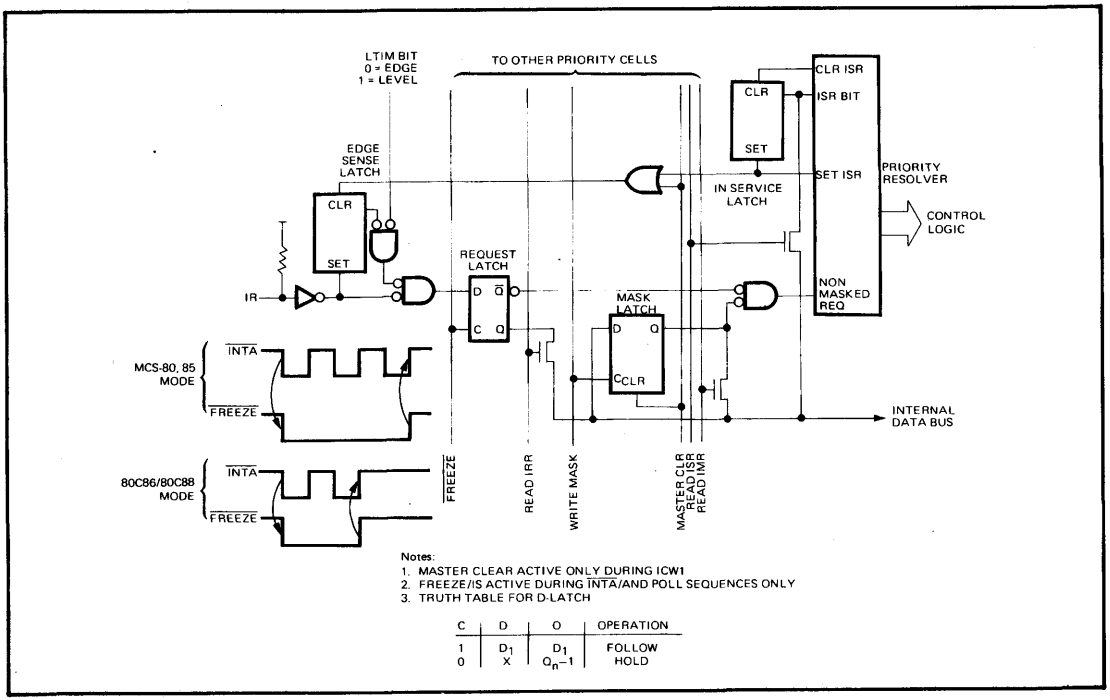


Figure 9. Priority Cell – Simplified Logic Diagram

Reading the UM82C59A-2 Status

The input status of several internal registers can be read to update the user information on the system. The following registers can be read via OCW3 (IRR and ISR or OCW1 (IMR)).

Interrupt Request Register (IRR): 8-bit register which contains the levels requesting an interrupt to be acknowledged. The highest request level is reset from the IRR when an interrupt is acknowledged. (Not affected by IMR).

In-Service Register (ISR): 8-bit register which contains the priority levels that are being serviced. The ISR is updated when an End of Interrupt Command is issued.

Interrupt Mask Register: 8-bit register which contains the interrupt request lines which are masked.

The IRR can be read when prior to the $\overline{RD}$ pulse, a Read Register Command is issued with OCW3 (RR = 1, RIS = 1).

There is no need to write an OCW3 before every status read operation, as long as the status read corresponds with the previous one; i.e., the UM82C59A-2 "remembers" whether the IRR or ISR has been previously selected by the OCW3. This is not true when poll is used. After initialization, the UM82C59A-2 is set to IRR.

For reading the IMR, no OCW3 is needed. The output data bus will contain the IMR whenever $\overline{RD}$ is active and A0 = 1 (OCW1). Polling overrides status read when P = 1, RR = 1 in OCW3.

Edge and Level Triggered Modes

This mode is programmed using bit 3 in ICW1.

If LTIM = '0', an interrupt request will be recognized by a low to high transition on an IR input. The IR input can remain high without generating another interrupt.

If LTIM = '1', an interrupt request will be recognized by a 'high' level on IR Input, and there is no need for an edge detection. The interrupt request must be removed before the EOI command is issued or the CPU

interrupt is enabled to prevent a second interrupt from occurring.

The priority cell diagram shows a conceptual circuit of the level sensitive and edge sensitive input circuitry of the UM82C59A-2. Be sure to note that the request latch is a transparent D type latch.

In both the edge and level triggered modes the IR inputs must remain high until after the falling edge of the first $\overline{\text{INTA}}$. If the IR input goes low before this time a DEFAULT IR7 will occur when the CPU acknowledges the interrupt. This can be a useful safeguard for detecting interrupts caused by spurious noise glitches on the IR inputs. To implement this feature the IR7 routine is used for "clean up" simply executing a return instruction, thus ignoring the interrupt. If IR7 is needed for other purposes a default IR7 can still be detected by reading the ISR. A normal IR7 interrupt will set the corresponding ISR bit, a default IR7 won't. If a default IR7 routine occurs during a normal IR7 routine, however, the ISR will remain set. In this case it is necessary to keep track of whether or not the IR7 routine was previously entered. If another IR7 occurs it is a default.

In power sensitive applications, it is advisable to place the UM82C59A-2 in the edge-triggered mode. This will minimize the current through the pull-up resistors on the IR pins.

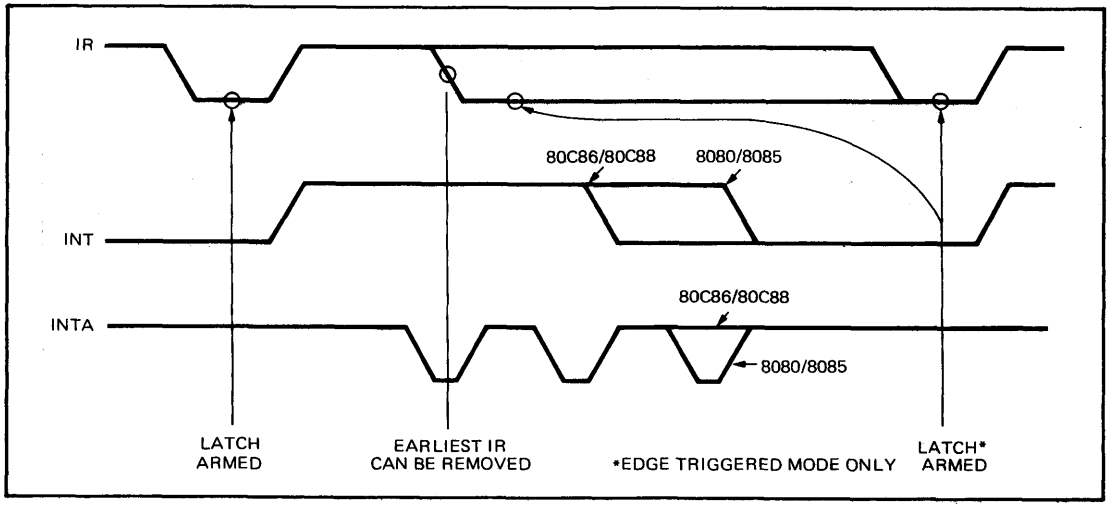


Figure 10. IR Triggering Timing Requirements

The Special Fully Nested Mode

This mode will be used in the case of a big system where cascading is used, and the priority has to be conserved within each slave. In this case the fully nested mode will be programmed to the master (using ICW4). This mode is similar to the normal nested mode with the following exceptions:

a. When an interrupt request from a certain slave is in service, this slave is not locked out from the master's priority logic and further interrupt requests from higher priority IR's within the slave will be recognized by the master and will initiate interrupts to the processor. (In the normal nested mode a slave is masked out when its request is in service and no higher requests from the same slave can be serviced.)

b. When exiting the Interrupt Service routine the software has to check whether the interrupt serviced was the only one from that slave. This is done by sending a non-specific End of Interrupt (EOI) command to the slave and then reading its In-Service register and checking for zero. If it is empty, a non-specified EOI can be sent to the master, too. If not, no EOI should be sent.

Buffered Mode

When the UM82C59A-2 is used in a large system where bus driving buffers are required on the data bus and the cascading mode is used, there exists the problem of enabling buffers.

The buffered mode will structure the UM82C59A-2 to send an enable signal on $\overline{SP}/\overline{EN}$ to enable the buffers. In this mode, whenever the UM82C59A-2's data bus outputs are enabled, the $\overline{SP}/\overline{EN}$ output becomes active.

This modification forces the use of software programming to determine whether the UM82C59A-2 is a master or a slave. Bit 3 in ICW4 programs the buffered mode, and bit 2 in ICW3 determines whether it is a master or a slave.

Cascade Mode

The UM82C59A-2 can be easily interconnected in a system of one master with up to eight slaves to handle up to 64 priority levels.

The master controls the slaves through the 3 line cascade bus. The cascade bus acts like chip selects to the slaves during the $\overline{INTA}$ sequence.

In a cascade configuration, the slave interrupt outputs are connected to the master interrupt request inputs. When a slave request line is activated and afterwards acknowledged, the master will enable the corresponding slave to release the device routine address during bytes 2 and 3 of INTA. (Byte 2 only for 80C86/8088).

The cascade bus lines are normally low and will contain the slave address code from the trailing edge of the first $\overline{INTA}$ pulse to the trailing edge of the third pulse. Each UM82C59A-2 in the system must follow a separate initialization sequence and can be programmed to work in a different mode. An EOI command must be issued twice: Once for the master and once for the corresponding slave. An adress decoder is required to activate the Chip Select (CS) input of each UM82C59A-2.

The cascade lines of the Master UM82C59A-2 are activated only for slave inputs, non slave inputs leave the cascade line inactive (low).

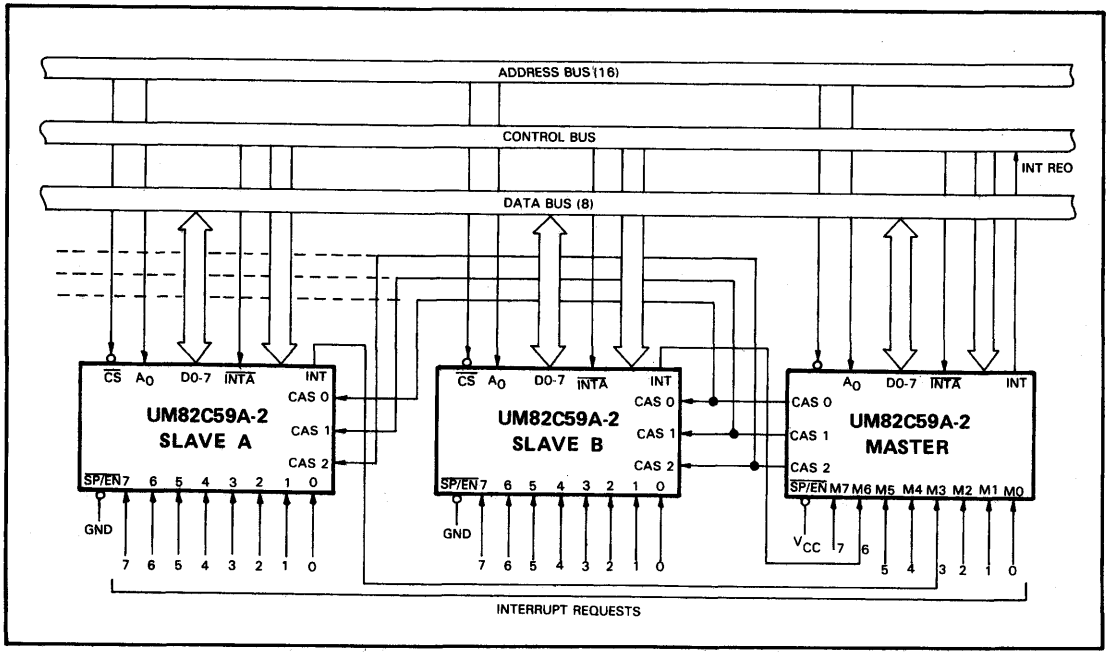


Figure 11. Cascading the UM82C59A-2

UMC

UM82C84AE

CMOS Clock Generator and Driver

Features

- Generates the system clock for CMOS or NMOS microprocessors
- Up to 25 MHz operation
- Uses a parallel mode crystal circuit or external frequency source
- Provides ready synchronization
- Generates system reset output from Schmitt Trigger input
- Capable of clock synchronization with other 8284A
- TTL compatible inputs/outputs
- Very low power consumption
- Single +5V power supply

General Description

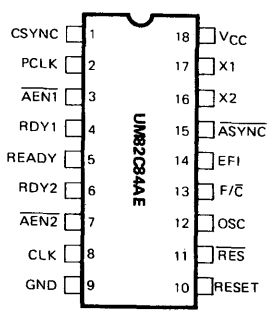
The UM82C84AE is a high performance CMOS clock generator-driver which is designed to service the requirements of both CMOS and NMOS microprocessors such as the 80C86, 80C88, 8086 and the 8088. The chip contains a crystal controlled oscillator, a divide-by-three counter and complete "Ready" synchronization and reset logic.

Static CMOS circuit design permits operation with an external frequency source from DC to 25MHz. Crystal controlled operation to 25MHz is guaranteed with the use of a parallel, fundamental mode crystal and two small load capacitors.

All inputs (except X1, X2 and $\overline{RES}$) are TTL compatible with a V_{IH} of 2.0 volts over the industrial temperature and voltage ranges.

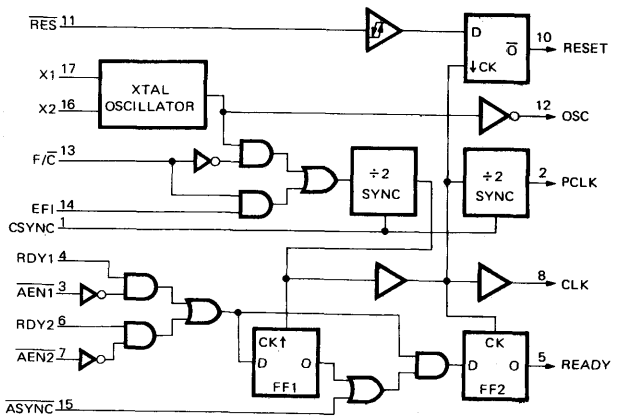
Power consumption is a fraction of that of the equivalent bipolar circuits. This speed-power characteristic of CMOS permits the designer to custom tailor his system design with respect to power and/or speed requirements.

Pin Configuration



Control Pin	Logic 1	Logic 0
F/$\overline{C}$	External Clock	Crystal Drive
$\overline{RES}$	Normal	Reset
RDY1 RDY2	Bus Ready	Bus not Ready
$\overline{AEN1}$ $\overline{AEN2}$	Address Disabled	Address Enabled
$\overline{ASYNC}$	2 Stage Ready Synchronization	1 Stage Ready Synchronization

Block Diagram



Absolute Maximum Ratings*

Supply Voltage . . . . . +8.0 Volts
Operating Voltage Range . . . . . +4V to +7V
Applied Voltage on Any Pin
V_{IN} . . . . . GND −0.3V to V_{CC}0.3V
Ambient Temperature Under Bias T_A . . . . . 0°C to +70°C
Storage Temperature Range
T_{STG} . . . . . −65°C to +150°C
Maximum Power Dissipation . . . . . 1 Watt

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

V_{CC} = 5.0V ± 10% T_A = 0°C to +70°C

Symbol	Parameter	Min.	Max.	Unit	Conditions
V_{IH}	Logic One Input Voltage	2.0		V	
V_{IL}	Logic Zero Input Voltage		0.8	V	
V_{T+}	Reset Input High Voltage	0.7 V_{CC}		V	
V_{T+}-V_{T-}	Reset Input Hysteresis	0.2 V_{CC}			
V_{OH}	Logic One Output Voltage	V_{CC}-0.4		V	I_{OH} = -4.0mA for CLK output I_{OH} = -2.5mA for all others
V_{OL}	Logic Zero Output Voltage		0.4	V	I_{OL} = +4.0mA for CLK output I_{OL} = +2.5mA for for others
I_{CL}	Input Leakage Current	−1.0	1.0	μA	$0V < V_{IN} < V_{CC}$ except $\overline{ASYNC}$, X1-see note 1
I_{CC}	Power S Supply Current		40	mA	Crystal Frequency = 25MHz Outputs Open

Notes:
ASYNC pin includes an internal 17.5KΩ nominal pull-up resistor. For $\overline{ASYNC}$ input at GND, $\overline{ASYNC}$ input leakage current = 130μA nominal.
X1-crystal feedback input.

Capacitance

(T_A = 25°C. V_{CC} = GND=0V; V_{IN} =+5V or GND)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_{IN}*	Input Capacitance		5	pf	Freq. = 1 MHz

*This parameter is guaranteed and sampled, but not 100% tested

AC Characteristics

(T_A = 0°C to +70°C, V_{CC} = 5V ± 10%)

TIMING REQUIREMENTS

Symbol	Parameter	Min.	Max.	Unit	Conditions
tEHEL	External Frequency HIGH Time	13		ns	90%–90% V_{IN}
tELEH	External Frequency LOW Time	13		ns	10%–10% V_{IN}
tELEL	EFI Period	36		ns	
	XTAL Frequency	2.4	25	MHz	
tR1VCL	RDY1, RDY2 Active Setup to CLK	35		ns	ASYNC = HIGH
tR1VCH	RDY1, RDY2 Inactive Setup to CLK	35		ns	ASYNC= LOW
tR1VCL	RDY1, RDY2 Inactive Setup to CLK	35		ns	
tCLR1X	RDY1, RDY2 Hold to CLK	0		ns	
tAYVCL	ASYNC Setup to CLK	50		ns	
tCLAYX	ASYNC Hold to CLK	0		ns	
tA1VR1V	AEN1, AEN2 Setup to RDY1, RDY2	15		ns	
tCLA1X	AEN1, AEN2 Hold to CLK	0		ns	
tYHEN	CSYNC Setup to EFI	20		ns	
tEHYL	CSYNC Hold to EFI	20		ns	
tYHYL	CSYNC Width	2.tELEL		ns	
t_{I1HCL}	RES Setup to CLK	65		ns	(Note 2)
tCLI1H	RES Hold to CLK	20		ns	(Note 2)

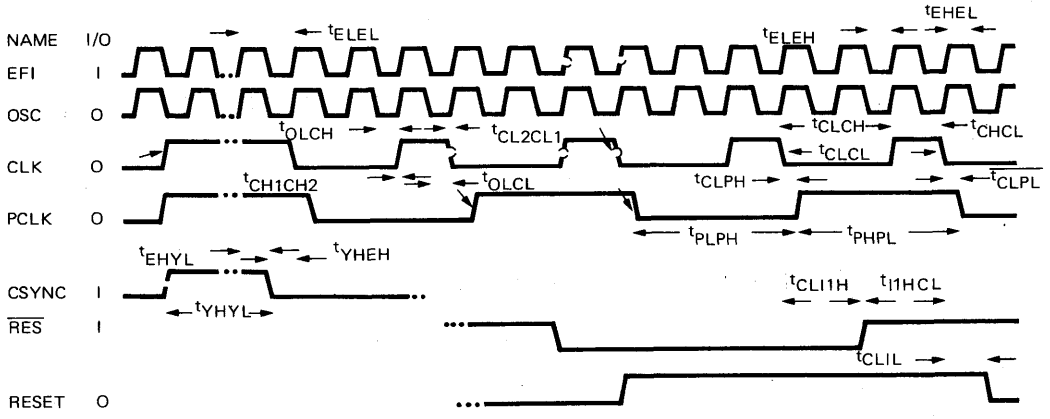
TIMING RESPONSES

Symbol	Parameter	Min.	Max.	Unit	Conditions
tCLCL	CLK Cycle Period	125		ns	
tCHCL	CLK HIGH Time	(1/3 tCLCL)+2.0		ns	Fig. 7 & Fig. 8
tCLCH	CLK LOW Time	(2/3 tCLCL)215.0		ns	Fig. 7 & Fig. 8
tCH1CH2	CLK Rise or Fall Time		10	ns	1.0V to 3.5V
tCL2CL1					
tPHPL	PCLK HIGH Time	tCLCL–20		ns	
tPLPH	PCLK LOW Time	tCLCL–20		ns	
tRYLCL	Ready Inactive to CLK (See note 4)	–8		ns	Fig. 8 & Fig. 10
tRYHCH	Ready Active to CLK (See note 3)	(2/3 tCLCL)–15.0		ns	Fig. 9 & Fig. 10
tCLIL	CLK to Reset Delay		40	ns	
tCLPH	CLK to PCLK HIGH Delay		22	ns	
tCLPL	CLK to PCLK LOW Delay		22	ns	
tOLCH	OSC to CLK HIGH Delay	–5	22	ns	
tOLCL	OSC to CLK LOW Delay	2	35	ns	

Notes:

1. Output signals switch between V_{OH} and V_{OL} unless otherwise specified.
2. Setup and hold necessary only to guarantee recognition at next clock.
3. Applies only to T3 TW states.
4. Applies only to T2 states.
5. All timing delays are measured at 1.5 volts unless otherwise noted.
6. Input signals must switch between V_{IL} max–.4 V_{OH} and V_{IH} min +.4 volts in 15ns unless otherwise specified.

Timing Waveforms



Note: All timing measurements are made at 1.5 volts, unless otherwise noted.

Figure 2. Waveforms for Clocks and Reset Signals

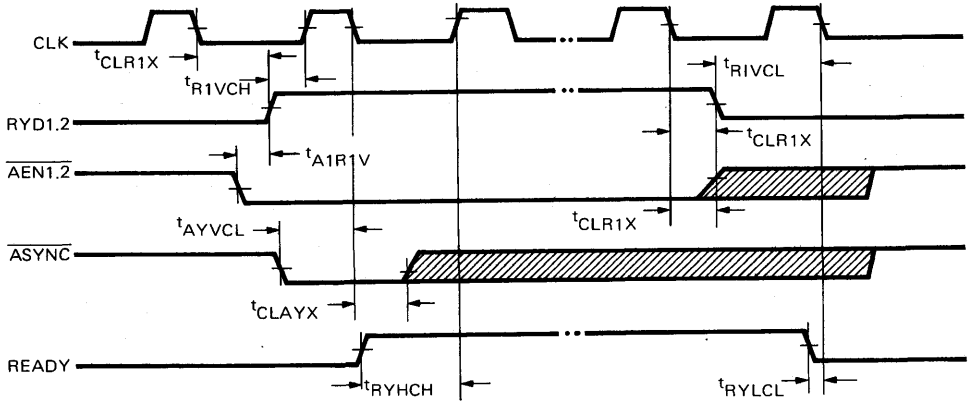


Figure 3. Waveforms for Ready Signals (For Asynchronous Devices)

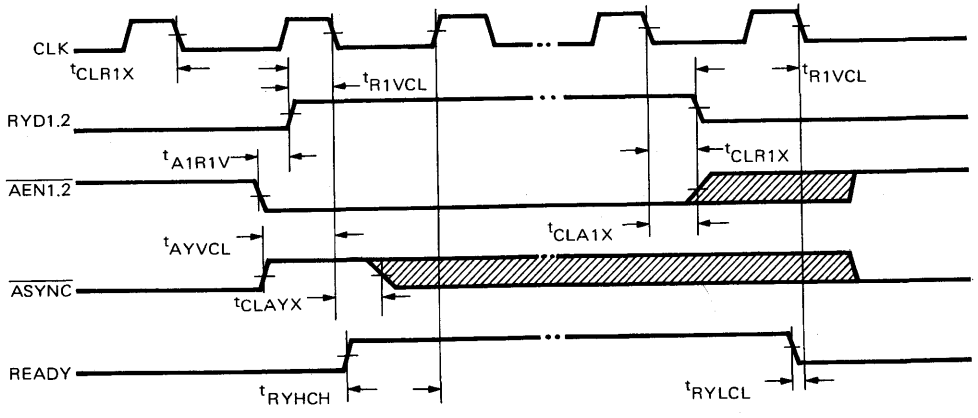


Figure 4. Waveforms for Ready Signals (For Synchronous Devices)

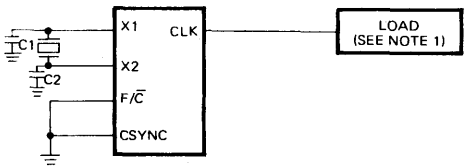


Figure 5. Clock High and Low Time (Using X1, X2)

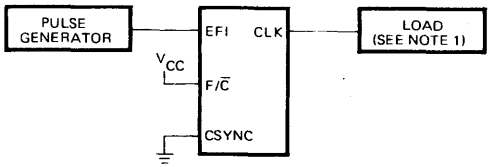


Figure 6. Clock High and Low Time (Using EFI)

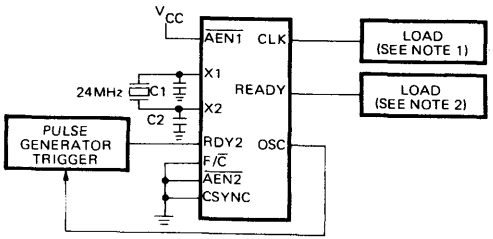


Figure 7. Ready to Clock (Using X1, X2)

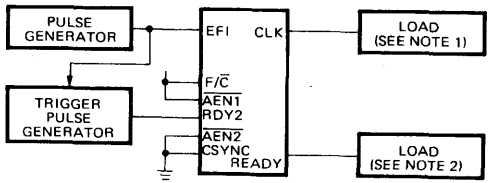
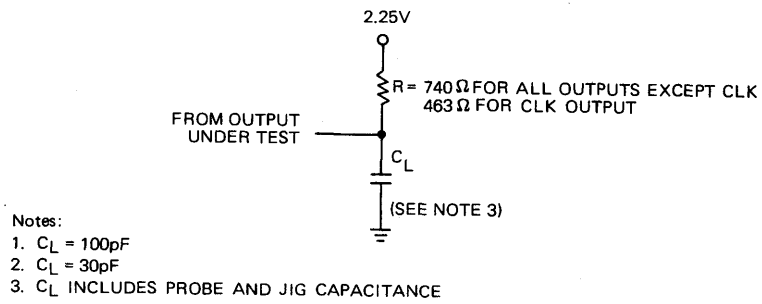


Figure 8. Ready to Clock (Using EFI)



Notes:
1. C_L = 100pF
2. C_L = 30pF
3. C_L INCLUDES PROBE AND JIG CAPACITANCE

Figure 9. Test Load Measurement Conditions

Table 1. Crystal Specifications

Parameter	Typical Crystal
Frequency	2.4–25MHz, Fundamental, "AT" cut
Type of Operation	Parallel
Unwanted Modes	–6db (Min)
Load Capacitance	18–32pf

Pin Description

Symbol	I/O	Description
$\overline{AEN1}$, $\overline{AEN2}$	I	ADDRESS ENABLE: $\overline{AEN}$ is an active LOW signal. $\overline{AEN}$ serves to qualify its respective Bus Ready Signal (RYD1 or RDY2). $\overline{AEN1}$ validates RDY1 while $\overline{AEN2}$ validates RDY2. Two AEN signal inputs are useful in system configurations which permit the processor to access two Multi-Master System Buses. In non Multi-Master configurations, the $\overline{AEN}$ signal inputs are tied true (LOW).
RDY1, RDY2	I	BUS READY (Transfer Complete). RDY is an active HIGH signal which is an indication from a device located on the system data bus that data has been received, or is available. RDY1 is qualified by AEN1 while RDY2 is qualified by AEN2.
$\overline{ASYNC}$	I	READY SYNCHRONIZATION SELECT: $\overline{ASYNC}$ is an input which defines the synchronization mode of the READY logic. When $\overline{ASYNC}$ is low, two stages of READY synchronization are provided. When $\overline{ASYNC}$ is left open or HIGH a single stage of READY synchronization is provided.
READY	O	READY: READY is an active HIGH signal which is the synchronized RDY signal input. READY is cleared after the guaranteed hold time to the processor has been met.
X1, X2	I	CRYSTAL IN: X1 and X2 are the pins to which a crystal is attached. The crystal frequency is 3 times the desired processor clock frequency.
F/$\overline{C}$	I	FREQUENCY/CRYSTAL SELECT: F/$\overline{C}$ is a strapping option. When strapped LOW, F/$\overline{C}$ permits the processor's clock to be generated by the crystal. When F/$\overline{C}$ is strapped HIGH, CLK is generated from the EFI input.
EFI	I	EXTERNAL FREQUENCY IN: When F/$\overline{C}$ is strapped HIGH, CLK is generated from the input frequency appearing on this pin. The input signal is a square wave 3 times the frequency of the desired CLK output.
CLK	O	PROCESSOR CLOCK: CLK is the clock output used by the processor and all devices which directly connect to the processor's local bus. CLK has an output frequency which is 1/3 of the crystal of EFI input frequency and a 1/3 duty cycle.
PCLK	O	PERIPHERAL CLOCK: PCLK is a peripheral clock signal whose output frequency is 1/2 that of CLK and has a 50% duty cycle.
OSC	O	OSCILLATOR OUTPUT: OSC is the output of the internal oscillator circuitry. Its frequency is equal to that of the crystal.
$\overline{RES}$	I	RESET IN: $\overline{RES}$ is an active LOW signal which is used to generate RESET. The UM82C84AE provides a Schmitt Trigger input so that an RC connection can be used to establish the power-up reset of proper duration.
RESET	O	RESET: RESET is an active HIGH signal which is used to reset the 80C86 family processors. Its timing characteristics are determinded by $\overline{RES}$.
CSYNC	I	CLOCK SYNCHRONIZATION: CSYNC is an active HIGH signal which allows multiple UM82C84AEs to be synchronized to provide clocks that are in phase. When CSYNC is HIGH the internal counters are reset. When CSYNC goes LOW the internal counters are allowed to resume counting. CSYNC needs to be externally synchronized to EFI. When using the internal oscillator CSYNC should be hardwired to ground.
GND		Ground
V_{CC}		+5V supply

Functional Description

Oscillator

The oscillator circuit of the UM82C84AE is designed primarily for use with an external parallel resonant fundamental mode crystal from which the basic operating frequency is derived.

The crystal frequency should be selected at three times the required CPU clock. X1 and X2 are the two crystal input connections. For the most stable operation of the oscillator (OSC) output circuit, two capacitors (C1 = C2) as shown in the waveform figures are recommended. The output of the oscillator is buffered and brought out on OSC so that other system timing signals can be derived from this stable, crystal-controlled source. Capacitors C1, C2 are chosen such that their combined capacitance:

$$CT = \frac{C1 \cdot C2}{C1+C2} \quad \text{(Including stray capacitance)}$$

matches the load capacitance as specified by the crystal manufacturer. This insures operation within the frequency tolerance specified by the crystal manufacturer.

Clock Generator

The clock generator consists of a synchronous divide-by-three counter with a special clear input that inhibits the counting. This clear input (CSYNC) allows the output clock to be synchronized with an external event (such as another UM82C84AE clock). It is necessary to synchronize the CSYNC input to the EFI clock external to the UM82C84AE. This is accomplished with two flip-flops. The counter output is a 33% duty cycle clock at one-third the input frequency.

The F/$\overline{C}$ input is a strapping pin that selects either the crystal oscillator or the EFI input as the clock for the –3 counter. If the EFI input is selected as the clock source, the oscillator section can be used independently for another clock source*. Output is taken from OSC.

Clock Outputs

The CLK output is a 33% duty cycle clock driver designed to drive the 80C86, 80C88 processors directly. PCLK is a peripheral clock signal whose output frequency is 1/2 that of CLK. PCLK has a 50% duty cycle.

Reset Logic

The reset logic provides a Schmitt Trigger input (RES) and a synchronizing flip-flop to generate the reset timing. The reset signal is synchronized to the falling edge of CLK. A simple RC network can be used to provide power-on reset by utilizing this function of the UM82C84AE. Wave-forms for clocks and reset signals are illustrated in Fig. 2.

Ready Synchronization

Two READY inputs (RDY1, RDY2) are provided to accommodate two system buses. Each input has a qualifier ($\overline{AEN1}$ and $\overline{AEN2}$, respectively). The $\overline{AEN}$ signals validate their respective RDY signals. If a Multi-Master system is not being used the $\overline{AEN}$ pin should be tied LOW.

Synchronization is required for all asynchronous active-going edges of either RDY input to guarantee that the RDY setup and hold times are met. Inactive-going edges of RDY in normally ready systems do not require synchronization but must satisfy RDY setup and hold as a matter of proper system design.

The $\overline{ASYNC}$ input defines two modes of READY synchronization operation.

When $\overline{ASYNC}$ is LOW, two stages of synchronization are provided for active READY input signals. Positive-going asynchronous READY inputs will first be synchronized to flip-flop, one at the rising edge of CLK (requiring a setup time tR1VCH) and then synchronized to flip-flop two at the next falling edge of CLK, after which time the READY output will go active (HIGH). Negative-going asynchronous READY inputs will be synchronized directly to flip-flop two at the falling edge of CLK, after which time the READY output will go inactive. This mode of operation is intended for use by asynchronous (normally not ready) devices in the system which cannot be guaranteed by design to meet the required RDY setup timing, tR1VCL, on each bus cycle.

When $\overline{ASYNC}$ is high or left open, the first READY flip-flop is bypassed in the READY synchronization logic. READY inputs are synchronized by flip-flop two on the falling edge of CLK before they are presented to the processor. This mode is available for synchronous devices that can be guaranteed to meet the required RDY setup time.

$\overline{ASYNC}$ can be changed on every bus cycle to select the appropriate mode of synchronization for each device in the system.

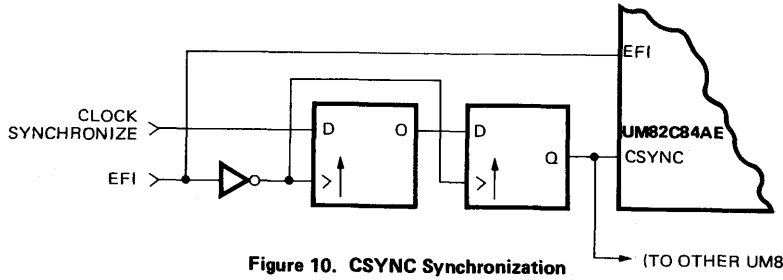


Figure 10. CSYNC Synchronization

*Note: If EFI input is used, then crystal input X1 must be tied to V_{CC} or GND and X2 should be left open. If the crystal inputs are used, then EFI should be tied to V_{CC} or GND.

UMC

UMC

UM82152

ADVANCED PRODUCT DESCRIPTION

Cache Controller

Features

- Controls 32-kB, 4-way, set-associative cache
- Available in 16-MHz, 20-MHz, and 25-MHz speeds
- Direct interface to the 80386
- Direct interface to industry-standard 8K x 8 SRAMs:
  45 ns for 16-MHz systems
  35 ns for 20-MHz systems
  25 ns for 25-MHz systems
- Full 32-bit addressability for 4-GB memory support.
- Cache coherency support
- Software cache invalidation
- On-chip programmable noncached regions
- Write buffer support
- Gate A20 support
- 1.5 micron CMOS technology
- 84-lead PLCC, JEDEC standard package
- Pin and functionally identical to A38152*

General Description

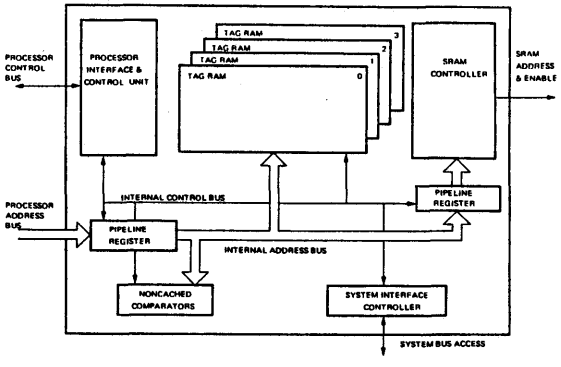
The UM82152 is a high-performance cache controller for Intel 80386 based systems and provides high levels of integration and functionality. It interfaces directly to the 80386; no additional support logic is required. A complete 32-kilobyte cache can be designed with just one UM82152 and four 8K by 8-bit static RAMs.

The UM82152 architecture enables easy design-in with current speed versions of the 80386, and simple migration to faster version processors with no alteration to system or memory design.

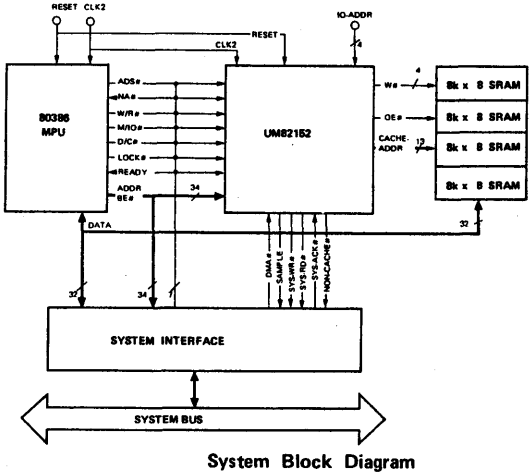
The 80386, operating in pipelined mode with the UM82152, runs with zero wait states during a cache hit (requested data is present in cache). If the data is not present (cache miss), it is fetched from main memory by the UM82152. This approach yields the high-speed performance of fast SRAMs for code and data most frequently used, while providing design economies (such as board space savings and lower component costs) by storing infrequently used code and data in slower dynamic RAM (with cycle times greater than 125 nanoseconds) that can be located in large memory banks either on-board or off-board.

The reduced system bus traffic inherent in the UM82152 implementation produces system performance gains by freeing the bus for use by other devices.

Block Diagrams



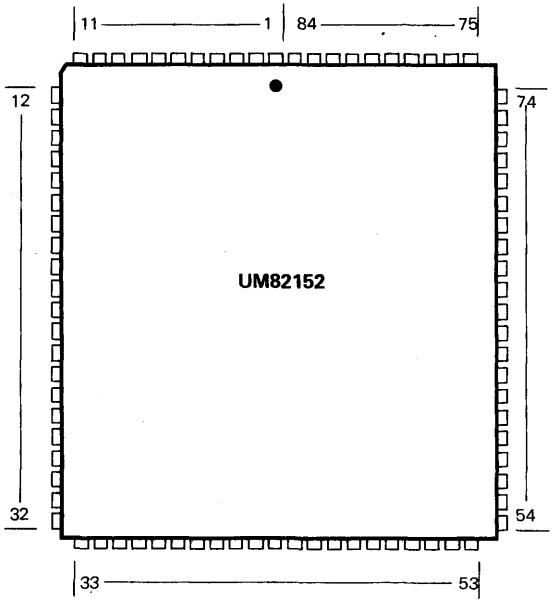
UM82152 Internal Configuration



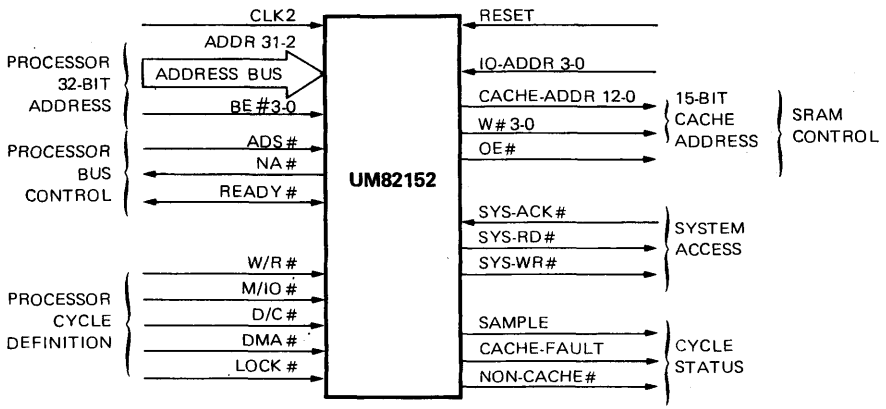
System Block Diagram

*A38152 is Austek's cache controller for 25 MHz 386 AT system.

Pin Configuration



Pin No	Signal	Pin No	Signal	Pin No	Signal
1	GND	29	CACHE-ADDR10	57	ADDR16
2	ADDR2	30	CACHE-ADDR9	58	ADDR17
3	BE0#	31	CACHE-ADDR8	59	ADDR18
4	BE1#	32	CACHE-ADDR7	60	ADDR19
5	BE2#	33	GND	61	ADDR20
6	BE3#	34	ADDR12	62	ADDR21
7	W/R#	35	ADDR11	63	ADDR22
8	CACHE-ADDR6	36	ADDR10	64	GND
9	CACHE-ADDR5	37	ADDR9	65	ADDR23
10	CACHE-ADDR4	38	ADDR8	66	ADDR24
11	CACHE-ADDR3	39	ADDR7	67	ADDR25
12	CACHE-ADDR2	40	ADS#	68	ADDR26
13	GND	41	V_{CC}	69	ADDR27
14	SYS-WR#	42	CLK2	70	ADDR28
15	SYS-RD#	43	GND	71	ADDR29
16	V_{CC}	44	V_{CC}	72	ADDR30
17	SYS-ACK#	45	RESET	73	ADDR31
18	OE#	46	SAMPLE	74	IO-ADDR3
19	W3#	47	NON-CACHE#	75	V_{CC}
20	W2#	48	NA#	76	IO-ADDR2
21	W1#	49	LOCK#	77	IO-ADDR1
22	W0#	50	DMA#	78	IO-ADDR0
23	CACHE-ADDR1	51	READY#	79	D/C#
24	CACHE-ADDR0	52	CACHE-FAULT	80	M/IO#
25	GND	53	ADDR13	81	ADDR6
26	CACHE-ADDR12	54	V_{CC}	82	ADDR5
27	V_{CC}	55	ADDR14	83	ADDR4
28	CACHE-ADDR11	56	ADDR15	84	ADDR3



UM82152 Signals

Pin Description

Pin No.	Symbol	I/O	Description
42	CLK2	I	Clock. Clock input.
45	RESET	I	Reset. Resets the microcache to a known state.
74, 76~78	IO-ADDR	I	Chip I/O Address. Address pins to locate the controller in the I/O space of the CPU.
2, 34~39, 53, 55~63, 65~73, 81~84	ADDR	I	Address Bus. The 30 physical address pins from the CPU.
3~6	BE#	I	Byte Enable. The 4 byte-enable pins from the CPU.
40	ADS#	I	Address Status. Direct connection from the CPU. Initiates a valid bus cycle.
48	NA#	O	Next Address. Direct connection to the CPU. Requests the CPU to use address pipelining.
51	READY#	I/O	Ready. Direct to the CPU. Indicates completion of the current bus cycle. This signal is bidirectional as it will also be driven by the system interface.
7	W/R#	I	Write/Read. Direct connection from the CPU. Indicates the type of CPU bus cycle, either write or read.
80	M/IO#	I	Memory/Input, Output. Direct connection from the CPU. Indicates the type of CPU bus cycle, either memory or I/O.
79	D/C#	I	Data/Control. Direct connection from the CPU. Indicates the type of CPU bus cycle, either data or control.
50	DMA#	I	DMA Cycle. Indicates that the cycle occurring is due to DMA activity on the system bus. Cache coherency is maintained by clearing any matching entries from the cache.
49	LOCK#	I	Lock. Direct connection from the CPU. When asserted indicates the current cycle is locked, exclusive access must be granted to the memory location addressed until LOCK# is negated. For cache coherency reasons, any matching entries are cleared from the cache.
17	SYS-ACK#	I	System Transfer Acknowledge. Control input from the system interface to acknowledge completion of read and write transfers to the system.
15	SYS-RD#	O	System Read. Control output to the system interface initiating a main memory read.
14	SYS-WR#	O	System Write. Control output to the system interface initating a main memory read.

Pin Description (Continued)

Pin No.	Symbol	I/O	Description
46	SAMPLE	O	Sample. Control output to the system interface to latch address and status information describing a processor bus cycle. SAMPLE is strobed at the end of a Tstate where the A38152 is either in a Ti state or a T2P state (when READY# will be asserted).
52	CACHE-FAULT	O	Cache Fault. A request to the system for an interrupt due to an internal error.
47	NON-CACHE#	O	Noncache Transfers. Indicates a data access within a noncached region. External decoding of addresses must be performed if necessary.
8-12, 23, 24, 26, 28~32	CACHE-ADDR	O	Cache Memory Address Bus. The physical address pins to the cache RAMs.
19~22	W#	O	Write Enable. Indicates a write to the cache RAMS when asserted and a read when negated. There is a W# line for cach byte in a word.
18	OE#	O	Output Enable. The data output enable for the cache RAMs.
16, 27, 41, 44 54, 75	V_{CC}		+5 Volt Supply
1, 13, 25, 33 43, 64	GND		Ground

UMC

UM8237AE/-4/-5

Programmable DMA Controller (DMAC)

Features

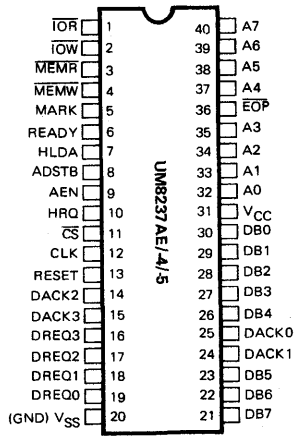
- Enable/Disable Control of Individual DMA Requests
- Four Independent DMA Channels
- Independent Autoinitialization of all Channels
- Memory-to-Memory Transfers
- Memory Block Initialization
- Single 5V power supply
- High performance: Transfers up to 1.6M Bytes/Second with 5 MHz UM8237AE-5
- Directly Expandable to any Number of Channels
- End of Process Input for Terminating Transfers
- Software DMA Requests
- Independent Polarity Control for DREQ and DACK Signals

General Description

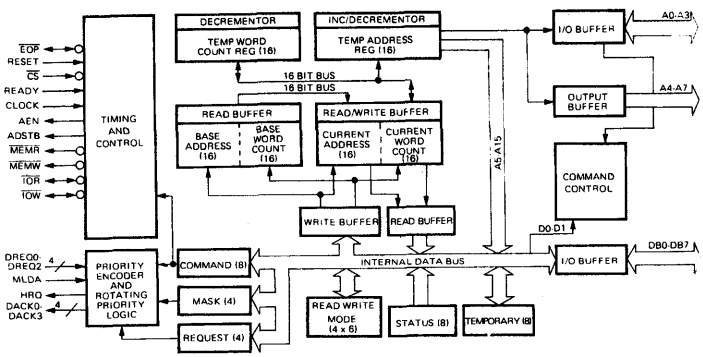
The UM8237AE/-4/-5 Direct Memory Access Controller (DMAC) is a peripheral interface circuit for microprocessor systems. It is designed to improve system performance by allowing external devices to directly transfer information from the system memory. Memory-to-memory transfer capability is also provided. The UM8237AE/-4/-5 offers a wide variety of programmable control features to enhance data throughput and system optimization and to allow dynamic reconfiguration under program control.

UM8237AE/-4/-5 is fabricated in Si-Gate NMOS process, with each channel having a full 64K address and word count capability.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Ambient Temperature under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . −65°C to + 150°C
Voltage on any Pin with Respect to Ground . . . . . −0.5 to 7V
Power Dissipation . . . . . 1.5 Watt

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

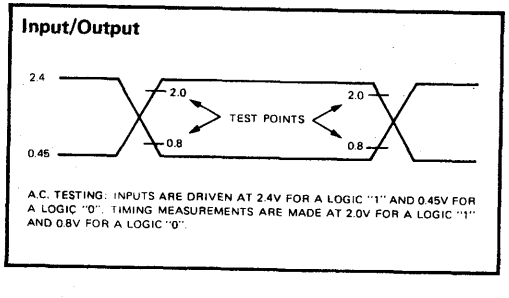
DC Electrical Characteristics (T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%, V_{SS} = 0V)

Symbol	Parameter	Min.	Typ.(1)	Max.	Unit	Test Conditions
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = −200 μA
		3.3			V	I_{OH} = −100 μA (HRQ Only)
V_{OL}	Output LOW Voltage			0.45	V	I_{OL} = 2.0 mA (data bus) I_{OL} = 3.2 mA (other outputs)
V_{IH}	Input HIGH Voltage	2.0		V_{CC} + 0.5	V	
V_{IL}	Input LOW Voltage	−0.5		0.8	V	
I_{LI}	Input Load Current			± 10	μA	$0V \leqslant V_{IN} \leqslant V_{CC}$
I_{LO}	Output Leakage Current			± 10	μA	$0.45V \leqslant V_{OUT} \leqslant V_{CC}$
I_{CC}	V_{CC} Supply Current		65	130	mA	T_A = +25°C
			75	150	mA	T_A = 0°C
C_O	Output Capacitance		4	8	pF	fc = 1.0 MHz, Inputs = 0V
C_I	Input Capacitance		8	15	pF	
C_{IO}	I/O Capacitance		10	18	pF	

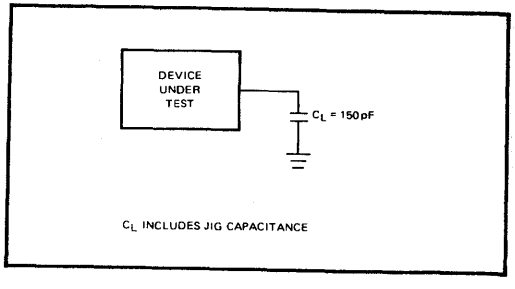
NOTES:

1. Typical values are for T_A = 25°C, nominal supply voltage and nominal processing parameters.
2. Input timing parameters assume transition times of 20 ns or less. Waveform measurement points for both input and output signals are 2.0V for HIGH and 0.8V for LOW, unless otherwise noted.
3. Output loading is 1 TTL gate plus 50 pF capacitance, unless otherwise noted.
4. The net $\overline{IOW}$ or $\overline{MEMW}$ Pulse width for normal write will be TCY-100 ns and for extended write will be 2TCY-100 ns. The net $\overline{IOR}$ or $\overline{MEMR}$ pulse width for normal read will be 2TCY-50 ns and for compressed read will be TCY-50 ns.
5. TDQ is specified for two different output HIGH levels. TDQ1 is measured at 2.0V. TDQ2 is measured at 3.3V. The value for TDQ2 assumes an external 3.3 kΩ pull-up resistor connected from HRQ to VCC.
6. DREQ should be held active until DACK is returned.
7. DREQ and DACK signals may be active high or active low. Timing diagrams assume the active high mode.
8. Output loading on the data bus is 1 TTL gate plus 100 pF capacitance.
9. Successive read and/or write operations by the external processor to program or examine the controller must be timed to allow at least 600 ns for the UM8237AE at least 500 ns for the UM8237AE-4 and at least 400 ns for the UM8237AE-5, as recovery time between active read or write pulses.
10. Parameters are listed in alphabetical order.
11. Pin 5 is an input that should always be at a logic high level. An internal pull-up resistor will establish a logic high when the pin is left floating. Alternatively, pin 5 may be tied to V_{CC}.

AC Testing Input, Output Waveform



AC Testing Load Circuit



PC Mainboard

AC Characteristics—DMA (master) Mode

(T_A = 0°C to 70°C, V_{CC} = +5V ± 5%, V_{SS} = 0V)

Symbol	Parameter	8237AE		8237AE-4		8237AE-5		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
TAEL	AEN HIGH from CLK LOW (S1) Delay Time		300		225		200	ns
TAET	AEN LOW from CLK HIGH (S1) Delay Time		200		150		130	ns
TAFAB	ADR Active to Float Delay from CLK HIGH		150		120		90	ns
TAFC	$\overline{READ}$ or $\overline{WRITE}$ Float from CLK HIGH		150		120		120	ns
TAFDB	DB Active to Float Delay from CLK HIGH		250		190		170	ns
TAHR	ADR from $\overline{READ}$ HIGH Hold Time	TCY-100		TCY-100		TCY-100		ns
TAHS	DB from ADSTB LOW Hold Time	50		40		30		ns
TAHW	ADR from $\overline{WRITE}$ HIGH Hold Time	TCY-50		TCY-50		TCY-50		ns
TAK	DACK Valid from CLK LOW Delay Time (Note 7)		250		220		170	ns
	$\overline{EOP}$ HIGH from CLK HIGH Delay Time		250		190		170	ns
	$\overline{EOP}$ LOW to CLK HIGH Delay Time		250		190		100	ns
TASM	ADR Stable from CLK HIGH		250		190		170	ns
TASS	DB to ADSTB LOW Setup Time	100		100		100		ns
TCH	Clock HIGH Time (Transitions ≤ 10 ns)	120		100		80		ns
TCL	Clock LOW Time (Transitions ≤ 10 ns)	150		110		68		ns
TCY	CLK Cycle Time	320		250		200		ns
TDCL	CLK HIGH to $\overline{READ}$ or $\overline{WRITE}$ LOW Delay (Note 4)		270		200		190	ns
TDCTR	$\overline{READ}$ HIGH from CLK HIGH (S4) Delay Time (Note 4)		270		210		190	ns
TDCTW	$\overline{WRITE}$ HIGH from CLK HIGH (S4) Delay Time (Note 4)		200		150		130	ns
TDQ1	HRQ Valid from CLK HIGH Delay Time (Note 5)		160		120		120	ns
TDQ2			250		190		120	ns
TEPS	$\overline{EOP}$ LOW from CLK LOW Setup Time	60		45		40		ns
TEPW	$\overline{EOP}$ Pulse Width	300		225		220		ns
TFAAB	ADR Float to Active Delay from CLK HIGH		250		190		170	ns
TFAC	$\overline{READ}$ or $\overline{WRITE}$ Active from CLK HIGH		200		150		150	ns
TFADB	DB Float to Active Delay from CLK HIGH		300		225		200	ns
THS	HLDA Valid to CLK HIGH Setup Time	100		75		75		ns
TIDH	Input Data from $\overline{MEMR}$ HIGH Hold Time	0		0		0		ns
TIDS	Input Data to $\overline{MEMR}$ HIGH Setup Time	250		190		170		ns
TODH	Output Data from $\overline{MEMW}$ HIGH Hold Time	20		20		10		ns
TODV	Output Data Valid to $\overline{MEMW}$ HIGH	200		125		125		ns
TQS	DREQ to CLK LOW (S1, S4) Setup Time (Note 7)	0		0		0		ns
TRH	CLK to READY LOW Hold Time	20		20		20		ns
TRS	READY to CLK LOW Setup Time	100		60		60		ns
TSTL	ADSTB HIGH from CLK HIGH Delay Time		200		150		130	ns
TSTT	ADSTB LOW from CLK HIGH Delay Time		140		110		90	ns

AC Characteristics—Peripheral (Slave) Mode

(T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%, V_{SS} = 0V)

Symbol	Parameter	8237AE		8237AE-4		8237AE-5		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
TAR	ADR Valid or $\overline{CS}$ LOW to $\overline{READ}$ LOW	50		50		50		ns
TAW	ADR Valid to $\overline{WRITE}$ HIGH Setup Time	200		150		150		ns
TCW	CS LOW to $\overline{WRITE}$ HIGH Setup Time	200		150		150		ns
TDW	Data Valid to $\overline{WRITE}$ HIGH Setup Time	200		150		150		ns
TRA	ADR or CS Hold from $\overline{READ}$ HIGH	0		0		0		ns
TRDE	Data Access from $\overline{READ}$ LOW (note 8)		200		200		140	ns
TRDF	DB Float Delay from $\overline{READ}$ HIGH	20	100	20	100	0	70	ns
TRSTD	Power Supply HIGH to RESET LOW Setup Time	500		500		500		ns
TRSTS	RESET to First $\overline{IOWR}$	2TCY		2TCY		2TCY		ns
TRSTW	RESET Pulse Width	300		300		300		ns
TRW	$\overline{READ}$ Width	300		250		200		ns
TWA	ADR from $\overline{WRITE}$ HIGH Hold Time	20		20		20		ns
TWC	CS HIGH from WRITE HIGH Hold Time	20		20		20		ns
TWD	Data from $\overline{WRITE}$ HIGH Hold Time	30		30		30		ns
TWWS	Write Width	200		200		160		ns

Pin Description

Pin No.	Symbol	I/O	Description
31	V_{CC}		+5 volt supply.
20	V_{SS}		Ground.
12	CLK	I	Clock input controls the internal operations of the UM8237AE/-4/-5 and its rate of data transfer. The input may be driven at up to 5 MHz for the UM8237AE—5.
11	$\overline{CS}$	I	Chip Select is an active low input used to select the UM8237AE/-4/-5 as an I/O device during the Idle cycle. This allows CPU communication on the data bus.
13	RESET	I	Reset is an active high input which clears the Command, Status, Request and Temporary registers. It also clears the first/last flip-flop and sets the Mask register. Following a Reset the device is in the Idle cycle.
6	READY	I	Ready is an input used to extend the memory read and write pulses from the UM8237AE/-4/-5 to accommodate slow memories or I/O peripheral devices. Ready must not make transitions during its specified setup/hold time.
7	HLDA	I	The active high Hold Acknowledge from the CPU indicates that it has relinquished control of the system busses.
5	MARK	I	This pin has no use for the UM8237AE/-4/-5, but should always be tied high.
19, 18 17, 16	DREQ0-DREQ3	I	The DMA Request lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. In fixed Priority, DREQ0 has the highest priority and DREQ3 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of a DREQ signal. Polarity of DREQ is programmable. Reset intializes these lines to active high. DREQ must be maintained until the corresponding DACK goes active.

Pin Description (Continued)

Pin No.	Symbol	I/O	Description
30 ~ 26 23 ~ 21	DB0-DB7	I/O	The Data Bus lines are bidirectional three-state signals connected to the system data bus. The outputs are enabled in the Program condition during the I/O Read to output the contents of an Address register, a Status register, the Temporary register or a Word Count register to the CPU. The outputs are disabled and the inputs are read during and I/O Write cycle when the CPU is programming the UM8237AE/-4/-5 control registers. During DMA cycles the most significant 8 bits of the address are output onto the data bus to be strobed into an external latch by ADSTB. In memory-to-memory operations, data from the memory comes into the UM8237AE/-4/-5 on the data bus during the read-from-memory transfer. In the write-to-memory transfer, the data bus outputs place the data into the new memory location.
1	$\overline{IOR}$	I/O	I/O Read is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to read the control registers. In the Active cycle, it is an output control signal used by the UM8237AE/-4/-5 to access data from a peripheral during a DMA Write transfer.
2	$\overline{IOW}$	I/O	I/O Write is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to load information into the UM8237AE/-4/-5. In the Active cycle, it is an output control signal used by the UM8237AE/-4/-5 to load data to the peripheral during a DMA Read transfer.
36	$\overline{EOP}$	I/O	End of Process is an active low bidirectional signal. Information concerning the completion of DMA services is available at the bidirectional $\overline{EOP}$ pin. The UM8237AE/-4/-5 allows an external signal to terminate an active DMA service. This is accomplished by pulling the $\overline{EOP}$ input low with an external $\overline{EOP}$ signal. The UM8237AE/-4/-5 also generates a pulse when the terminal count (TC) for any channel is reached. This generates an $\overline{EOP}$ signal which is output through the $\overline{EOP}$ Line. The reception of $\overline{EOP}$, either internal or external, will cause the UM8237AE/-4/-5 to terminate the service, reset the request, and, if Autoinitialize is enabled, to write the base registers to the current registers of that channel. The mask bit and TC bit in the status word will be set for the currently active channel by $\overline{EOP}$ unless the channel is programmed for Autoinitialize. In that case, the mask bit remains clear. During memory-to-memory transfers, $\overline{EOP}$ will be output when the TC for channel 1 occurs. $\overline{EOP}$ should be tied high with a pull-up resistor if it is not used to prevent erroneous end of process inputs.
32 ~ 35	A0-A3	I/O	The four least significant address lines are bidirectional three-state signals. In the Idle cycle they are inputs and are used by the UM8237AE/-4/-5 to address the control register to be loaded or read. In the Active cycle they are outputs and provide the lower 4 bits of the output address.
37 ~ 40	A4-A7	O	The four most significant address lines are three-state outputs and provide 4 bits of address. These lines are enabled only during the DMA service.
10	HRQ	O	This is the Hold Request to the CPU and is used to request control of the system bus. If the corresponding mask bit is clear, the presence of any valid DREQ causes UM8237AE/-4/-5 to issue the HRQ. After HRQ goes active at least one clock cycle (TCY) must occur before HLDA goes active.
25, 24, 14, 15	DACK0-DACK3	O	DMA Acknowledge is used to notify the individual peripherals when one has been granted a DMA cycle. The sense of these lines is programmable. Reset initializes them to active low.

Pin Description (Continued)

Pin No.	Symbol	I/O	Description
9	AEN	O	Address Enable enables the 8-bit latch containing the upper 8 address bits onto the system address bus. AEN can also be used to disable other system bus drivers during DMA transfers. AEN is active HIGH.
Address Strobe	$\overline{\text{ADSTB}}$	O	The active high, Address Strobe is used to strobe the upper address byte into an external latch.
3	$\overline{\text{MEMR}}$	O	The Memory Read signal is an active low, three-state output used to access data from the selected memory location during a DMA Read or a memory-to memory transfer.
4	$\overline{\text{MEMW}}$	O	The Memory Write is an active low, three-state output used to write data to the selected memory location during a DMA Write or a memory-to-memory transfer.

Functional Description

The UM8237AE/-4/-5 block diagram includes the major logic blocks and all of the internal registers. The data interconnection paths are also shown. Not shown are the various control signals between the blocks. The UM8237AE/-4/-5 contains 344 bits of internal memory in the form of registers. Figure 1 lists these registers by name and shows the size of each. A detailed description of the registers and their functions can be found under Register Description.

The UM8237AE/-4/-5 contains three basic blocks of control logic. The Timing Control block generates internal timing and external control signals for the UM8237AE/-4/-5. The Program Command Control block decodes the various commands given to the UM8237AE/-4/-5 by the microprocessor prior to servicing a DMA Request. It also decodes the Mode Control word used to select the type of DMA during the servicing. The Priority Encoder block resolves priority contention between DMA channels requesting service simultaneously.

The Timing Control block derives internal timing from the clock input. In UM8237AE/-4/-5 systems this input will usually be the $\phi 2$ TTL clock from an 8224 or CLK from an 8085AH or 8284A. For 8085AH-2 systems above 3.9 MHz, the 8085 CLK (OUT) does not satisfy UM8237AE/-4/-5 clock LOW and HIGH time requirements. In this case, an external clock should be used to drive the UM8237AE/-4/-5.

Name	Size	Number
Base Address Registers	16 bits	4
Base Word Count Registers	16 bits	4
Current Address Registers	16 bits	4
Current Word Count Registers	16 bits	4
Temporary Address Register	16 bits	1
Temporary Word Count Register	16 bits	1
Status Register	8 bits	1
Command Register	8 bits	1
Temporary Register	8 bits	1
Mode Registers	6 bits	4
Mask Register	4 bits	1
Request Register	4 bits	1

Figure 1. UM8237AE/-4/-5 Internal Registers

DMA Operation

The UM8237AE/-4/-5 is designed to operate in two major cycles. These are called Idle and Active cycles. Each device cycle is made up of a number of states. The UM8237AE/-4/-5 can assume seven separate states, each composed of one full clock period. State 1 (S1) is the inactive state. It is entered when the UM8237AE/-4/-5 has no valid DMA requests pending. While in S1, the DMA controller is inactive but may be in the Program condition, being programmed by the processor. State S0 (S0) is the first state of a DMA service. The UM8237AE/-4/-5 has requested a hold but the processor has not yet returned an acknowledge. The UM8237AE/-4/-5 may still be programmed until it receives HLDA from the CPU. An acknowledge from the CPU will signal that DMA transfers may begin. S1, S2, S3 and S4 are the working states of the DMA service. If more time is needed to complete a transfer than is available with normal timing, wait states (SW) can be inserted between S2 or S3 and S4 by the use of the Ready line on the UM8237AE/-4/-5. Note that the data is transferred directly from the I/O device to memory (or vice versa) with $\overline{\text{IOR}}$ and $\overline{\text{MEMW}}$ (or $\overline{\text{MEMR}}$ and $\overline{\text{IOW}}$) being active at the same time. The data is not read into or driven out of the UM8237AE/-4/-5 in I/O-to-memory or memory-to-I/O DMA transfers.

Memory-to-memory transfers require a read-from and a write-to-memory to complete each transfer. The states, which resemble the normal working states, use two digit numbers for identification. Eight states are required for a single transfer. The first four states (S11, S12, S13, S14) are used for the read-from-memory half and the last four states (S21, S22, S23, S24) for the write-to-memory half of the transfer.

Idle Cycle

When no channel is requesting service, the UM8237AE/-4/-5 will enter the Idle cycle and perform "S1" states. In this cycle, the UM8237AE/-4/-5 will sample the DREQ lines every clock cycle to determine if any channel is requesting a DMA service. The device will also sample $\overline{CS}$, looking for an attempt by the microprocessor to write or read the internal registers of the UM8237AE/-4/-5. When $\overline{CS}$ is low and HLDA is low, the UM8237AE/-4/-5 enters the Program Condition. The CPU can now establish, change or inspect the internal definition of the part by reading from or writing to the internal registers. Address lines A0-A3 are inputs to the device and select which registers will be read or written. The $\overline{IOR}$ and $\overline{LOW}$ lines are used to select and time reads or writes. Due to the number and size of the internal registers, an internal flip-flop is used to generate an additional bit of address. This bit is used to determine the upper or lower byte of the 16-bit Address and Word Count registers. The flip-flop is reset by Master Clear or Reset. A separate software command can also reset this flip-flop.

Special software commands can be executed by the UM8237AE/-4/-5 in the Program Condition. These commands are decoded as sets of addresses with the $\overline{CS}$ and $\overline{IOW}$. The commands do not make use of the data bus. Instructions include Clear First/Last Flip-Flop and Master Clear.

Active Cycle

When the UM8237AE/-4/-5 is in the Idle cycle and a non-masked channel requests a DMA service, the device will output an HRQ to the microprocessor and enter the Active cycle. It is in this cycle that the DMA service will take place, in one of four modes:

Single Transfer Mode — In Single Transfer mode the device is programmed to make one transfer only. The word count will be decremented and the address decremented or incremented following each transfer. When the word count "rolls over" from zero to FFFFH, a Terminal Count (TC) will cause an Autoinitialize, if the channel has been programmed to do so.

DREQ must be held active until DACK becomes active in order to be recognized. If DREQ is held active throughout the single transfer, HRQ will go inactive and release the bus to the system. It will again go active and, upon receipt of a new HLDA, another single transfer will be performed, in 8080A, 8085AH, 8088, or 8086 systems this will ensure one full machine cycle execution between DMA transfers. Details of timing between the UM8237AE/-4/-5 and other bus control protocols will depend upon the characteristics of the microprocessor involved.

Block Transfer Mode — In Block Transfer mode the device is activated by DREQ to continue making transfers during the service until a TC, caused by word count going to FFFFH, or an external End of Process ($\overline{EOP}$) is encountered. DREQ need only be held active until DACK becomes active. Again, an Autoinitialization will occur at the end of the service if the channel has been programmed for it.

Demand Transfer Mode — In Demand Transfer mode the device is programmed to continue making transfers until a TC or external $\overline{EOP}$ is encountered or until DREQ goes inactive. Thus transfers may continue until the I/O device has exhausted its data capacity. After the I/O device has had a chance to catch up, the DMA service is re-established by means of a DREQ. During the time between services, when the microprocessor is allowed to operate, the intermediate values of address and word count are stored in the UM8237AE/-4/-5 Current Address and Current Word Count registers. Only an $\overline{EOP}$ can cause an Autoinitialize at the end of the service. $\overline{EOP}$ is generated either by TC or by an external signal.

Cascade Mode — This mode is used to cascade more than one UM8237AE/-4/-5 together for simple system expansion. The HRQ and HLDA signals from the additional UM8237AE/-4/-5 are connected to the DREQ and DACK signals of a channel of the initial UM8237AE/-4/-5. This allows the DMA requests of the additional device to propagate through the priority network circuitry of the preceding device. The priority chain is preserved and the new device must wait for its turn to acknowledge requests. Since the cascade channel of the initial UM8237AE/-4/-5 is used only for prioritizing the additional device, it does not output any address or control signals of its own. These could conflict with the outputs of the active channel in the added device. The UM8237AE/-4/-5 will respond to DREQ and DACK but all other outputs, except HRQ, will be disabled.

Figure 2 shows two additional devices cascaded into an initial device using two of the previous channels. This forms a two level DMA system. More UM8237AE/-4/-5 could be added at the second level by using the remaining channels of the first level. Additional devices can also be added by cascading into the channels of the second level devices, forming a third level.

Transfer Types

Each of the three active transfer modes can perform three different types of transfers. These are Read, Write and Verify. Write transfers move data from an I/O device to the memory by activating $\overline{MEMW}$ and $\overline{IOR}$. Read transfers move data from memory to an I/O device by activating $\overline{MEMR}$ and $\overline{IOW}$. Verify transfers are pseudo transfers. The UM8237AE/-4/-5 operates, as in Read or Write transfers, generating addresses, and responding to EOP, etc. However, the memory and I/O control lines all remain inactive. Verify mode is not permitted during memory to memory operations.

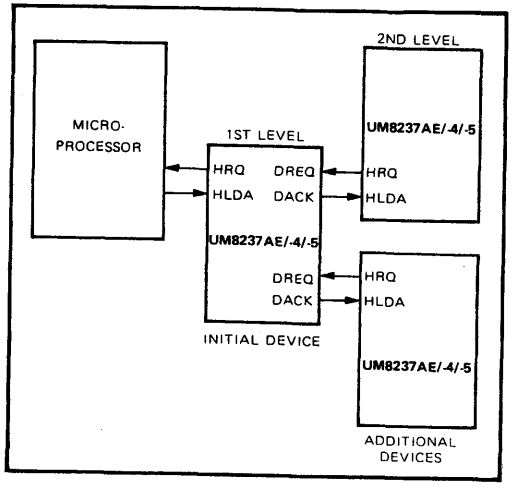


Figure 2. Cascaded UM8237AE/-4/-5

Memory-to-Memory — To perform block moves of data from one memory address space to another with a minimum of program effort and time, the UM8237AE/-4/-5 includes a memory-to-memory transfer feature. Programming a bit in the Command register selects channels 0 and 1 to operate as memory-to-memory transfer channels. The transfer is initiated by setting the software DREQ for channel 0. The UM8237AE/-4/-5 requests a DMA service in the normal manner. After HLDA is true, the device, using eightstate transfers in Block Transfer mode, reads data from the memory. The channel 0 Current Address register is the source for the address used and is decremented or incremented in the normal manner. The data byte read from the memory is stored in the UM8237AE/-4/-5 internal Temporary register. Channel 1 then writes the data from the Temporary register to memory using the address in its Current Address register and incrementing or decrementing it in the normal manner. The channel 1 Current Word Count is decremented. When the word count of channel 1 goes to FFFFH, a TC is generated causing an $\overline{EOP}$ output, terminating the service.

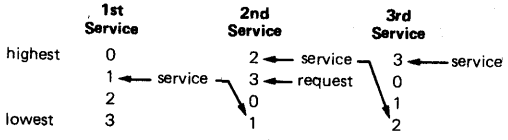
Channel 0 may be programmed to retain the same address for all transfers. This allows a single word to be written to a block of memory.

The UM8237AE/-4/-5 will respond to external $\overline{EOP}$ signals during memory-to-memory transfers. Data comparators in block search schemes may use this input to terminate the service when a match is found. The timing of memory-to-memory transfers is found in Figure 10. Memory-to-memory operations can be detected as an active AEN with no DACK outputs.

Autoinitialize — By programming a bit in the Mode register, a channel may be set up as an Autoinitialize channel. During Autoinitialize initialization, the original values of the Current Address and Current Word Count registers are automatically restored from the Base Address and Base Word count registers of that channel following $\overline{EOP}$.. The base registers are loaded simultaneously with the current registers by the microprocessor and remain unchanged throughout the DMA service. The mask bit is not set when the channel is in Autoinitialize. Following Autoinitialize, the channel is ready to perform another DMA service, without CPU intervention, as soon as a valid DREQ is detected.

Priority — The UM8237AE/-4/-5 has two types of priority encoding available as software selectable options. The first is Fixed Priority, which fixes the channels in priority order based upon the descending value of their number. The channel with the lowest priority is 3, followed by 2 and 1, and the highest priority channel, 0. After the recognition of any one channel for service, the other channels are prevented from interfering with that service until it is completed.

The second scheme is Rotating Priority. The last channel to get service becomes the lowest priority channel with the others rotating accordingly.



With Rotating Priority in a single chip DMA system, any device requesting service is guaranteed to be recognized after no more than three higher priority services have occurred. This prevents any one channel from monopolizing the system.

Compressed Timing — In order to achieve even greater throughput where system characteristics permit, the UM8237AE/-4/-5 can compress the transfer time to two clock cycles. From Figure 11 it can be seen that state S3 is used to extend the access time of the read pulse. By removing state S3, the read pulse width is made equal to the write pulse width and a transfer consists only of state S2 to change the address and state S4 to perform the read/write. S1 states will still occur when A8-A15 need updating (see Address Generation). Timing for compressed transfers is found in Figure 12.

Address Generation — In order to reduce pin count, the UM8237AE/-4/-5 multiplexes the eight higher order address bits on the data lines. State S1 is used to output the higher order address bits to an external latch, from which they may be placed on the address bus. The falling edge of Address Strobe (ADSTB) is used to load these bits from the data lines to the latch. Address Enable (AEN) is used to enable the bits onto the address bus through a threestate enable. The lower order address bits are output by the UM8237AE/-4/-5 directly. Lines A0-A7 should be connected to the address bus. Figure 9 shows the time relationships between CLK, AEN, ADSTB, DB0-DB7 and A0-A7.

During Block and Demand Transfer mode services, which include multiple transfers, the addresses generated will be sequential. For many transfers the data held in the external address latch will remain the same. This data

need change only when a carry or borrow from A7 to A8 takes place in the normal sequence of addresses. To save time and speed transfers, the UM8237AE/-4/-5 executes S1 states only when updating of A8-A15 in the latch is necessary. This means for long services, S1 states and Address Strobes may occur only once every 256 transfers, a savings of 255 clock cycles for each 256 transfers.

Register Description

Current Address Register – Each channel has a 16-bit Current Address register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the intermediate values of the address are stored in the Current Address register during the transfer. This register is written or read by the microprocessor in successive 8-bit bytes. It may also be reinitialized by an Autoinitialize back to its original value. Autoinitialize takes place only after an $\overline{EOP}$.

Current Word Register – Each channel has a 16-bit Current Word Count register. This register determines the number of transfers to be performed. The actual number of transfers will be one more than the number programmed in the Current Word Count register (i.e. programming a count of 100 will result in 101 transfers). The word count is decremented after each transfer. The intermediate value of the word count is stored in the register during the transfer. When the value in the register goes from zero to FFFFH, a TC will be generated. This register is loaded or read in successive 8-bit bytes by the microprocessor in the Program Condition. Following the end of a DMA service it may also be reinitialized, by an Autoinitialization, back to its original value. Autoinitialize can occur only when an $\overline{EOP}$ occurs. If it is not Autoinitialized, this register will have a count of FFFFH after TC.

Base Address and Base Word Count Register – Each channel has a pair of Base Address and Base Word Count registers. These 16-bit registers store the original value of their associated current registers. During Autoinitialize these values are used to restore the current registers to their original values. The base registers are written simultaneously with their corresponding current register in 8-bit bytes in the Program Condition by the microprocessor. These registers cannot be read by the microprocessor.

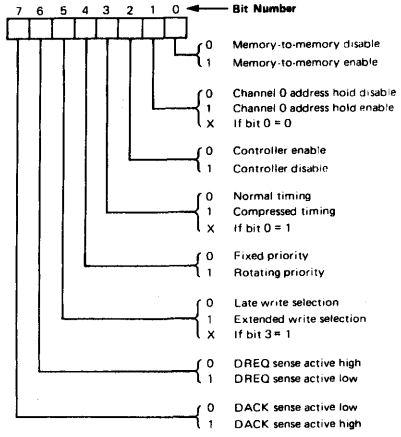
Command Register – This 8-bit register controls the operation of the UM8237AE/-4/-5. It is programmed by the microprocessor in the Program Condition and is cleared by Reset or a Master Clear instruction. The following table lists the functions of the command bits. See Figure 4 for address coding.

Mode Register – Each channel has a 6-bit Mode register associated with it. When the register is being written to by the microprocessor in the the Program Condition, bits 0 and 1 determine which channel Mode register is to be written.

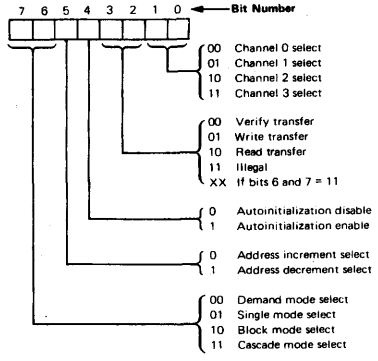
Request Register – The UM8237AE/-4/-5 can respond to requests for DMA service which are initiated by software as well as by a DREQ. Each channel has a request bit associated with it in the 4-bit Request register. These are nonmaskable and subject to prioritization by the Priority Encoder network. Each register bit is set or reset separately under software control, or is cleared upon generation of a TC or external $\overline{EOP}$. The entire register is cleared by a Reset. To set or reset a bit, the software loads the proper form of the data word. See Figure 3 for register address coding. In order to make a software request, the channel must be in Block Mode.

Mask Register – Each channel has associated with it a

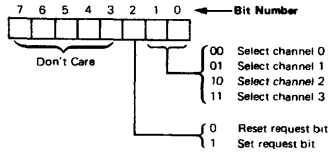
Command Register



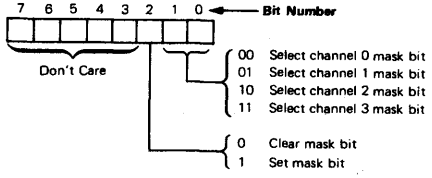
Mode Register



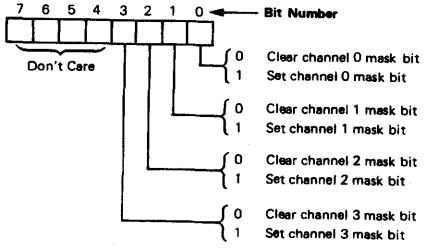
Request Register



mask bit which can be set to disable the incoming DREQ. Each mask bit is set when its associated channel produces an $\overline{EOP}$, if the channel is not programmed for Autoinitialize. Each bit of the 4-bit Mask register may also be set or cleared separately under software control. The entire register is also set by a Reset. This disables all DMA requests until a clear Mask register instruction allows them to occur. The instruction to separately set or clear the mask bits is similar in form to that used with the Request register. See Figure 3 for instruction addressing.



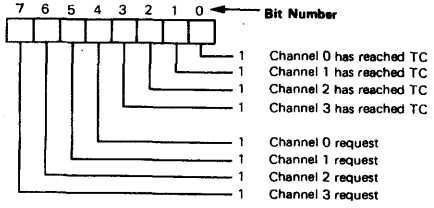
All four bits of the Mask register may also be written with a single command.



Register	Operation	Signals						
		$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A3	A2	A1	A0
Command	Write	0	1	0	1	0	0	0
Mode	Write	0	1	0	1	0	1	1
Request	Write	0	1	0	1	0	0	1
Mask	Set/Reset	0	1	0	1	0	1	0
Mask	Write	0	1	0	1	1	1	1
Temporary	Read	0	0	1	1	1	0	1
Status	Read	0	0	1	1	0	0	0

Figure 3. Definition of Register Codes

Status Register – The Status register is available to be read out of the UM8237AE/-4/-5 by the microprocessor. It contains information about the status of the devices at this point. This information includes which channels have reached a terminal count and which channels have pending DMA requests. Bits 0-3 are set every time a TC is reached by that channel or an external EOP is applied. These bits are cleared upon Reset and on each Status Read. Bits 4-7 are set whenever their corresponding channel is requesting service.



Temporary Register – The Temporary register is used to hold data during memory-to-memory transfers. Following the completion of the transfers, the last word moved can be read by the microprocessor in the Program Condition. The Temporary register always contains the last byte transferred in the previous memory-to-memory operation, unless cleared by a Reset.

Software Commands – These are additional special software commands which can be executed in the Program Condition. They do not depend on any specific bit pattern on the data bus. The two software commands are:

Clear First/Last Flip-Flop: This command is executed prior to writing or reading new address or word count information to the UM8237AE/-4/-5. This initializes the flip-flop to a known state so that subsequent accesses to register contents by the microprocessor will address upper and lower bytes in the correct sequence.

Master Clear: This software instruction has the same effect as the hardware Reset. The Command, Status, Request, Temporary, and Internal First/Last Flip-Flop registers are cleared and the Mask register is set. The UM8237AE/-4/-5 will enter the idle cycle.

Clear Mask Register: This command clears the mask bits of all four channels, enabling them to accept DMA requests.

Figure 4 lists the address codes for the software commands:

PROGRAMMING

The UM8237AE/-4/-5 will accept programming from the host processor any time that HLDA is inactive; this is true even if HRQ is active. The responsibility of the host is to assure that programming and HLDA are mutually exclusive. Note that a problem can occur if a DMA request occurs, on an unmasked channel while the UM8237AE/-4/-5 is being programmed. For instance, the CPU may be starting to reprogram the two byte Address register of channel 1 when channel 1 receives a DMA request. If the UM8237AE/-4/-5 is enabled (bit 2 in the command register is 0) and channel 1 is un-

Signals						Operation
A3	A2	A1	A0	$\overline{IOR}$	$\overline{IOW}$	
1	0	0	0	0	1	Read Status Register
1	0	0	0	1	0	Write Command Register
1	0	0	1	0	1	Illegal
1	0	0	1	1	0	Write Request Register
1	0	1	0	0	1	Illegal
1	0	1	0	1	0	Write Single Mask Register Bit
1	0	1	1	0	1	Illegal
1	0	1	1	1	0	Write Mode Register
1	1	0	0	0	1	Illegal
1	1	0	0	1	0	Clear Byte Pointer Flip/Flop
1	1	0	1	0	1	Read Temporary Register
1	1	0	1	1	0	Master Clear
1	1	1	0	0	1	Illegal
1	1	1	0	1	0	Clear Mask Register
1	1	1	1	0	1	Illegal
1	1	1	1	1	0	Write All Mask Register Bits

Figure 4. Software Command Codes

masked, a DMA service will occur after only one byte of the Address register has been reprogrammed. This can be avoided by disabling the controller (setting bit 2 in the command register) or masking the channel before programming any other registers. Once the programming is complete, the controller can be enabled/unmasked.

After power-up it is suggested that all internal locations, especially the Mode registers, be loaded with some valid value. This should be done even if some channels are unused.

Application Information

Figure 6 shows a convenient method for configuring a DMA system with the UM8237AE/-4/-5 controller and an 8080A/8085AH microprocessor system. The multi-mode DMA controller issues a HRQ to the processor whenever there is at least one valid DMA request from a peripheral device. When the processor replies with a HLDA signal, the UM8237AE/-4/-5 takes control of the address bus, the data bus and the control bus. The address for the first transfer operation comes out in two bytes – the least significant 8 bits on the eight address outputs and the most significiant 8 bits on the data bus. The contents of the data bus are then latched into the 8282 8-bit latch to complete the full 16 bits of the address bus.

Channel	Register	Operation	Signals							Internal Flip-Flop	Data Bus DB0-DB7
			$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A3	A2	A1	A0		
0	Base and Current Address	Write	0	1	0	0	0	0	0	0	A0-A7
			0	1	0	0	0	0	0	1	A8-A15
	Current Address	Read	0	0	1	0	0	0	0	0	A0-A7
			0	0	1	0	0	0	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	0	0	1	0	W0-W7
			0	1	0	0	0	0	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	0	0	1	0	W0-W7
			0	0	1	0	0	0	1	1	W8-W15
1	Base and Current Address	Write	0	1	0	0	0	1	0	0	A0-A7
			0	1	0	0	0	1	0	1	A8-A15
	Current Address	Read	0	0	1	0	0	1	0	0	A0-A7
			0	0	1	0	0	1	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	0	1	1	0	W0-W7
			0	1	0	0	0	1	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	0	1	1	0	W0-W7
			0	0	1	0	0	1	1	1	W8-W15
2	Base and Current Address	Write	0	1	0	0	1	0	0	0	A0-A7
			0	1	0	0	1	0	0	1	A8-A15
	Current Address	Read	0	0	1	0	1	0	0	0	A0-A7
			0	0	1	0	1	0	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	1	0	1	0	W0-W7
			0	1	0	0	1	0	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	1	0	1	0	W0-W7
			0	0	1	0	1	0	1	1	W8-W15
3	Base and Current Address	Write	0	1	0	0	1	1	0	0	A0-A7
			0	1	0	0	1	1	0	1	A8-A15
	Current Address	Read	0	0	1	0	1	1	0	0	A0-A7
			0	0	1	0	1	1	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	1	1	1	0	W0-W7
			0	1	0	0	1	1	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	1	1	1	0	W0-W7
			0	0	1	0	1	1	1	1	W8-W15

Figure 5. Word Count and Address Register Command Codes

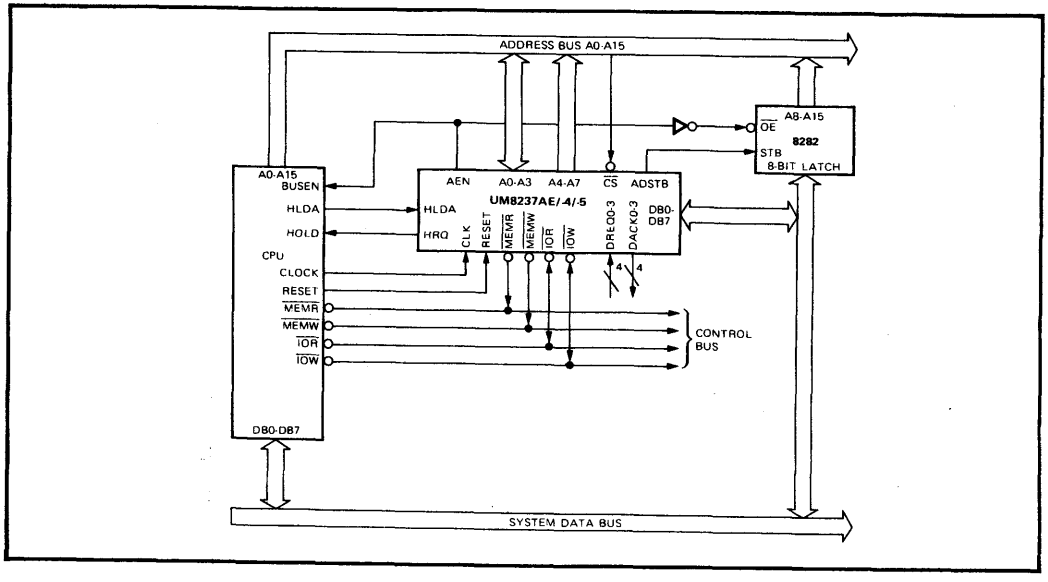


Figure 6. UM8237AE/-4/-5 System Interface

Timing Waveforms

Slave Mode Write Timing

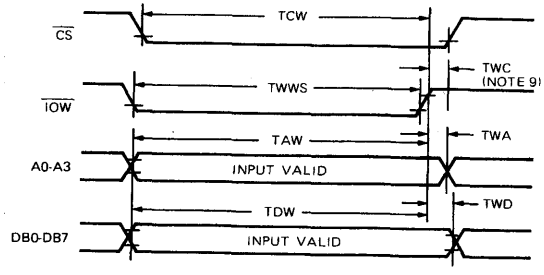


Figure 7. Slave Mode Write

Slave Mode Read Timing

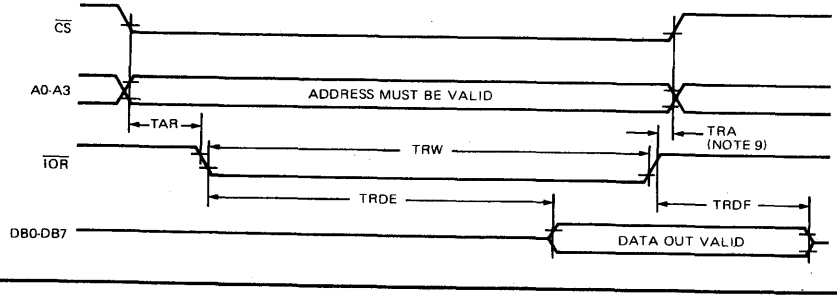


Figure 8. Slave Mode Read

Timing Waveforms (Continued)

DMA Transfer Timing

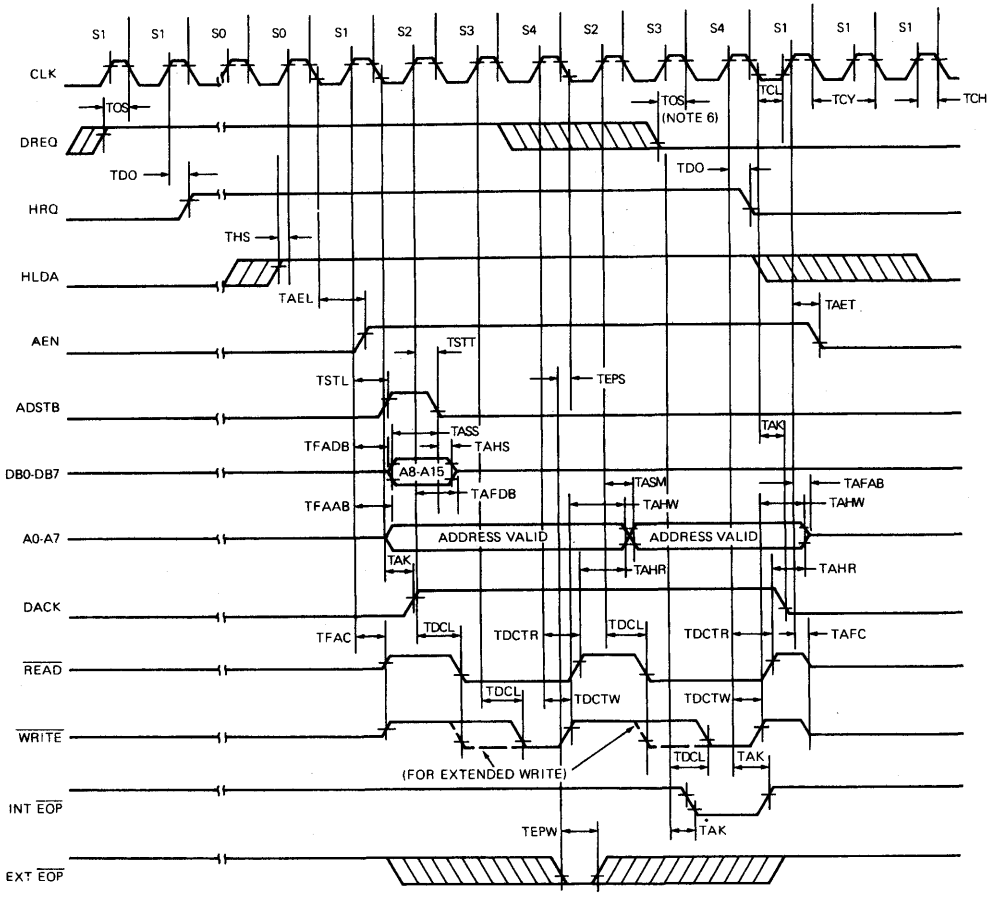


Figure 9. DMA Transfer

Timing Waveforms (Continued)

Memory-to-Memory Transfer Timing

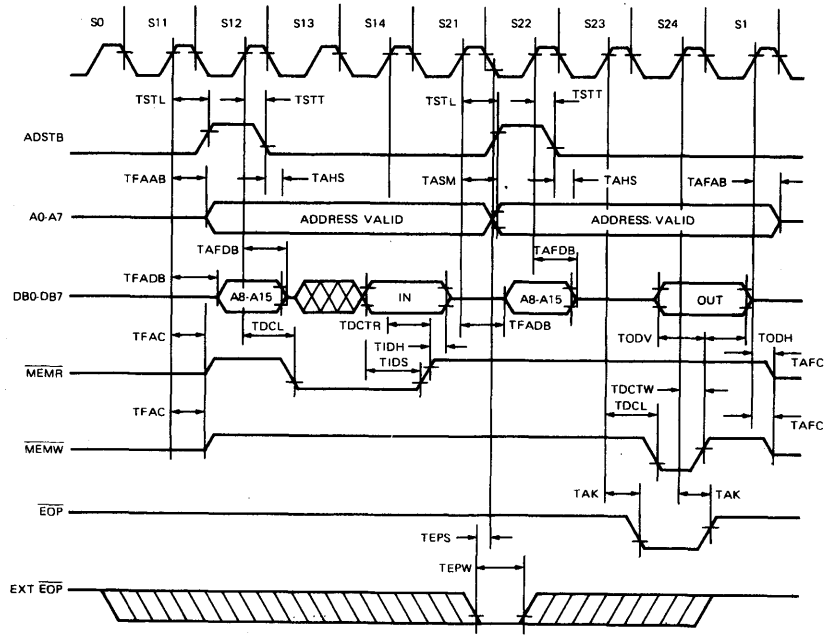


Figure 10. Memory-to-Memory Transfer

Ready Timing

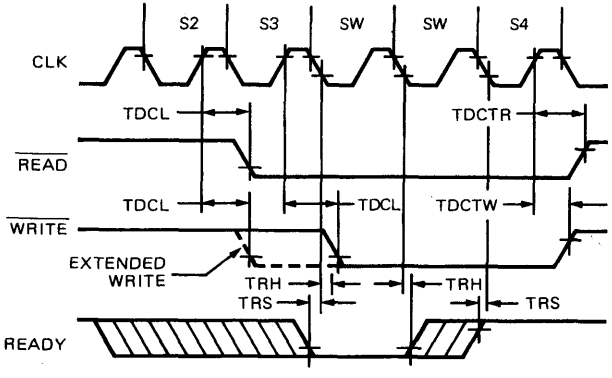


Figure 11. Ready

Timing Waveforms (Continued)

Compressed Transfer Timing

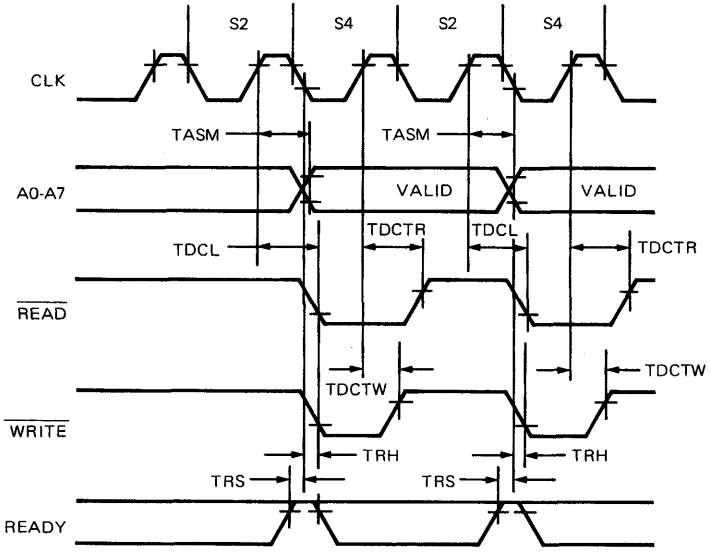


Figure 12. Compressed Transfer

Reset Timing

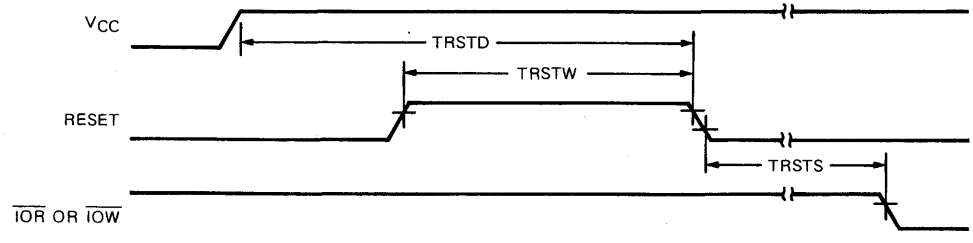


Figure 13. Reset

Ordering Information

Part No.	Frequency	Package
UM8237AE	3 MHz	40L DIP
UM8237AE-4	4 MHz	40L DIP
UM8237AE-5	5 MHz	40L DIP

UMC

UM8253/-5

Programmable Interval Timer

Features

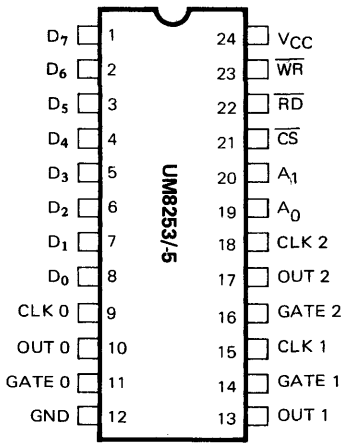
- 3 independent 16-bit counters
- DC to 2.6 MHz (UM8253)
- DC to 5.0 MHz (UM8253-5)
- Programmable counter modes
- Count binary or BCD
- Single +5V supply

General Description

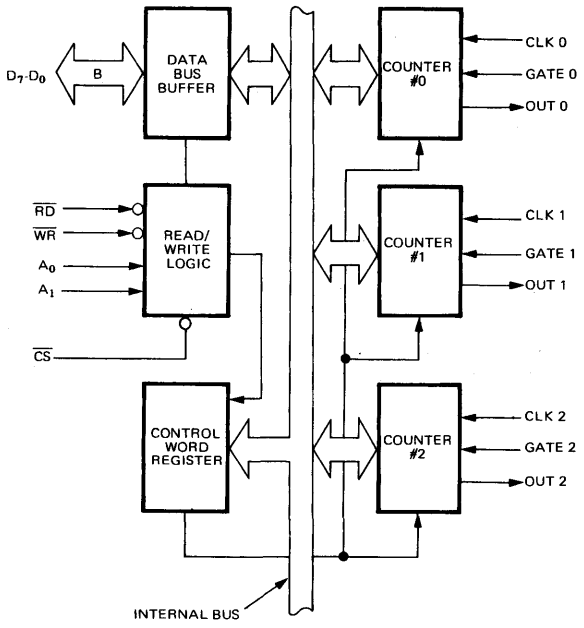
The UM8253/-5 is a programmable counter timer device designed for use as a microcomputer peripheral. It is processed using NMOS technology with a single +5V supply and is packaged in a 24-pin plastic DIP.

It is organized as 3 independent 16-bit counters, each with a count rate of up to 2.6 MHz. All modes of operation are software programmable.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Ambient Temperature Under Bias T_A . . . . . 0°C to 70°C

Storage Temperature T_{STG} . . . . . –65°C to +150°C

Voltage on Any Pin with Respect to Ground . . . . . –0.5V to +7V

Power Dissipation . . . . . 1 Watt

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Min	Max.	Unit	Conditions
V_{IL}	Input Low Voltage	–0.5	0.8	V	
V_{IH}	Input High Voltage	2.2	$V_{CC+0.5V}$	V	
V_{OL}	Output Low Voltage		0.45	V	Note 1
V_{OH}	Output High Voltage	2.4		V	Note 2
I_{IL}	Input Load Current		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = V_{CC} to 0.45V
I_{CC}	V_{CC} Supply Current		140	mA	

Capacitance

(T_A = 25°C, V_{CC} = GND = 0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance			10	pF	fc = 1 MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to V_{SS}

AC Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5.0V ± 10%, GND = 0V)

Bus Parameters (Note 3)

READ CYCLE

Symbol	Parameter	UM8253		UM8253-5		Unit
		Min.	Max.	Min.	Max.	
t_{AR}	Address Stable Before $\overline{READ}$	50		30		ns
t_{RA}	Address Hold Time for $\overline{READ}$	5		5		ns
t_{RR}	$\overline{READ}$ Pulse Width	400		300		ns
t_{RD}	Data Delay From $\overline{READ}$ (4)		300		200	ns
t_{DF}	$\overline{READ}$ to Data Floating	25	125	25	100	ns
t_{RV}	Recovery Time Between READ and Any Other Control Signal	1		1		μs

AC Characteristics (Continued)

WRITE CYCLE

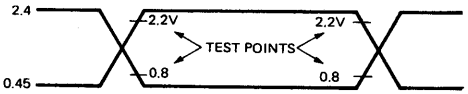
Symbol	Parameter	UM8253		UM8253-5		Unit
		Min.	Max.	Min.	Max.	
t_{AW}	Address Stable Before $\overline{WRITE}$	50		30		ns
t_{WA}	Address Hold Time for $\overline{WRITE}$	30		30		ns
t_{WW}	$\overline{WRITE}$ Pulse Width	400		300		ns
t_{DW}	Data Set Up Time for $\overline{WRITE}$	300		250		ns
t_{WD}	Data Hold Time for $\overline{WRITE}$	40		30		ns
t_{RV}	Recovery time Between $\overline{WRITE}$ and Any Other Control Signal	1		1		μs

Clock and Gate Timing

Symbol	Parameter	UM8253		UM8253-5		Unit
		Min.	Max.	Min.	Max.	
t_{CLK}	Clock Period	380	DC	380	DC	ns
t_{PWH}	High Pulse Width	230		230		ns
t_{PWL}	Low Pulse Width	150		150		ns
t_{GW}	Gate Width High	150		150		ns
t_{GL}	Gate Width Low	100		100		ns
t_{GS}	Gate Set Up Time to CLK↑	100		100		ns
t_{GH}	Gate Hold Time After CLK↑	50		50		ns
t_{OD}	Output Delay From CLK↓[4]		400		400	ns
t_{ODG}	Output Delay From Gate↓[4]		300		300	ns

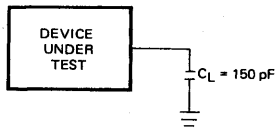
Notes:
1. I_{OL} = 2.2 mA.
2. I_{OH} = –400 μA.
3. AC timings measured at V_{OH} 2.2, V_{OL} = 0.8.
4. C_L = 150pF.

AC Testing Input, Output Waveform



A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0" TIMING MEASUREMENTS ARE MADE AT 2.2V FOR A LOGIC "1" AND 0.8V FOR A LOGIC 0

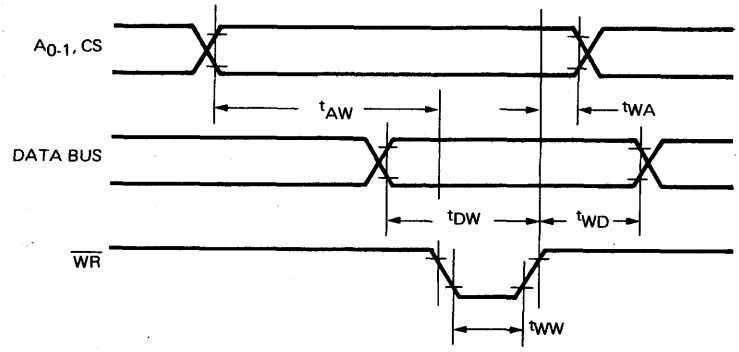
AC Testing Load Circuit



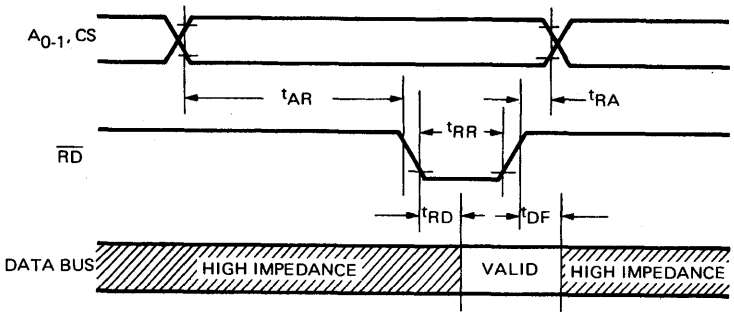
C_L INCLUDES JIG CAPACITANCE

Timing Waveforms

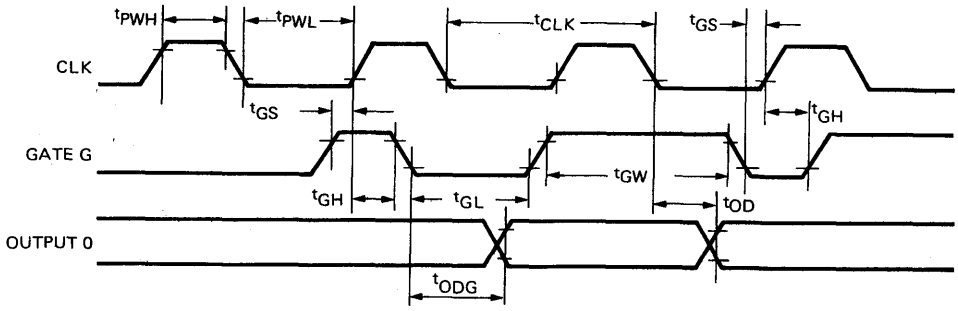
WRITE TIMING



READ TIMING



CLOCK AND GATE TIMING



Functional Description

General

The UM8253/-5 is a programmable interval timer/counter specifically designed for use with microcomputer systems. Its function is that of a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.

The UM8253/-5 solves one of the most common problems in any microcomputer system; the generation of accurate time delays under software control. Instead of setting up timing loops in systems software, the programmer configures the UM8253/-5 to match his requirements, initializes one of the counters of the UM8253/-5 with the desired quantity, then upon command the UM8253/-5 will count out the delay and interrupt the CPU when it has completed its tasks. It is easy to see that the software overhead is minimal and that multiple delays can easily be maintained by assignment of priority levels.

Other counter/timer functions that are non-delay in nature but also common to most microcomputers can be implemented with the UM8253/-5.

- Programmable Rate Generator
- Event Counter
- Binary Rate Multiplier
- Real Time Clock
- Digital One-Shot
- Complex Motor Controller

Data Bus Buffer

This 3-state, bi-directional, 8-bit buffer is used to interface the UM8253/-5 to the system data bus. Data is transmitted or received by the buffer upon execution of input or output CPU instructions. The Data Bus Buffer has three basic functions.

1. Programming the MODES of the UM8253/-5.
2. Loading the count registers.
3. Reading the count values.

Read/Write Logic

The Read/Write Logic accepts inputs from the system bus and in turn generates control signals for overall device operation. It is enabled or disabled by CS so that no operation can occur to change the function unless the device has been selected by the system logic.

$\overline{RD}$ (Read)

A "low" on this input informs the UM8253/-5 that the CPU is inputting data in the form of a counter value.

$\overline{WR}$ (Write)

A "low" on this input informs the UM8253/-5 that the CPU is outputting data in the form of mode information or loading counters.

A_0 , A_1

These inputs are normally connected to the address bus. Their function is to select one of the three counters to be operated on and to address the control word register for mode selection.

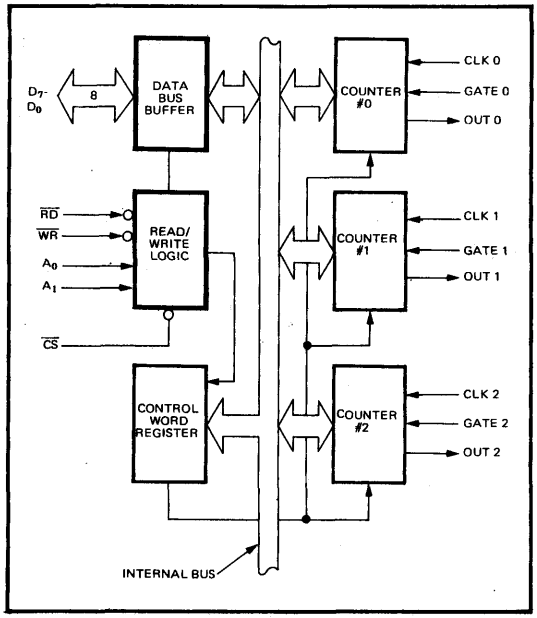


Figure 1. Block Diagram Showing Data Bus Buffer and Read/Write Logic Functions

CS	RD	WR	A_1	A_0	Operation
0	1	0	0	0	Load Counter No. 0
0	1	0	0	1	Load Counter No. 1
0	1	0	1	0	Load Counter No. 2
0	1	0	1	1	Write Mode Word
0	0	1	0	0	Read Counter No. 0
0	0	1	0	1	Read Counter No. 1
0	0	1	1	0	Read Counter No. 2
0	0	1	1	1	No-Operation 3-State
1	X	X	X	X	Disable 3-State
0	1	1	X	X	No-Operation 3-State

$\overline{CS}$ (Chip Select)

A "low" on this input enables the UM8253/-5. No reading or writing will occur unless the device is selected. The $\overline{CS}$ input has no effect upon the actual operation of the counters.

Control Word Register

The Control Word Register is selected when A_0, A_1 are 1,1. It then accepts information from the data bus buffer and stores it in a register. The information stored in this register controls the operational MODE of each counter, selection of binary or BCD counting and the loading of each count register.

The Control Word Register can only be written into; no read operation of its contents is available.

Counter #0, Counter #1, Counter #2

These three functional blocks are identical in operation so only a single Counter will be described. Each Counter consists of a single, 16-bit, pre-settable, DOWN counter. The counter can operate in either binary or BCD and its input, gate and output are configured by the selection of MODES stored in the Control Word Register.

The counters are fully independent and each can have separate mode configuration and counting operation, binary or BCD. Also, there are special features in the control words that handle the loading of the count value so that software overhead can be minimized for these functions.

The reading of the contents of each counter is available to the programmer with simple READ operations for event counting applications and special commands and logic are included in the UM8253/-5 so that the contents of each counter can be read "on the fly" without having to inhibit the clock input.

UM8253/-5 System Interface

The UM8253/-5 is a component of the UMC Microcomputer Systems and interfaces in the same manner as all other peripherals of the family. It is treated by the systems software as an array of peripheral I/O ports; three are counters and the fourth is a control register for MODE programming.

Basically, the select inputs A_0, A_1 connect to the A_0, A_1 address bus signals of the CPU. The CS can be derived directly from the address bus using a linear select method. Or it can be connected to the output of a decoder, such as an 8205 for larger systems.

Operational Description

General

The complete functional definition of the UM8253/-5 is programmed by the systems software. A set of control words must be sent out by the CPU to initialize each counter of the UM8253/-5 with the desired MODE and

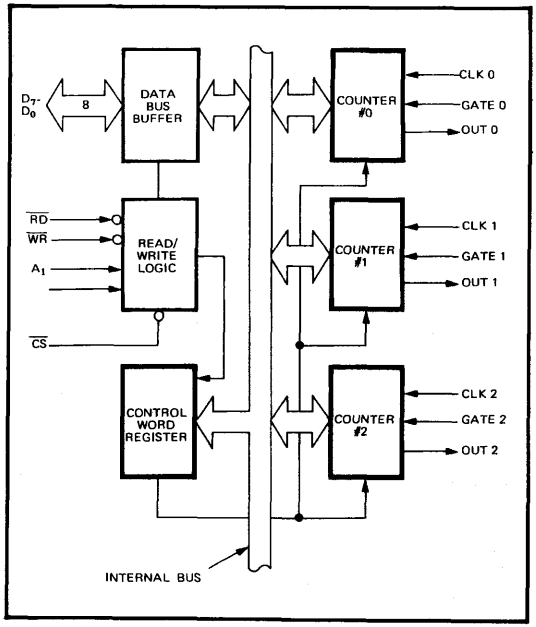


Figure 2. Block Diagram Showing Control Word Register and Counter Functions

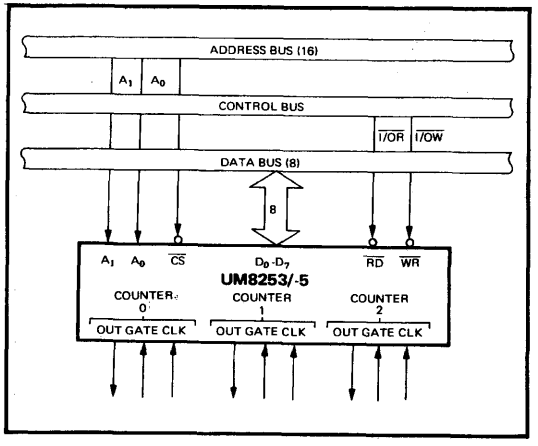


Figure 3. UM8253/-5 System Interface

quantity information, prior to initialization, the MODE, count, and output of all counters is undefined. These control words program the MODE, loading sequence and selection of binary or BCD counting.

Once programmed, the UM8253/-5 is ready to perform whatever timing tasks it is assigned to accomplish.

The actual counting operation of each counter is completely independent and additional logic is provided on-chip so that the usual problems associated with efficient monitoring and management of external, asynchronous events or rates to the microcomputer system have been eliminated.

Programming the UM8253/-5

All of the MODES for each counter are programmed by the systems software by simple I/O operations.

Each counter of the UM8253/-5 is individually programmed by writing a control word into the Control Word Register. (A_0, A_1 = 11)

Control Word Format

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

Definition of Control

SC – Select Counter:

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Illegal

RL – Read/Load:

RL1	RL0	
0	0	Counter Latching operation (see READ/WRITE procedure Section)
1	0	Read/Load most significant byte only.
0	1	Read/Load least significant byte only.
1	1	Read/Load least significant byte first, then most significant byte.

M – MODE:

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD:

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

Counter Loading

The count register is not loaded until the count value is written (one or two bytes, depending on the mode selected by the RL bits), followed by a rising edge and a falling edge of the clock. Any read of the counter prior to that falling clock edge may yield invalid data.

MODE Definition

MODE 0: Interrupt on Terminal Count. The output will be initially low after the mode set operation. After the count is loaded into the selected count register, the output will remain low and the counter will count. When terminal count is reached the output will go high and remain high until the selected count register is reloaded with the mode or a new count is loaded. The counter continues to decrement after terminal count has been reached.

Rewriting a counter register during counting results in the following:

(1) Write 1st byte stops the current counting.
(2) Write 2nd byte starts the new count.

MODE 1: Programmable One-Shot. The output will go low on the count following the rising edge of the gate input.

The output will go high on the terminal count. If a new count value is loaded while the output is low it will not affect the duration of the one-shot pulse until the succeeding trigger. The current count can be read at any time without affecting the one-shot pulse.

The one-shot is retriggerable, hence the output will remain low for the full count after any rising edge of the gate input.

MODE 2: Rate Generator. Divide by N counter. The output will be low for one period of the input clock. The period from one output pulse to the next equals the number of input counts in the count register. If the count register is reloaded between output pulses the present period will not be affected, but the subsequent period will reflect the new value.

The gate input, when low, will force the output high. When the gate input goes high, the counter will start from the initial count. Thus, the gate input can be used to synchronize the counter.

When this mode is set, the output will remain high until after the count register is loaded. The output then can also be synchronized by software.

MODE 3: Square Wave Rate Generator. Similar to MODE 2 except that the output will remain high until one half the count has been completed (for even numbers) and go low for the other half of the count. This is accomplished by decrementing the counter by two on the falling edge of each clock pulse. When the counter reaches terminal count, the state of the output is changed and the counter is reloaded with the full count and the whole process is repeated.

If the count is odd and the output is high, the first clock pulse (after the count is loaded) decrements the count by 1. Subsequent clock pulses decrement the clock by 2. After timeout, the output goes low and the full count is reloaded. The first clock pulse (following the reload) decrements the counter by 3. Subsequent clock pulses decrement the count by 2 until timeout. Then the whole process is repeated. In this way, if the count is odd, the output will be high for (N+1)/2 counts and low for (N–1)/2 counts.

In Modes 2 and 3, if a CLK source other than the system clock is used, GATE should be pulsed immediately following WR of a new count value.

MODE 4: Software Triggered Strobe. After the mode is set, the output will be high. When the count is loaded, the counter will begin counting. On terminal count, the output will go low for one input clock period, then will go high again.

If the count register is reloaded during counting, the new count will be loaded on the next CLK pulse. The count will be inhibited while the GATE input is low.

MODE 5: Hardware Triggered Strobe. The counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable. The output will not go low until the full count after the rising edge of any trigger.

Signal Status / Modes	Low or Going Low	Rising	High
0	Disables counting	—	Enables counting
1	—	1) Initiates counting 2) Resets output after next clock	—
2	1) Disables counting 2) Sets output immediately high	1) Reloads counter 2) Initiates counting	Enables counting
3	1) Disables counting 2) Sets output immediately high	1) Reloads counter 2) Initiates counting	Enables counting
4	Disables counting	—	Enables counting
5	—	Initiates counting	—

Figure 4. Gate Pin Operations Summary

UM8253/-5 Read/Write Procedure

Write Operations

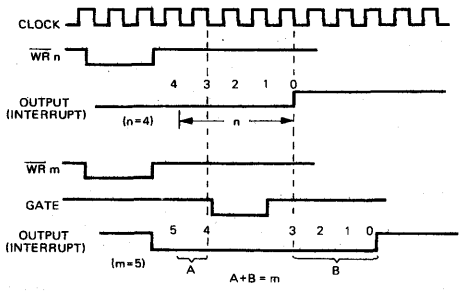
The systems software must program each counter of the UM8253/-5 with the mode and quantity desired. The programmer must write out to the UM8253/-5 a MODE control word and the programmed number of count register bytes (1 or 2) prior to actually using the selected counter.

The actual order of the programming is quite flexible. Writing out of the MODE control word can be in any sequence of counter selection, e.g., counter #0 does not have to be first or counter #2 last. Each counter's MODE control word register has a separate address so that its loading is completely sequence independent. (SC0, SC1)

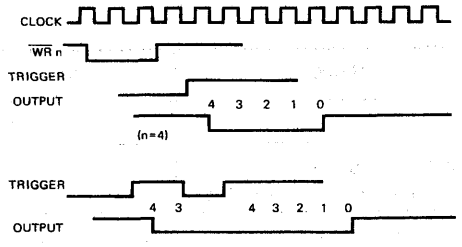
The loading of the Count Register with the actual count value, however, must be done in exactly the sequence programmed in the MODE control word (RL0, RL1). This loading of the counter's count register is still sequence independent like the MODE control word loading, but when a selected count register is to be loaded it ***must*** be loaded with the number of bytes programmed in the MODE control word (RL0, RL1). The one or two bytes to be loaded in the count register do not have to follow the associated MODE control word. They can be programmed at any time following the MODE control word loading as long as the correct number of bytes is loaded in order.

All counters are down counters. Thus, the value loaded into the count register will actually be decremented. Loading all zeroes into a count register will result in the maximum count (2^{16} for Binary or 10^4 for BCD).

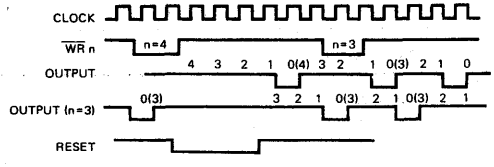
MODE 0: INTERRUPT ON TERMINAL COUNT



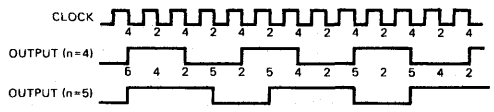
MODE 1: PROGRAMMABLE ONE-SHOT



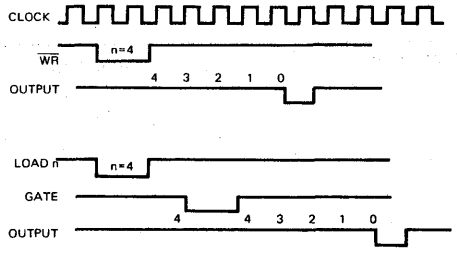
MODE 2: RATE GENERATOR



MODE 3: SQUARE WAVE GENERATOR



MODE 4: SOFTWARE TRIGGERED STROBE



MODE 5: HARDWARE TRIGGERED STROBE

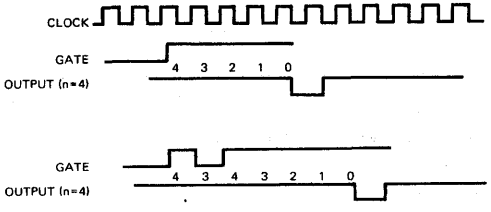


Figure 5. UM8253/-5 Timing Diagrams

In MODE 0 the new count will not restart until the load has been completed. It will accept one of two bytes depending on how the MODE control words (RL0, RL1) are programmed. Then proceed with the restart operation.

Read Operations

In most counter applications it becomes necessary to read the value of the count in progress and make a computational decision based on this quantity. Event counters are probably the most common application that uses this function. The UM8253/-5 contains logic that will allow the programmer to easily read the contents of any of the three counters without disturbing the actual count in progress.

There are two methods that the programmer can use to read the value of the counters. The first method involves the use of simple I/O read operations of the selected counter. By controlling the A_0, A_1 inputs to the UM8253/-5 the programmer can select the counter to be read

(remember that no read operation of the mode register is allowed A_0, $A_1 = 11$. The only requirement with this method is that in order to assure a stable count reading the actual operation of the selected counter ***must be inhibited*** either by controlling the Gate input or by external logic that inhibits the clock input. The contents of the counter selected will be available as follows:

First I/O Read contains the least significant byte (LSB).

second I/O Read contains the most significant byte (MSB).

Due to the internal logic of the UM8253/-5 it is absolutely necessary to complete the entire reading procedure. If two bytes are programmed to be read then two bytes must be read before any loading WR command can be sent to the same counter.

Read Operation Chart

A_1	A_0	RD	
0	0	0	Read Counter No. 0
0	1	0	Read Counter No. 1
1	0	0	Read Counter No. 2
1	1	0	Illegal

Reading While Counting

In order for the programmer to read the contents of any counter without affecting or disturbing the counting operation the UM8253/-5 has special internal logic that can be accessed using simple WR commands to the MODE register. Basically, when the programmer wishes to read the contents of a selected counter "on the fly" he loads the MODE register with a special code which latches the present count value into a storage register so that its contents contain an accurate, stable quantity. The programmer then issues a normal read command to the selected counter and the contents of the latched register are available.

	MODE Control Word Counter n
LSB	Count Register byte Counter n
MSB	Count Register byte Counter n

Note: Format shown is a simple example of loading the UM8253/-5 and does not imply that it is the only format.

Figure 6. Programming Format

MODE Register for Latching Count

A_0, A_1 = 11

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	0	0	X	X	X	X

SC1, SC0 – specify counter to be latched.

D5, D4 – 00 designates counter latching operation.

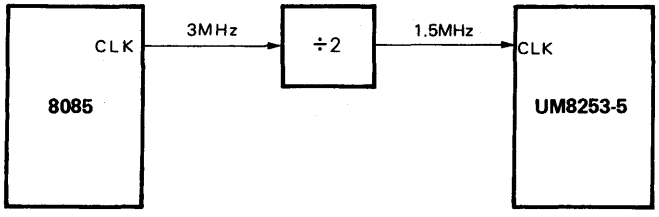
X – don't care.

The same limitation applies to this mode of reading the counter as the previous method. That is, it is mandatory to complete the entire read operation as programmed. This command has no effect on the counter's mode.

			A_1	A_0
No. 1		MODE Control Word Counter 0	1	1
No. 2		MODE Control Word Counter 1	1	1
No. 3		MODE Control Word Counter 2	1	1
No. 4	LSB	Count Register Byte Counter 1	0	1
No. 5	MSB	Count Register Byte Counter 1	0	1
No. 6	LSB	Count Register Byte Counter 2	1	0
No. 7	MSB	Count Register Byte Counter 2	1	0
No. 8	LSB	Count Register Byte Counter 0	0	0
No. 9	MSB	Count Register Byte Counter 0	0	0

Note: The exclusive addresses of each counter's count register make the task of programming the UM8253/-5 a very simple matter, and maximum effective use of the device will result if this feature is fully utilized.

Figure 7. Alternate Programming Formats



If an 8085 clock output is to drive a UM8253-5 clock input, it must be reduced to 2MHz or less.

Figure 8. MCS-85™ Clock Interface

Ordering Information

Part Number	Clock
UM8253	2.6MHz
UM8253–5	5MHz

UMC

UM8259A-2

Programmable Interrupt Controller

Features

- Eight-level priority controller
- Expandable to 64 levels
- Programmable interrupt modes
- Individual request mask capability
- Single +5V supply (no clocks)
- 28-pin dual-in-line package

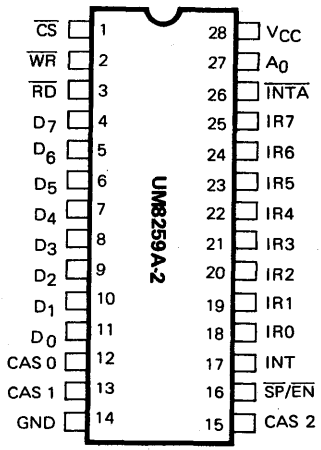
General Description

The UM8259A-2 Programmable Interrupt Controller handles up to eight vectored priority interrupts for the CPU. It is cascadable for up to 64 vectored priority interrupts without additional circuitry. Packaged in a 28-pin DIP, it uses NMOS technology and requires a single +5V supply. Circuitry is static, requiring no clock input.

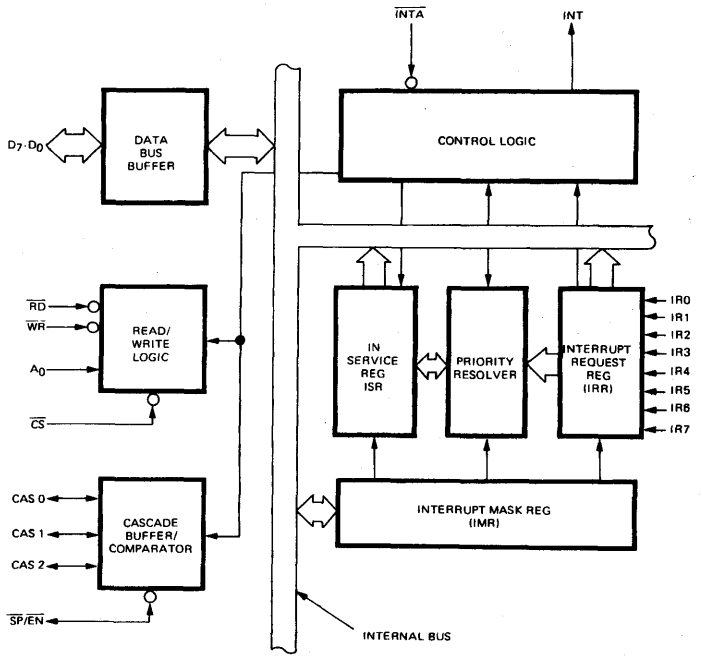
The UM8259A-2 is designed to minimize the software and real time overhead in handling multi-level priority interrupts. It has several modes, permitting optimization for a variety of system requirements.

The UM8259A-2 is fully compatible with the Intel 8259A-2. Software originally written for the 8259A-2 will operate the UM8259A-2 in all 8259A-2 equivalent modes.

Pin Configuration



Block Diagram



*iAPX86, iAPX88, MCS-80 and MCS-85 are all trademarks of Intel Microsystems

Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . 0°C to 70°C

Storage Temperature . . . . . –65°C to +150°C

Voltage on Any Pin with

Respect to Ground . . . . . –0.5V to +7V

Power Dissipation . . . . . 1 Watt

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Min.	Max.	Unit	Conditions
V_{IL}	Input Low Voltage	–0.5	0.8	V	
V_{IH}	Input High Voltage	2.0*	V_{CC}+ 0.5V	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = –400μA
$V_{OH(INT)}$	Interrupt Output High Voltage	3.5		V	I_{OH} = –100μA
		2.4		V	I_{OH} = –400μA
I_{LI}	Input Load Current	–10	+10	μA	0V V_{IN} V_{CC}
I_{LOL}	Output Leakage Current	–10	+10	μA	0.45V V_{OUT} V_{CC}
I_{CC}	V_{CC} Supply Current		85	mA	
I_{LIR}	IR Input Load Current		–300	μA	V_{IN} = 0
			10	μA	V_{IN} = V_{CC}

Capacitance

(T_A = 25°C; V_{CC} = GND = 0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance			10	pF	fc = 1 MHZ
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to V_{SS}

AC Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 10%)

TIMING REQUIREMENTS

Symbol	Parameter	Min.	Max.	Unit	Conditions
TAHRL	A0/$\overline{CS}$ Setup to $\overline{RD}$/$\overline{INTA}$↓	0		ns	
THRAX	A0/$\overline{CS}$ Hold after $\overline{RD}$/$\overline{INTA}$↑	0		ns	
TRLRH	$\overline{RD}$ Pulse Width	160		ns	
TAHWL	A0/$\overline{CS}$ Setup to $\overline{WR}$↓	0		ns	
TWHAX	A0/$\overline{CS}$ Hold after $\overline{WR}$↑	0		ns	
TWLWH	$\overline{WR}$ Pulse Width	190		ns	
TDVWH	Data Setup to $\overline{WR}$↑	160		ns	
TWHDX	Data Hold after $\overline{WR}$↑	0		ns	
TJLJH	Interrupt Request Width (Low)	100		ns	See Note
TCVIAL	Cascade Setup to Second or Third $\overline{INTA}$↓ (Slave only)	40		ns	
TRHRL	End of $\overline{RD}$ to next $\overline{RD}$ End of $\overline{INTA}$ to next $\overline{INTA}$ within an $\overline{INTA}$ sequence only	160		ns	
TWHWL	End of $\overline{WR}$ to next $\overline{WR}$	190		ns	

AC Characteristics (Continued)

Symbol	Parameter	Min.	Max.	Unit	Conditions
*TCHCL	End of Command to next Command (Not same command type)	400		ns	
	End of $\overline{INTA}$ sequence to next $\overline{INTA}$ sequence.				

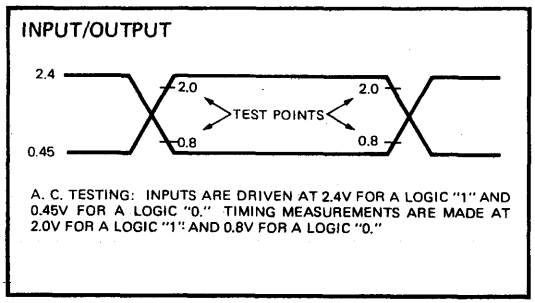
*Worst case timing for TCHCL in an actual microprocessor system is typically much greater than 500 ns (i.e. 8085A = 1.6μs, 8085A-2 = 1 μs, 8086 = 1 μs, 8086-2 = 625 ns)

Note: This is the low time required to clear the input latch in the edge triggered mode.

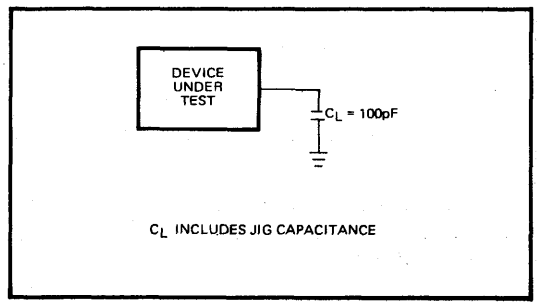
Timing Responses

Symbol	Parameter	Min.	Max.	Unit	Conditions
TRLDV	Data Valid from $\overline{RD}/\overline{INTA}\downarrow$		120	ns	C of Data Bus = 100 pF
TRHDZ	Data Float after $\overline{RD}/\overline{INTA}\uparrow$	10	85	ns	C of Data Bus Max. test C = 100 pF Min. test C = 15 pF
TJHIH	Interrupt Output Delay		300	ns	
TIALCV	Cascade Valid from First $\overline{INTA}$ (Master Only)		360	ns	C_{INT} = 100 pF
TRLEL	Enable Active from $\overline{RD}\downarrow$ or $\overline{INTA}\downarrow$		100	ns	$C_{CASCADE}$ = 100 pF
TRHEH	Enable Inactive from $\overline{RD}\uparrow$ or $\overline{INTA}\uparrow$		150	ns	
TAHDV	Data Valid from Stable Address		200	ns	
TCVDV	Cascade Valid to Valid Data		200	ns	

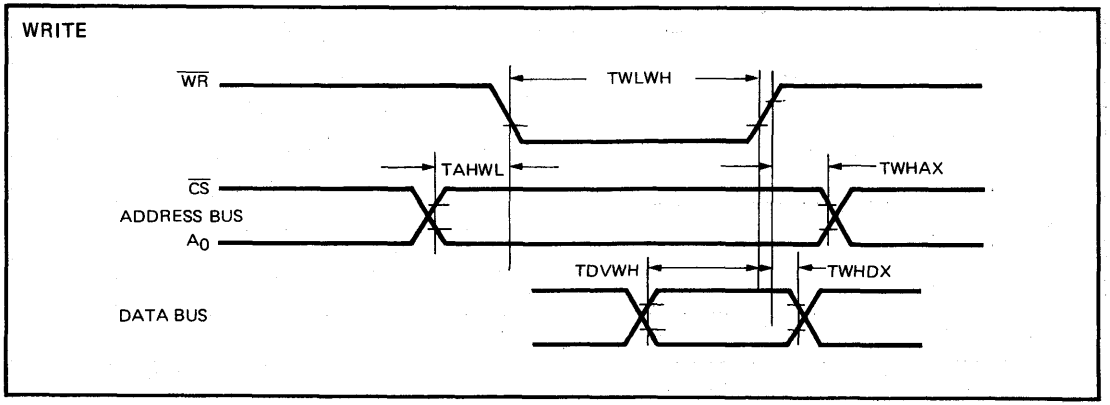
AC Testing Input, Output Waveform



AC Testing Load Circuit

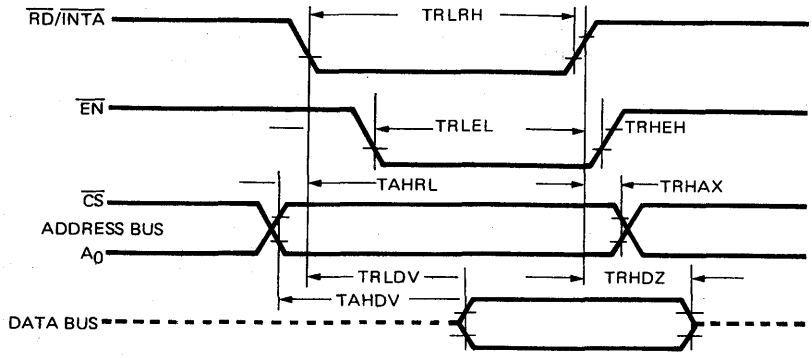


Timing Waveforms

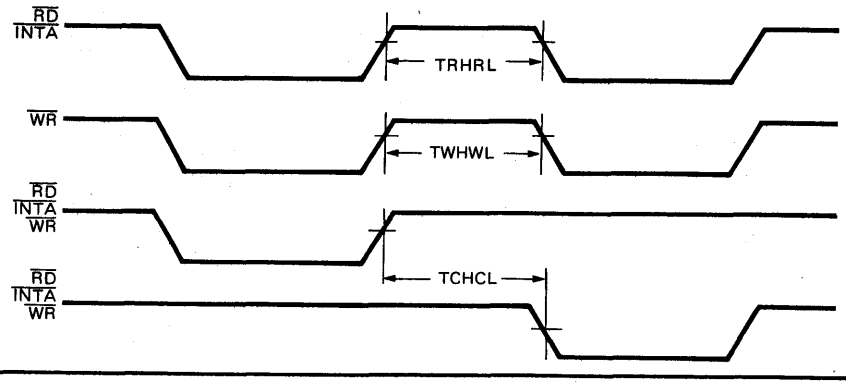


Waveforms (Continued)

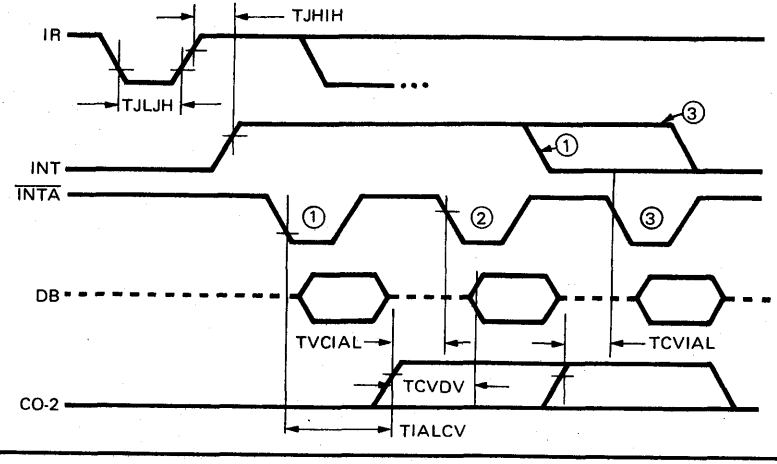
READ/INTA



OTHER TIMING



INTA SEQUENCE



Notes: Interrupt output must remain HIGH at least until leading edge of first INTA.

1. Cycle 1 in iAPX86, iAPX88 systems, the Data Bus is not active.

Pin Description

Pin No.	Symbol	I/O	Description
28	V_{CC}	I	Supply: +5V Supply.
14	GND	I	Ground.
1	$\overline{CS}$	I	Chip Select: A low on this pin enables RD and WR communication between the CPU and the UM8259A-2. INTA functions are independent of CS.
2	$\overline{WR}$	I	Write: A low on this pin when CS is low enables the UM8259A-2 to accept command words from the CPU.
3	$\overline{RD}$	I	Read: A low on this pin when CS is low enables the UM8259A-2 to release status onto the data bus for the CPU.
4–11	D_7–D_0	I/O	Bidirectional Data Bus: Control, status and interrupt-vector information is transferred via this bus.
12, 13, 15	CAS0–CAS2	I/O	Cascade Lines: The CAS lines form a private UM8259A-2 bus to control a multiple UM8259A-2 structure. These pins are outputs for a master UM8259A-2 and inputs for a slave UM8259A-2.
16	$\overline{SP}/\overline{EN}$	I/O	Slave Program/Enable Buffer: This is a dual function pin. When in the Buffered Mode it can be used as an output to control buffer transceivers (EN). When not in the buffered mode it is used as an input to designate a master (SP = 1) of slave (SP = 0).
17	INT	O	Interrupt: This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, thus it is connected to the CPU's interrupt pin.
18–25	IR0–IR7	I	Interrupt Requests: Asynchronous inputs. An interrupt request is executed by raising an IR input (low to high), and holding it high until it is acknowledged (Edge Triggered Mode), or just by a high level on an IR input (Level Triggered Mode).
26	$\overline{INTA}$	I	Interrupt Acknowledge: This pin is used to enable UM8259A-2 interrupt-vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
27	A_0	I	AO Address Line: This pin acts in conjunction with the $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ pins. It is used by the UM8259A-2 to decipher various Command Words the CPU writes and status the CPU wishes to read. It is typically connected to the CPU A0 address line (A1 for iAPX 86, 88).

Functional Description

Interrupts in Microcomputer Systems

Microcomputer system design requires that I/O devices such as keyboards, displays, sensors and other components receive servicing in an efficient manner so that large amounts of the total system tasks can be assumed by the microcomputer with little or no effect on throughput.

The most common method of servicing such devices is the Polled approach. This is where the processor must test each device in sequence and in effect "ask" each one if it needs servicing. It is easy to see that a large portion of the main program is looping through this continuous polling cycle and that such a method would have a serious, detrimental effect on system throughput, thus limiting the tasks that could be assumed by the microcomputer and reducing the cost effectiveness of using such devices.

A more desirable method would be one that would allow the microprocessor to be executing its main program and only stop to service peripheral devices when it is told to do so by the device itself. In effect, the method would provide an external asynchronous input that would inform the processor that it should complete whatever instruction that is currently being executed and fetch a new routine that will service the requesting device. Once this servicing is complete, however, the processor would resume exactly where it left off.

This method is called Interrupt. It is easy to see that system throughput would drastically increase, and thus more tasks could be assumed by the microcomputer to further enhance its cost effectiveness.

The Programmable Interrupt Controller (PIC) functions as an overall manager in an Interrupt-Driven system environment. It accepts requests from the peripheral equipment, determines which of the incoming requests is of the highest importance (priority), ascertains whether the incoming request has a higher priority value than the level currently being serviced, and issues an interrupt to the CPU based on this determination.

Each peripheral device or structure usually has a special program or "routine" that is associated with its specific functional or operational requirements; this is referred to as a "service routine". The PIC, after issuing an interrupt to the CPU, must somehow input information into the CPU that can "point" the Program Counter to the Service routine associated with the requesting device. This "pointer" is an address in a vectoring table and will often be referred to, in this document, as vectoring data.

The UM8259A-2

The UM8259A-2 is a device specifically designed for use in real time, interrupt driven microcomputer systems. It manages eight levels or requests and has built-in features for expandability to other UM8259A-2's (up to 64 levels). It is programmed by the system's software as an I/O peripheral. A selection of priority modes is available to the programmer so that the manner in which the requests are processed by the UM8259A-2 can be configured to match his system requirements. The priority modes can be changed or reconfigured dynamically at any time during the main program. This means that the complete interrupt structure can be defined as required, based on the total system environment.

Interrupt Request Register (IRR) and In-Service Register (ISR)

The Interrupts at the IR input lines are handled by two registers in cascade, the Interrupt Request Register (IRR) and the In-Service Register (ISR). The IRR is used to store all the interrupt levels which are requesting service; and the ISR is used to store all the interrupt levels which are being serviced.

Priority Resolver

This logic block determines the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during $\overline{INTA}$ pulse.

Interrupt Mask Register (IMR)

The IMR stores the bits which mask the interrupt lines to be masked. The IMR operates on the IRR. Masking of a higher priority input will not affect the interrupt request lines of lower priority.

INT (Interrupt)

This output goes directly to the CPU interrupt input. The V_{OH} level on this line is designed to be fully compatible with the 8080A, 8085A and 8086 input levels.

$\overline{INTA}$ (Interrupt Acknowledge)

$\overline{INTA}$ pulses will cause the UM8259A-2 to release vectoring information onto the data bus. The format of this data depends on the system mode (μPM) of the UM8259A-2.

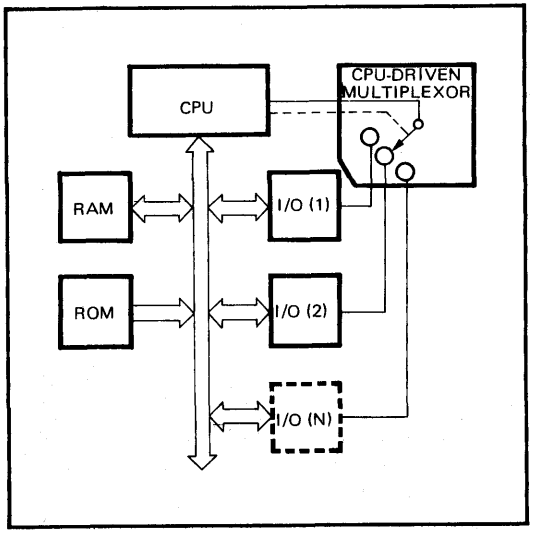


Figure 1a. Polled Method

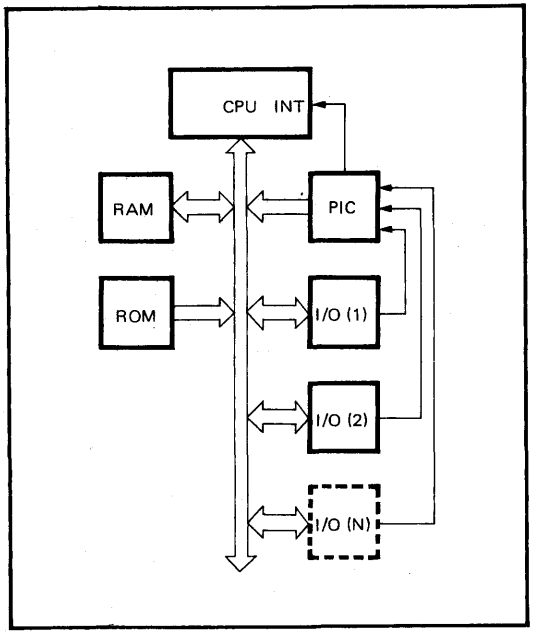


Figure 1b. Interrupt Method

Data Bus Buffer

This 3-state, bidirectional 8-bit buffer is used to interface the UM8259A-2 to the system Data Bus. Control words and status information are transferred through the Data Bus Buffer.

Read/Write Control Logic

The function of this block is to accept OUT put commands from the CPU. It contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers which store the various control formats for device operation. This function block also allows the status of the UM8259A-2 to be transferred onto the Data Bus.

$\overline{CS}$ (Chip Select)

A LOW on this input enables the UM8259A-2. No reading or writing of the chip will occur unless the device is selected.

$\overline{WR}$ (Write)

A LOW on this input enables the CPU to write control words (ICWs and OCWs) to the UM8259A-2.

$\overline{RD}$ (Read)

A LOW on this input enables the UM8259A-2 to send the status of the interrupt Request Register (IRR). In Service Register (ISR), the Interrupt Mask Register (IMR), or the Interrupt level onto the Data Bus.

A_0

This input signal is used in conjunction with $\overline{WR}$ and $\overline{RD}$ signals to write commands into the various command registers, as well as reading the various status registers of the chip. This line can be tied directly to one of the address lines.

The Cascade Buffer/Comparator

This function block stores and compares the IDs of all UM8259A-2's used in the system. The associated three I/O pins (CAS0–2) are outputs when the UM8259A-2 is used as a master and are inputs when the UM8259A-2 is used as a slave. As a master, the UM8259A-2 sends the ID of the interrupting slave device onto the CAS0–2 lines. The slave thus selected will send its preprogrammed subroutine address onto the Data Bus during the next one or two consecutive $\overline{INTA}$ pulses. (See section "Cascading the UM8259A-2".)

Interrupt Sequence

The powerful features of the UM8259A-2 in a microcomputer system are its programmability and the interrupt routine addressing capability. The latter allows direct or indirect jumping to the specific interrupt routine requested without any polling of the interrupting devices. The normal sequence of events during an interrupt depends on the type of CPU being used.

The events occur as follows in an MCS-80/85 system:

1. One or more of the INTERRUPT REQUEST lines (IR7–0) are raised high, setting the corresponding IRR bit(s).
2. The UM8259A-2 evaluates these requests, and sends an INT to the CPU, if appropriate.
3. The CPU acknowledges the INT and responds with an $\overline{INTA}$ pulse.
4. Upon receiving an $\overline{INTA}$ from the CPU group, the highest priority ISR bit is set, and the corresponding IRR bit is reset. The UM8259A-2 will also release a CALL instruction code (11001101) onto the 8-bit Data Bus through its D7–0 pins.
5. This CALL Instruction will initiate two more $\overline{INTA}$ pulses to be sent to the UM8259A-2 from the CPU group.
6. These two $\overline{INTA}$ pulses allow the UM8259A-2 to release its preprogrammed subroutine address onto the Data Bus. The lower 8-bit address is released at the first $\overline{INTA}$ pulse and the higher 8-bit address is released at the second $\overline{INTA}$ pulse.
7. This completes the 3-byte CALL instruction released by the UM8259A-2. In the AEOI mode the ISR bit is reset at the end of the third $\overline{INTA}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt sequence.

The events occurring in an iAPX 86 system are the same until step 4.

4. Upon receiving an $\overline{INTA}$ from the CPU group, the highest priority ISR bit is set and the corresponding IRR bit is reset. The UM8259A-2 does not drive the Data Bus during this cycle.
5. The iAPX 86/10 will initiate a second $\overline{INTA}$ pulse. During this pulse, the UM8259A-2 releases an 8-bit pointer onto the Data Bus where it is read by the CPU.
6. This completes the interrupt cycle. In the AEOI mode the ISR bit is reset at the end of the second $\overline{INTA}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

If no interrupt request is present at step 4 of either sequence (i.e., the request was too short in duration) the UM8259A-2 will issue an interrupt level 7. Both the vectoring bytes and the CAS lines will look like an interrupt level 7 was requested.

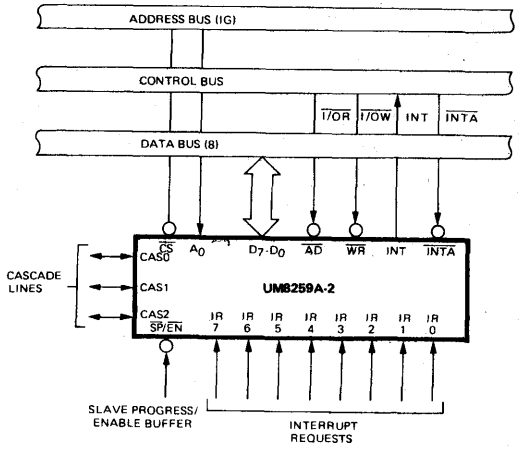


Figure 3. UM8259A-2 Interface to Standard System Bus

Interrupt Sequence Outputs

MCS-80®, MCS-85®

This sequence is timed by three $\overline{INTA}$ pulses. During the first $\overline{INTA}$ pulse the CALL opcode is enabled onto the data bus.

Content of First Interrupt Vector Byte

	D7	D6	D5	D4	D3	D2	D1	D0
CALL CODE	1	1	0	0	1	1	0	1

During the second $\overline{INTA}$ pulse the lower address of the appropriate service routine is enabled onto the data bus. When Interval=4 bits A_5-A_7 are programmed, while A_0-A_4 are automatically inserted by the UM8259A-2. When Interval=8 bits only A_6 and A_7 are programmed, while A_0-A_5 are automatically inserted.

Content of Second Interrupt Vector Byte

IR	Interval = 4							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	A5	1	1	1	0	0
6	A7	A6	A5	1	1	0	0	0
5	A7	A6	A5	1	0	1	0	0
4	A7	A6	A5	1	0	0	0	0
3	A7	A6	A5	0	1	1	0	0
2	A7	A6	A5	0	1	0	0	0
1	A7	A6	A5	0	0	1	0	0
0	A7	A6	A5	0	0	0	0	0

IR	Interval = 8							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	1	1	1	0	0	0
6	A7	A6	1	1	0	0	0	0
5	A7	A6	1	0	1	0	0	0
4	A7	A6	1	0	0	0	0	0
3	A7	A6	0	1	1	0	0	0
2	A7	A6	0	1	0	0	0	0
1	A7	A6	0	0	1	0	0	0
0	A7	A6	0	0	0	0	0	0

During the third INTA pulse the higher address of the appropriate service routine, which was programmed as byte 2 of the initialization sequence (A_8-A_{15}), is enabled onto the bus.

Content of Third Interrupt Vector Byte

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

iAPX 86, iAPX 88

iAPX 86 mode is similar to MCS-80 mode except that only two interrupt Acknowledge cycles are issued by the processor and no CALL opcode is sent to the processor. The first interrupt acknowledge cycle is similar to that of MCS-80, 85 systems in that the UM8259A-2 uses it to internally freeze the state of the interrupts for priority resolution and as a master it issues the interrupt code on the cascade lines at the end of the INTA pulse. On this first cycle it does not issue any data to the processor and leaves its data bus buffers disabled. On the second interrupt acknowledge cycle in iAPX 86 mode the master (or slave if so programmed) will send a byte of data to the processor with the acknowledged interrupt code composed as follows (note the state of the ADI mode control is ignored and A_5-A_{11} are unused in iAPX 86 mode):

Content of Interrupt Vector Byte for iAPX 86 System Mode

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	T7	T6	T5	T4	T3	1	1	1
IR6	T7	T6	T5	T4	T3	1	1	0
IR5	T7	T6	T5	T4	T3	1	0	1
IR4	T7	T6	T5	T4	T3	1	0	0
IR3	T7	T6	T5	T4	T3	0	1	1
IR2	T7	T6	T5	T4	T3	0	1	0
IR1	T7	T6	T5	T4	T3	0	0	1
IR0	T7	T6	T5	T4	T3	0	0	0

Programming the UM8259A-2

The UM8259A-2 accepts two types of command words generated by the CPU:

1. Initialization Command Words (ICWs): Before normal operation can begin, each UM8259A-2 in the system must be brought to a starting point by a sequence of 2 to 4 bytes timed by $\overline{WR}$ pulses.
2. Operation Command Words (OCWs): These are the command words which command the UM8259A-2 to operate in various interrupt modes. These modes are:
   a. Fully nested mode
   b. Rotating priority mode
   c. Special mask mode
   d. Polled mode

The OCWs can be written into the UM8259A-2 anytime after initialization.

Initialization Command Words (ICWs)

General

Whenever a command is issued with A0=0 and D4=1, this is interpreted as Initialization Command Word 1 (ICW1). ICW1 starts the initialization sequence during which the

following automatically occur.

a. The edge sense circuit is reset, which means that following initialization, an interrupt request (IR) input must make a low-to-high transition to generate an interrupt.
b. The Interrupt Mask Register is cleared.
c. IR7 input is assigned priority 7.
d. The slave mode address is set to 7.
e. Special Mask Mode is cleared and Status Read is set to IRR.
f. If IC4=0, then all functions selected in ICW4 are set to zero. (Non-Buffered mode*, no Auto-EOI, MCS-80, 85 system).

*Note: Master/Slave in ICW4 is only used in the buffered mode.

Initialization Command Words 1 and 2 (ICW1, ICW2)

A_5-A_{15}: Page starting address of service routines. In an MCS 80/85 system, the 8 request levels will generate CALLs to 8 locations equally spaced in memory. These can be programmed to be spaced at intervals of 4 or 8 memory locations, thus the 8 routines will occupy a page of 32 or 64 bytes, respectively.

The address format is 2 bytes long (A_0-A_{15}). When the routine interval is 4, A_0-A_4 are automatically inserted by the UM8259A-2. While A_5–A_{15} are programmed externally. When the routine interval is 8, A_0-A_5 are automatically inserted by the UM8259A-2, while A_6-A_{15} are programmed externally.

The 8-byte interval will maintain compatibility with current software, while the 4-byte interval is best for a compact jump table.

In an iAPX 86 system A_{15}-A_{11} are inserted in the five most significant bits of the vectoring byte and the UM8259A-2 sets the three least significant bits according to the interrupt level. A_{10}-A_5 are ignored and ADI (Address interval) has no effect.

LTIM: If LTIM=1, then the UM8259A-2 will operate in the level interrupt mode. Edge detect logic on the interrupt inputs will be disabled.

ADI: CALL address interval. ADI=1 then interval=4; ADI=0 then interval=8.

SNGL: Single. Means that this is the only UM8259A-2 in the system. If SNGL=1 no ICW3 will be issued.

IC4: If this bit is set — ICW4 has to be read. If ICW4 is not needed, set IC4=0.

Initialization Command Word 3 (ICW3)

This word is read only when there is more than one UM8259A-2 in the system and cascading is used, in which case SNGL=0. It will load the 8-bit slave register. The functions of this register are:

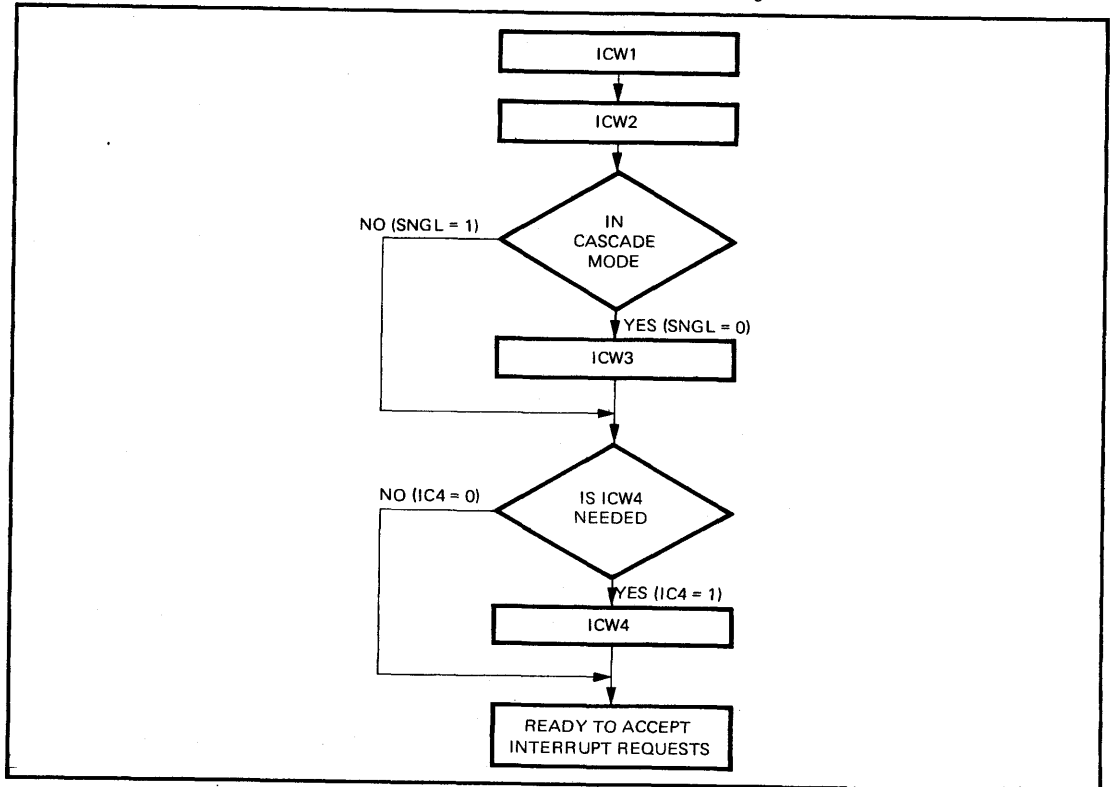
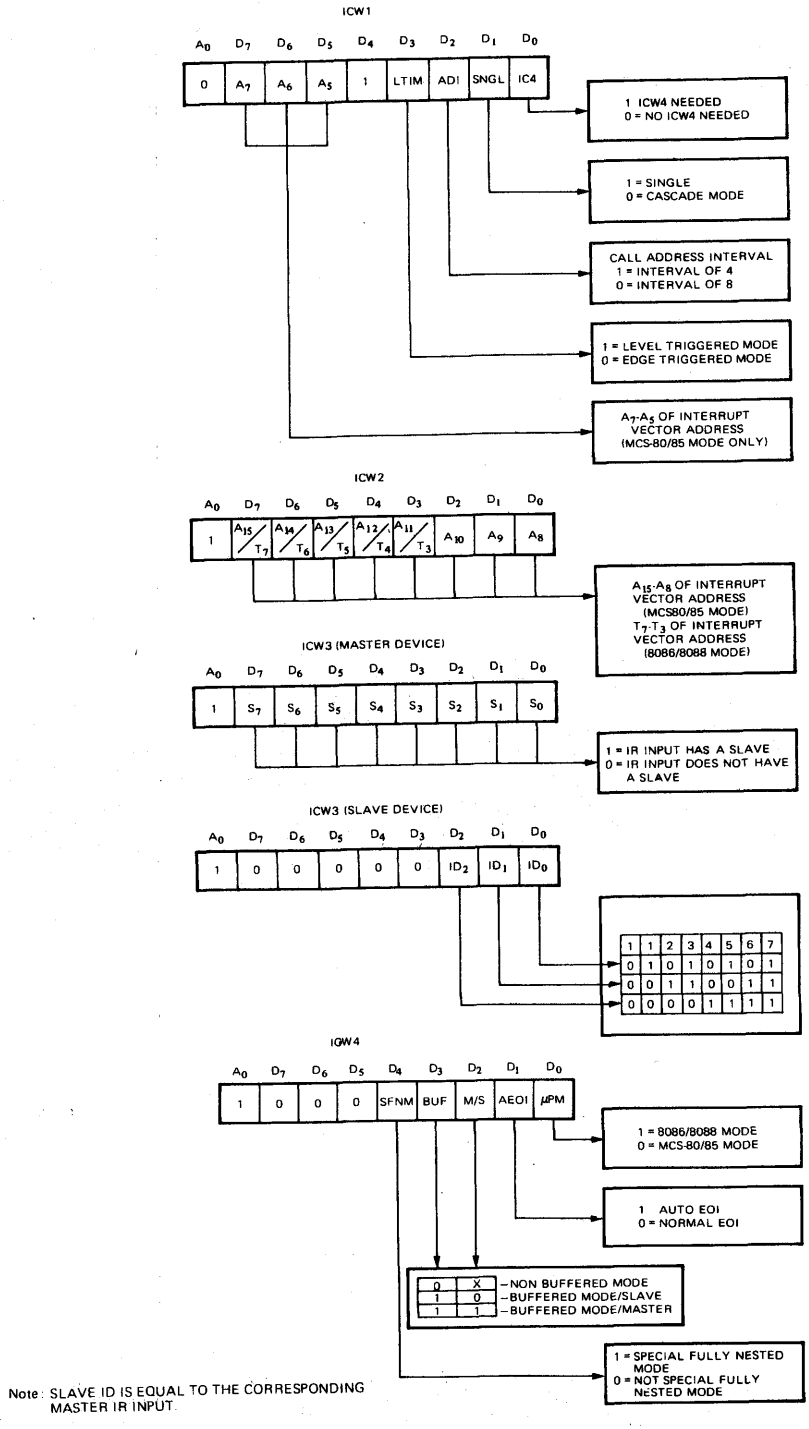


Figure 4. Initialization Sequence



Note: SLAVE ID IS EQUAL TO THE CORRESPONDING MASTER IR INPUT.

Figure 5. Initialization Command Word Format

a. In the master mode (either when SP=1, or in buffered mode when M/S=1 in ICW4) a "1" is set for each slave in the system. The master then will release byte 1 of the call sequence (for MCS-80/85 system) and will enable the corresponding slave to release bytes 2 and 3 (for iAPX 86 only byte 2) through the cascade lines.

b. In the slave mode (either when $\overline{SP}$=0, or if BUF=1 and M/S=0 in ICW4) bits 2-0 identify the slave. The slave compares its cascade input with these bits and, if they are equal, bytes 2 and 3 of the call sequence (or just byte 2 for iAPX 86) are released by it on the Data Bus.

Initialization Command Word 4 (ICW4)

SFNM: If SFNM=1 the special fully nested mode is programmed.

BUF: If BUF=1 the buffered mode is programmed. In buffered mode $\overline{SP}/\overline{EN}$ becomes an enable output and the master/slave determination is by M/S.

M/S: If buffered mode is selected: M/S=1 means the UM8259A-2 is programmed to be a master, M/S=0 means the UM8259A-2 is programmed to be a slave. If BUF=0, M/S has no function.

AEOI: If AEOI=1 the automatic end of interrupt mode is programmed .

μPM: Microprocessor mode: μPM=0 sets the UM8259A-2 for MCS-80, 85 system operation, μPM=1 sets the UM8259A-2 for iAPX 86 system operation.

Operation Command Words (OCWs)

After the Initialization Command Words (ICWs) are programmed into the UM8259A-2, the chip is ready to accept interrupt requests at its input lines. However, during the UM8259A-2 operation, a selection of algorithms can command the UM8259A-2 to operate in various modes through the Operation Command Words (OCWs).

				OCW1				
A0	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	M7	M5	M5	M4	M3	M2	M1	M0
				OCW2				
0	R	SL	EOI	0	0	L2	L1	L0
				OCW3				
0	0	ESMM	SMM	0	1	p	RR	RIS

Operation Control Word 1 (OCW1)

OCW1 sets and clears the mask bits in the interrupt Mask Register (IMR). M_7-M_0 represent the eight mask bits. M=1 indicates the channel is masked (inhibited), M=0 indicates the channel is enabled.

Operation Control Word 2 (OCW2)

R, SL, EOI — These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations can be found on the Operation Command Word Format.

L_2, L_1, L_0 — These bits determine the interrupt level acted upon when the SL bit is active.

Operation Control Word 3 (OCW3)

ESMM — Enable Special Mask Mode. When this bit is set to 1 it enables the SMM bit to set or reset the Special Mask Mode. When ESMM=0 the SMM bit becomes a "don't care".

SMM — Special Mask Mode. If ESMM=1 and SMM=1 the UM8259A-2 will enter Special Mask Mode. If ESMM=1 and SMM=0 the UM8259A-2 will revert to normal mask mode. When ESMM=0, SMM has no effect.

Fully Nested Mode

This mode is entered after initialization unless another mode is programmed. The interrupt requests are ordered in priority from 0 through 7 (0 highest). When an interrupt is acknowledged the highest priority request is determined and its vector placed on the bus. Additionally, a bit of the Interrupt Service register (ISO-7) is set. This bit remains set until the microprocessor issues an End of Interrupt (EOI) command immediately before returning from the service routine, or if AEOI (Automatic End of Interrupt) bit is set, until the trailing edge of the last INTA. While the IS bit is set, all further interrupts of the same or lower priority are inhibited, while higher levels will generate an interrupt (which will be acknowledged only if the microprocessor internal interrupt enable flip-flop has been re-enabled through software).

After the initialization sequence, IR0 has the highest priority and IR7 the lowest. Priorities can be changed, as will be explained, in the rotating priority mode.

End of Interrupt (EOI)

The In Service (IS) bit can be reset either automatically following the trailing edge of the last in sequence $\overline{INTA}$ pulse (when AEOI bit in ICW1 is set) or by a command word that must be issued to the UM8259A-2 before returning from a service routine (EOI command). An EOI command must be issued twice if in the Cascade mode, once for the master and once for the corresponding slave.

There are two forms of EOI command: Specific and Non-Specific. When the UM8259A-2 is operated in modes which preserve the fully nested structure, it can determine which IS bit to reset on EOI. When a Non-Specific EOI command is issued the UM8259A-2 will automatically reset the highest IS bit of those that are set, since in the fully nested mode the highest IS level was necessarily the last level acknowledged and serviced. A non-specific EOI can

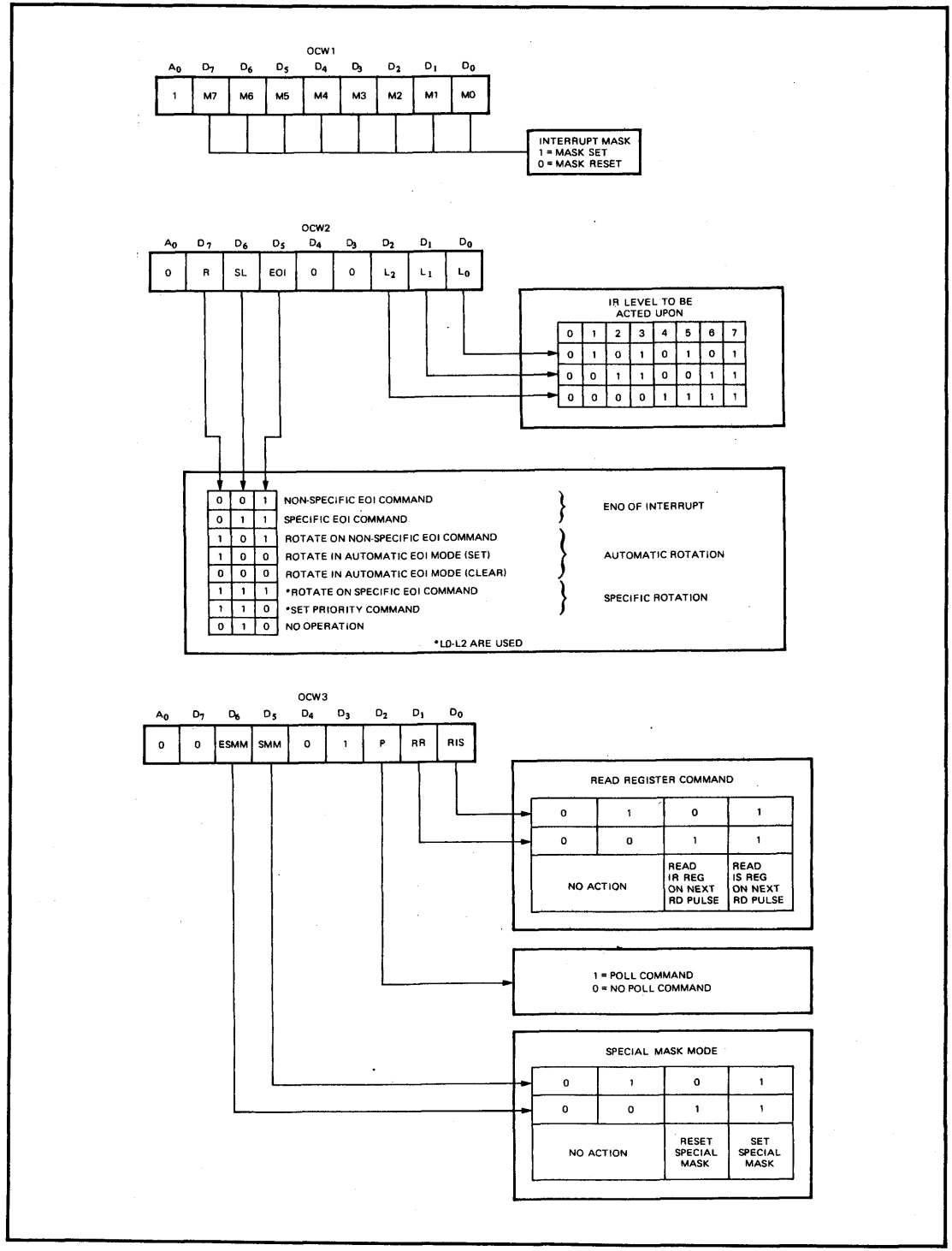


Figure 6. Operation Command Word Format

be issued with OCW2 (EOI=1, SL=0, R=0).

When a mode is used which may disturb the fully nested structure, the UM8259A-2 may no longer be able to determine the last level acknowledged. In this case a Specific End of Interrupt must be issued which includes as part of the command the IS level to be reset. A specific EOI can be issued with OCW2 (EOI=1, SL=1, R=0, and L0-L2 is the binary level of the IS bit to be reset).

It should be noted that an IS bit that is masked by an IMR bit will not be cleared by a non-specific EOI if the UM8259A-2 is in the Special Mask Mode.

Automatic End of Interrupt (AEOI) Mode

If AEOI=1 in ICW4, then the UM8259A-2 will operate in AEOI mode continuously until reprogrammed by ICW4. In this mode the UM8259A-2 will automatically perform a non-specific EOI operation at the trailing edge of the last interrupt acknowledge pulse (third pulse in MCS-80/85, second in iAPX 86). Note that from a system standpoint, this mode should be used only when a nested multilevel interrupt structure is not required within a single UM8259A-2.

The AEOI mode can only be used in a master UM8259A-2 and not a slave.

Automatic Rotation (Equal Priority Devices)

In some applications there are a number of interrupting devices of equal priority. In this mode a device, after being serviced, receives the lowest priority, so a device requesting an interrupt will have to wait, in the worst case until each of 7 other devices are serviced at most once. For example, if the priority and "in service" status is:

Before Rotate (IR4 the highest priority requiring service)

	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
"IS" Status	0	1	0	1	0	0	0	0

	Lowest Priority							Highest Priority
Priority Status	7	6	5	4	3	2	1	0

After Rotate (IR4 was serviced, all other priorities rotated correspondingly)

	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0s
"IS" Status	0	1	0	0	0	0	0	0

	Highest Priority							Lowest Priority
Priority Status	2	1	0	7	6	5	4	3

There are two ways to accomplish Automatic Rotation using OCW2, the Rotation on Non-Specific EOI Command (R=1, SL=0, EOI=1) and the Rotate in Automatic EOI Mode which is set by (R=1, SL=0, EOI=0) and cleared by (R=0, SL=0, EOI=0).

Specific Rotation (Specific Priority)

The programmer can change priorities by programming the bottom priority and thus fixing all other priorities; i.e., if IR5 is programmed as the bottom priority device, then IR6 will have the highest one.

The Set Priority command is issued in OCW2 where: R=1, SL=1; L0-L2 is the binary priority level code of the bottom priority device.

Observe that in this mode internal status is updated by software control during OCW2. However, it is independent of the End of Interrupt (EOI) command (also executed by OCW2). Priority changes can be executed during an EOI command by using the Rotate on Specific EOI command in OCW2 (R=1, SL=1, EOI=1 and L0-L2=IR level to receive bottom priority).

Interrupt Masks

Each Interrupt Request input can be masked individually by the Interrupt Mask Register (IMR) programmed through OCW1. Each bit in the IMR masks one interrupt channel if it is set (1). Bit 0 masks IR0, Bit 1 masks IR1 and so forth. Masking an IR channel does not affect the other channels operation.

Special Mask Mode

Some applications may require an interrupt service routine to dynamically alter the system priority structure during its execution under software control. For example, the routine may wish to inhibit lower priority requests for a portion of its execution but enable some of them for another portion.

The difficulty here is that if an Interrupt Request is acknowledged and an End of Interrupt command did not reset its IS bit (i.e., while executing a service routine), the UM8259A-2 would have inhibited all lower priority requests with no easy way for the routine to enable them.

That is where the Special Mask Mode comes in. In the special Mask Mode, when a mask bit is set in OCW1, it inhibits further interrupts at that level and enables interrupts from all other levels (lower as well as higher) that are not masked.

Thus, any interrupts may be selectively enabled by loading the mask register.

The special Mask Mode is set by OCW3 where: SSMM=1, SMM=1, and cleared where SSMM=1, SMM=0.

Poll Command

In this mode the INT output is not used or the microprocessor internal Interrupt Enable flip-flop is reset, disabling its interrupt input. Service to devices is achieved by software using a Poll command.

The Poll command is issued by setting P="1" in OCW3. The UM8259A-2 treats the next $\overline{RD}$ pulse to the UM8259A-2 (i.e., $\overline{RD}$=0, $\overline{CS}$=0 as an interrupt acknowledgement, sets the appropriate IS bit if there is a request, and reads the priority level. Interrupt is frozen from $\overline{WR}$ to $\overline{RD}$.

The word enabled onto the data bus during $\overline{RD}$ is:

D7	D6	D5	D4	D3	D2	D1	D0
1	–	–	–	–	W2	W1	W0

W0-W2: Binary code of the highest priority level requesting service.

I: Equal to a "1" if there is an interrupt.

This mode is useful if there is a routine command common to several levels so that the $\overline{INTA}$ sequence is not needed (saves ROM space). Another application is to use the poll mode to expand the number of priority levels to more than 64.

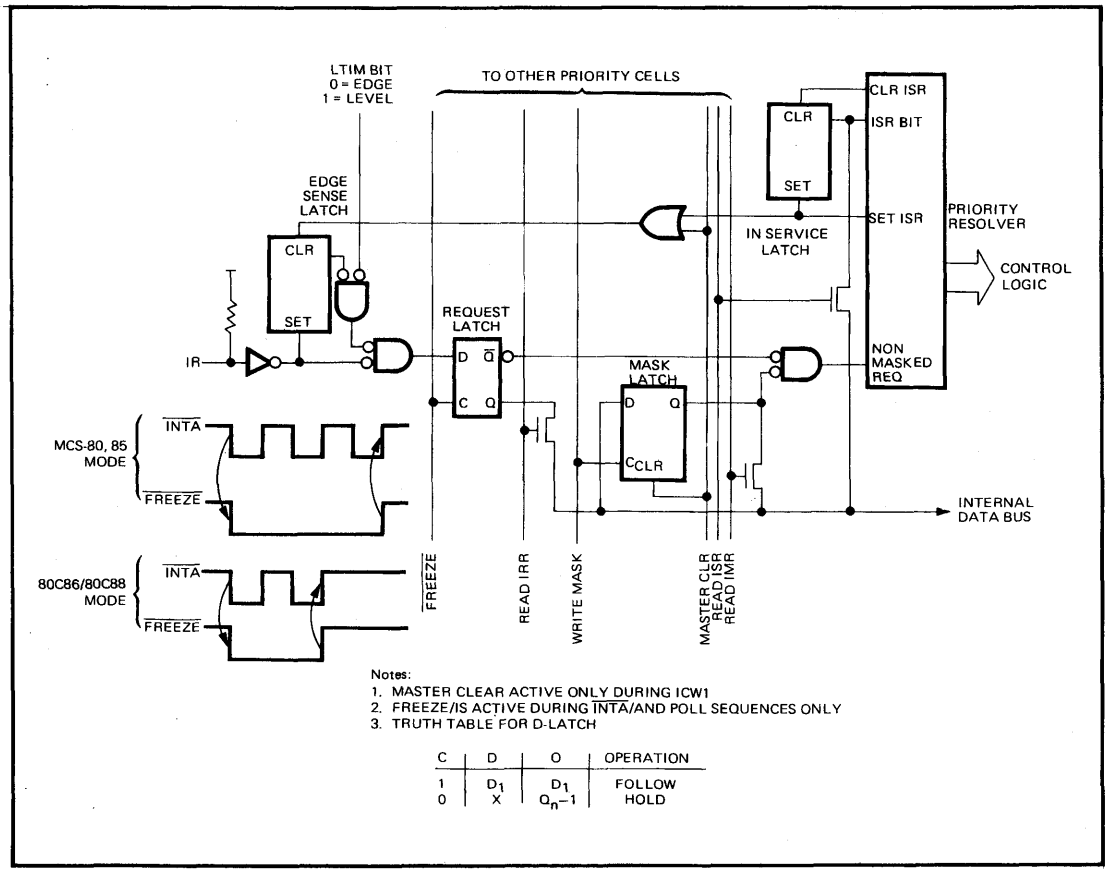
Reading the UM8259A-2 Status

The input status of several internal registers can be read to update the user information on the system. The following registers can be read via OCW3 (IRR and ISR or OCW1 [IMR]).

Interrupt Request Register (IRR): 8-bit register which contains the levels requesting an interrupt to be acknowledged. The highest request level is reset from the IRR when an interrupt is acknowledged. (Not affected by IMR.).

In-Service Register (ISR): 8-bit register which contains the priority levels that are being serviced. The ISR is updated when an End of Interrupt Command is issued.

Interrupt Mask Register: 8-bit register which contains the interrupt request lines which are masked.



Notes:
1. MASTER CLEAR ACTIVE ONLY DURING ICW1
2. FREEZE/IS ACTIVE DURING $\overline{INTA}$/AND POLL SEQUENCES ONLY
3. TRUTH TABLE FOR D-LATCH

C	D	O	OPERATION
1	D_1	D_1	FOLLOW
0	X	Q_{n-1}	HOLD

Figure 7. Priority Cell—Simplified Logic Diagram

The IRR can be read when, prior to the RD pulse, a Read Register Command is issued with OCW3 (RR=1, RIS=0.).

The ISR can be read when, prior to the RD pulse, a Read Register Command is issued with OCW3 (RR=1, RIS=1).

There is no need to write an OCW3 before every status read operation, as long as the status read corresponds with the previous one; i.e., the UM8259A-2 "remembers" whether the IRR or ISR has been previously selected by the OCW3. This is not true when poll is used.

After initialization the UM8259A-2 is set to IRR.

For reading the IMR, no OCW3 is needed. The output data bus will contain the IMR whenever $\overline{RD}$ is active and AO=1 (OCW1).

Polling overrides status read when P=1, RR=1 in OCW3.

Edge and Level Triggered Modes

This mode is programmed using bit 3 in ICW1.

If LTIM='0', an interrupt request will be recognized by a low to high transition on an IR input. The IR input can remain high without generating another interrupt.

If LTIM='1', an interrupt request will be recognized by a 'high' level on IR Input, and there is no need for an edge detection. The interrupt request must be removed before the EOI command is issued or the CPU interrupt is enabled to prevent a second interrupt from occurring.

The priority cell diagram shows a conceptual circuit of the level sensitive and edge sensitive input circuitry of the UM8259A-2. Be sure to note that the request latch is a transparent D type latch.

In both the edge and level triggered modes the IR inputs must remain high until after the falling edge of the first INTA. If the IR input goes low before this time a DEFAULT IR7 will occur when the CPU acknowledges the interrupt. This can be a useful safeguard for detecting interrupts caused by spurious noise glitches on the IR inputs. To implement this feature the IR7 routine is used for "clean up" simply executing a return instruction, thus ignoring the interrupt. If IR7 is needed for other purposes a default IR7 can still be detected by reading the ISR. A normal IR7 interrupt will set the corresponding ISR bit, a default IR7 won't. If a default IR7 routine occurs during a normal IR7 routine, however, the ISR will remain set. In this case it is necessary to keep track of whether or not the IR7 routine was previously entered. If another IR7 occurs it is a default.

The Special Fully Nested Mode

This mode will be used in the case of a big system where cascading is used, and the priority has to be conserved within each slave. In this case the fully nested mode will be programmed to the master (using ICW4). This mode is similar to the normal nested mode with the following exceptions:

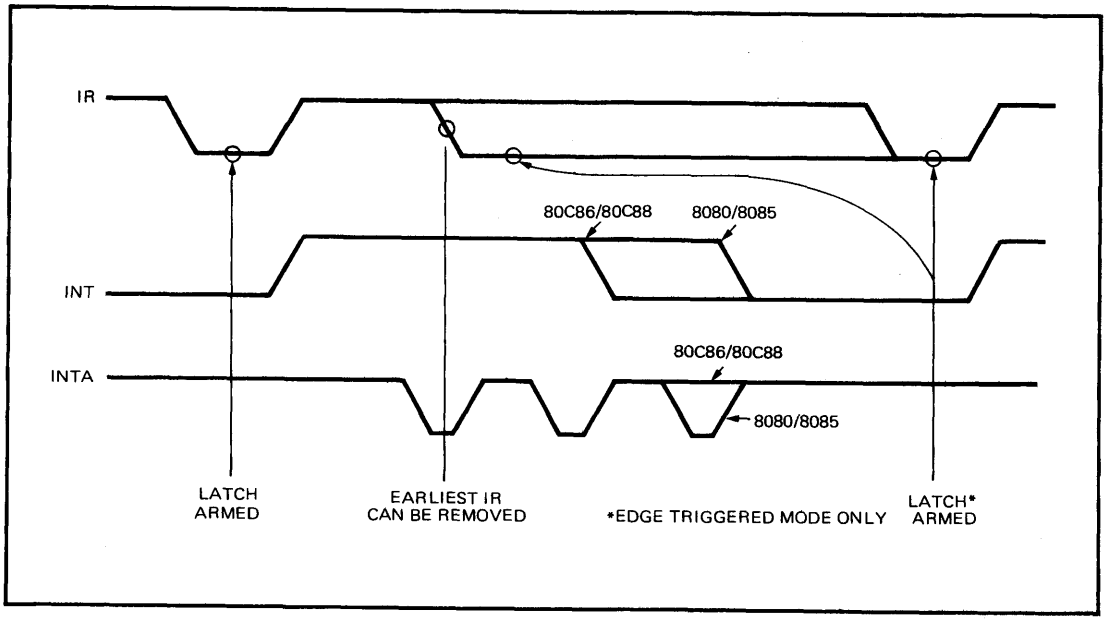


Figure 8. IR Triggering Timing Requirements

a. When an interrupt request from a certain slave is in service this slave is not locked out from the master's priority logic and further interrupt requests from higher priority IR's within the slave will be recognized by the master and will initiate interrupts to the processor. (In the normal nested mode a slave is masked out when its request is in service and no higher requests from the same slave can be serviced.)

b. When exiting the Interrupt Service routine the software has to check whether the interrupt serviced was the only one from that slave. This is done by sending a non-specific End of Interrupt (EOI) command to the slave and then reading its In-Service register and checking for zero. If it is empty, a non-specific EOI can be sent to the master too. If not, no EOI should be sent.

Buffered Mode

When the UM8259A-2 is used in a large system where bus driving buffers are required on the data bus and the cascading mode is used, there exists the problem of enabling buffers.

The buffered mode will structure the UM8259A-2 to send an enable signal on $\overline{SP}/\overline{EN}$ to enable the buffers. In this mode, whenever the UM8259A-2's data bus outputs are enabled, the $\overline{SP}/\overline{EN}$ output becomes active.

This modification forces the use of software programming to determine whether the UM8259A-2 is a master or a slave. Bit 3 in ICW4 programs the buffered mode, and bit 2 in ICW4 determines whether it is a master or a slave.

Cascade Mode

The UM8259A-2 can be easily interconnected in a system of one master with up to eight slaves to handle up to 64 priority levels.

The master controls the slaves through the 3 line cascade bus. The cascade bus acts like chip selects to the slaves during the $\overline{INTA}$ sequence.

In a cascade configuration, the slave interrupt outputs are connected to the master interrupt request inputs. When a slave request line is activated and afterwards acknowledged, the master will enable the corresponding slave to release the device routine address during bytes 2 and 3 of INTA. (Byte 2 only for 8086/8088).

The cascade bus lines are normally low and will contain the slave address code from the trailing edge of the first INTA pulse to the trailing edge of the third pulse. Each UM8259A-2 in the system must follow a separate initialization sequence and can be programmed to work in a different mode. An EOI command must be issued twice: once for the master and once for the corresponding slave. An address decoder is required to activate the Chip Select (CS) input of each UM8259A-2.

The cascade lines of the Master UM8259A-2 are activated only for slave inputs, non slave inputs leave the cascade line inactive (low).

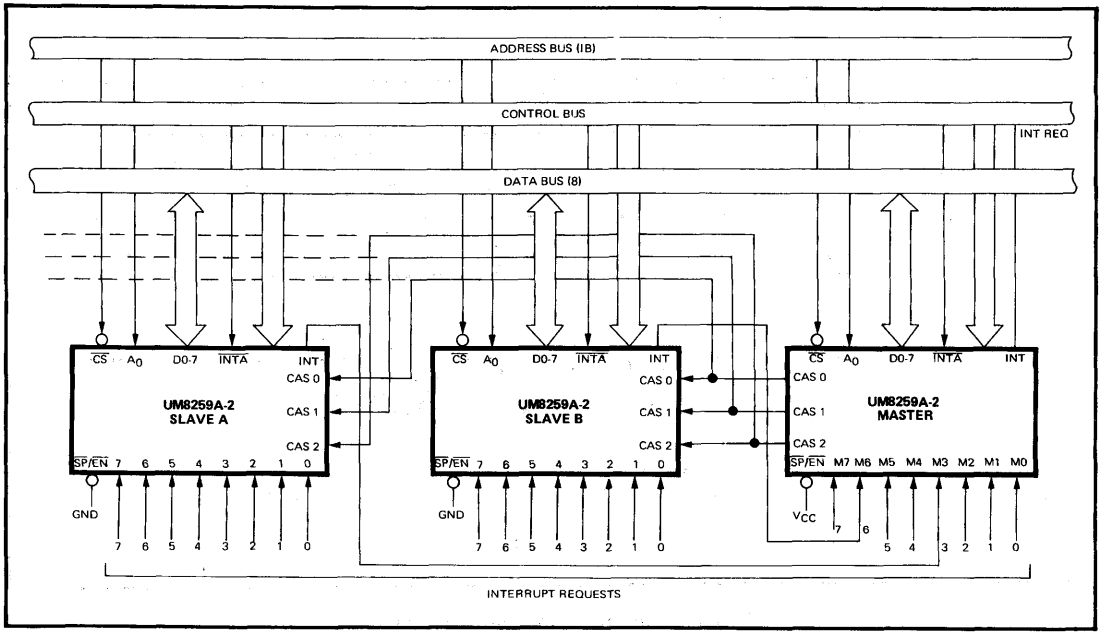


Figure 9. Cascading the UM8259A-2

Display

Part No.	Description	Page
UM487	HCGA Controller	3-3
UM587	VGA Controller	3-17
UM6845/A/B	CRT Controller	3-45
UM6845R/RA/RB	CRT Controller	3-68
UM6845E/EA/EB	CRT Controller	3-81
UM70C171/-50/-65	Color Palette with Triple 6-Bit DAC	3-98

UMC

UM487

PRELIMINARY

HCGA CONTROLLER

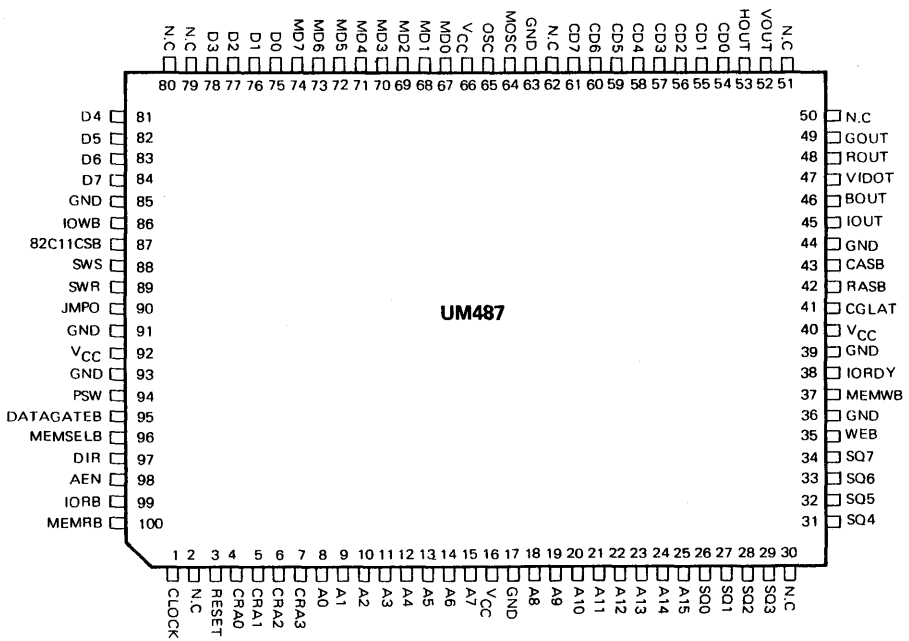
Features

- MGA (Hercules) and CGA compatible
- Built-in 6845 CRTC
- 64K Bytes of video memory
- Flicker-Free operation during CPU read/write
- Minimum circuit board space required
- Display mode changeable using hardware or software
- Optional primary printer port

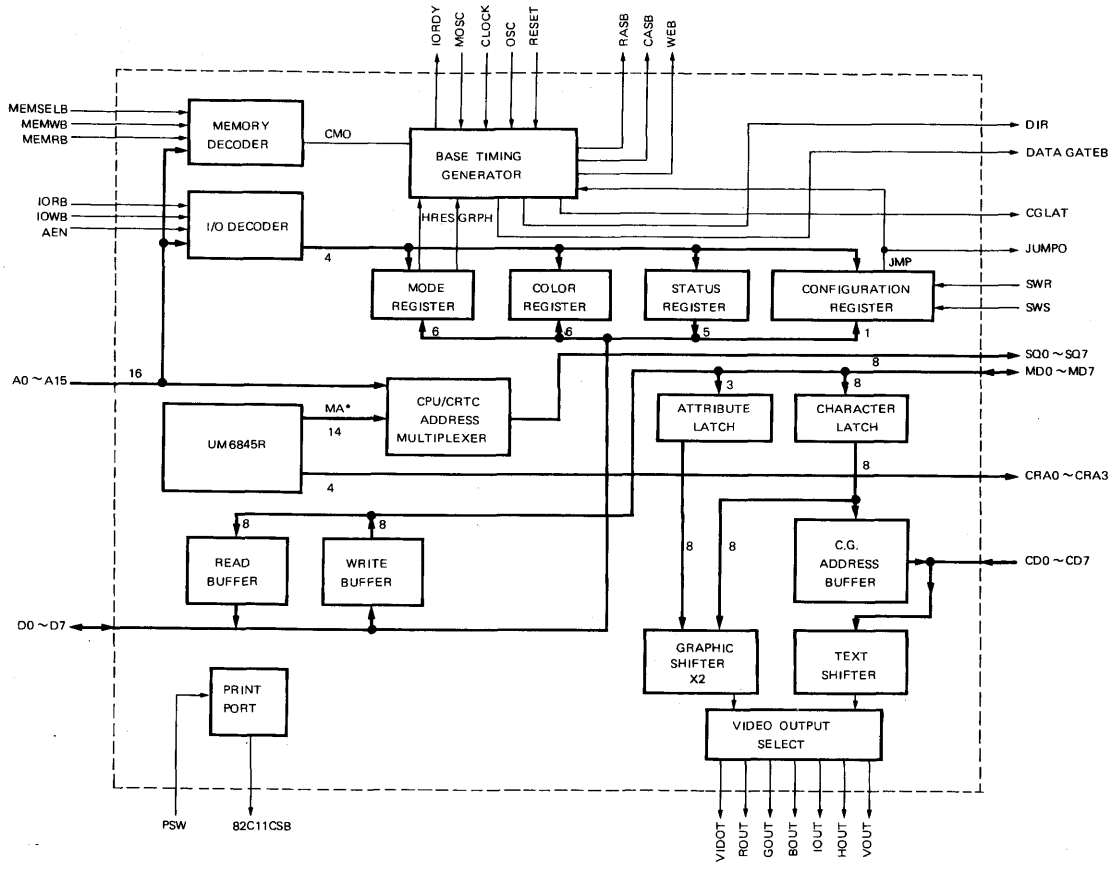
General Description

The UM487 single-chip HCGA controller is an advanced product designed to serve as a combination MGA and CGA through the integration of most of the circuits found on MGA and CGA cards. Built with the UMC 2μm CMOS process, the UM487 incorporates a built-in 6845 CRTC circuit. Thus, for MGA and CGA functions, only a few external components are required to complete the circuits. These include: 64K bytes DRAM; 4 TTLs (74LS374, 74LS245 74LS04 and 74LS20); one character generator (UM2310) and a 16.257 MHz crystal. The UM487 comes packaged in a compact, 100-pin plastic flat pack.

Pin Configuration



Block Diagram



Absolute Maximum Ratings *

Operating Temperature . . . . . 0°C to 70°C
Storage Temperature . . . . . –55°C to 150°C
All Output Voltages . . . . . –0.5V to +7V
All Input Voltages . . . . . –0.5V to +7V
Supply Voltage V_{CC} . . . . . 0V to +7V
Power Dissipation 0.5W

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{CC} = 5V ± 10%, T_A = 0°C to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{IH}	Input Voltage	2.0			V	
V_{IL}				0.8	V	
V_{OH1}	Output Voltage (for SQ0 ~ SQ7	2.4			V	I_{OH} = –6.0 mA
V_{OL1}	IORDY, RASB, CASB, WEB)			0.4	V	I_{OL} = +6.0 mA
V_{OH2}	Output Voltage (other outputs)	2.4			V	I_{OH} = –3.0 mA
V_{OL2}				0.4	V	I_{OH} = +3.0 mA
I_{IL}	Input Leakage	–10		+10	μA	$0 \leqslant V_{in} \leqslant V_{CC}$
I_{OL}	Output Leakage	–10		+10	μA	
I_{OP}	Operating Current			+12	mA	

AC Characteristics (CGA MODE BASE CLOCK 14.318 MHz, MGA MODE BASE CLOCK 16.257 MHz)

C–1 CPU Interface

No.	Symbol	Parameter	Min.	Typ.	Max.	Unit
0	t_{DAC}	DIR, DATAGATEB Active to CPU I/O or Memory Read/Write Cycle			25	ns
1	t_{ASI}	Address Setup Time to IORB, IOWB	30			ns
2	t_{DNC}	DIR, DATAGATEB Non-active to CPU I/O or Memory Read/Write Cycle			20	ns
3	t_{IPW}	IORB, IOWB Active Pulse Width	160			ns
4	t_{DOIR}	Data Output Valid Time to IORB			20	ns
5	t_{DHIR}	Data Output Valid Hold Time to IORB	30			ns
6	t_{DSIW}	Data in Setup Time to IOWB	30			ns
7	t_{DHIW}	Data in Hold Time to IOWB	10			ns
8	t_{ASM}	Address Setup Time to MEMRB, MEMWB	0			ns
9	t_{AMD}	Addr. Valid to MEMCSB Active Delay			15	ns
10	t_{MID}	MEMRB, MEMWB Active to IORDY Low Delay			30	ns
11	t_{MWED}	MEMWB Active to WEB Active Delay	10		2240	ns
12	t_{WDHD}	Memory Write Data Hold Time to WEB	10			ns

C–1 CPU Interface (Continued)

No.	Symbol	Parameter	Min.	Typ.	Max.	Unit
13	t_{DORD}	MEMRB Data Output Valid to IORDY	20	30		ns
14	t_{DOMR}	MEMRB Data Output Valid Hold to MEMRB	20			ns

C–2 DRAM Interface

No.	Symbol	Parameter	Min.	Typ.	Max.	Unit
15	t_{RL}	RASB Low Time		150		ns
16	t_{RH}	RASB High Time		90		ns
17	t_{CL}	CASB Low Time		90		ns
18	t_{CH}	CASB High Time		60		ns
19	t_{RLCL}	RASB ↓ to CASB ↓		60		ns
20	t_{CLRH}	CASB ↓ to RASB ↑		60		ns
21	t_{CHRL}	CASB ↑ to RASB ↓		60		ns
22	t_{RSU}	Row Address Setup Time to RASB ↓	0			ns
23	t_{RHL}	Row Address Hold Time to RASB ↓	20			ns
24	t_{CSU}	Column Addr. Setup Time to CASB ↓	0			ns
25	t_{CHL}	Column Addr. Hold Time to CASB ↓	25			ns
26	t_{ACR}	Access Time from RASB ↓			150	ns
27	t_{ACC}	Access Time from CASB ↓			90	ns
28	t_{WCL}	WEB Active before CASB ↓		40		ns
29	t_{WPW}	WEB Active Pulse Width		90		ns
30	t_{RLW}	RASB to WEB Active Hold		150		ns
31	t_{CAW}	CASB to WEB Active Hold		60		ns
32	t_{WDSC}	Write Data Setup Time to CASB ↓	0			ns
33	t_{WDHC}	Write Data Hold Time to CASB ↓	45			ns
34	t_{WDHR}	Write Data Hold Time to RASB ↓	110			ns
35	t_{DODC}	Data Output Disable Time to CASB ↑	0			ns
36	t_{PCYC}	Page Mode Read Cycle Time	150			ns

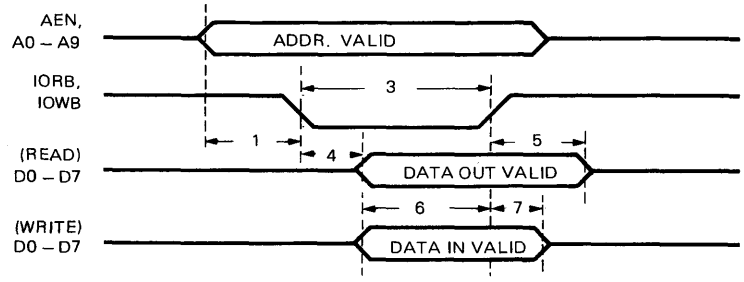
C–3 C. G. Interface

No.	Symbol	Parameter	Min.	Typ.	Max.	Unit
39	t_{CGCH}	CGLAT ↑ to CASB ↑	5		10	ns
40	t_{CGAD}	CGLAT to C. G. Address Valid Delay			10	ns
41	t_{ACC}	C. G. Access Time			250	ns
42	t_{DOHA}	Data Output Hold Time from Addr.	0			ns

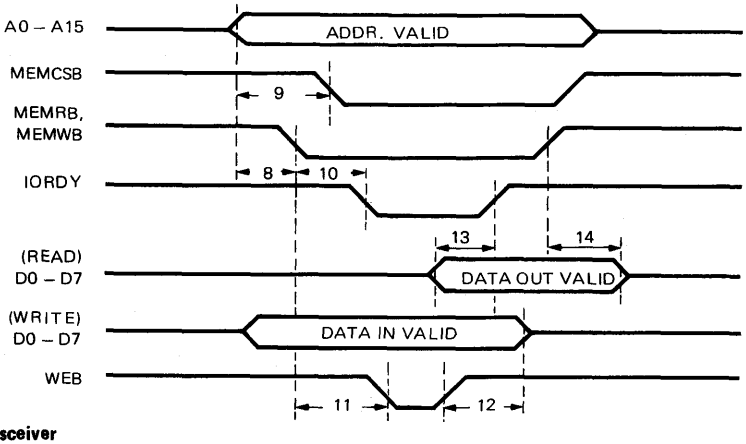
Timing Waveforms

CPU Interface Timing:

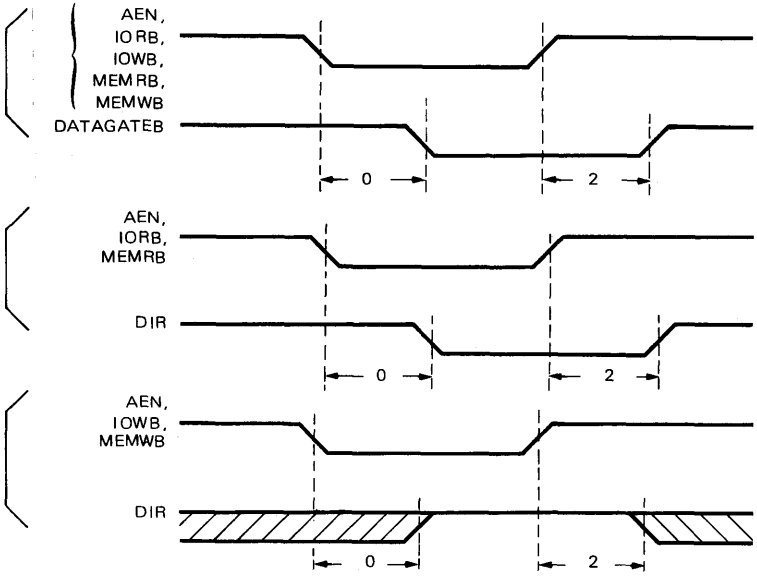
***I/O Cycle**



***Memory Cycle**



*** Bus Transceiver**

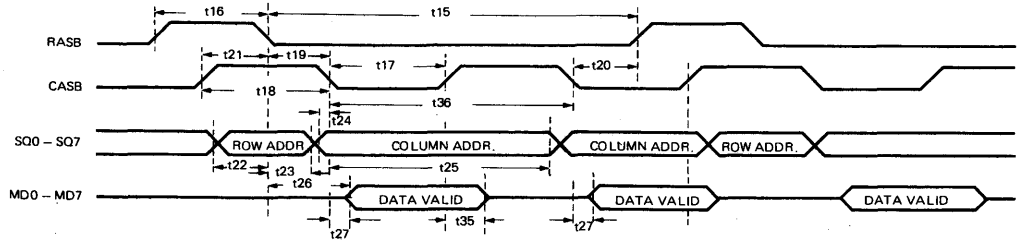


Display

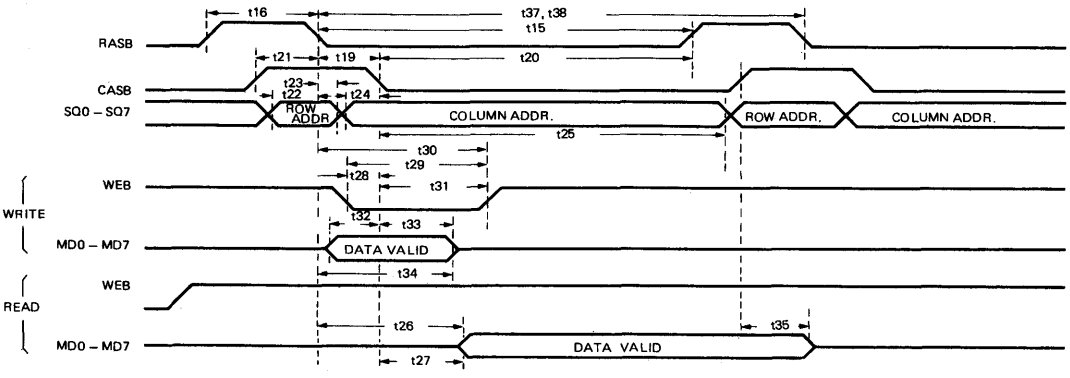
Timing Waveforms (Continued)

DRAM Interface Timing

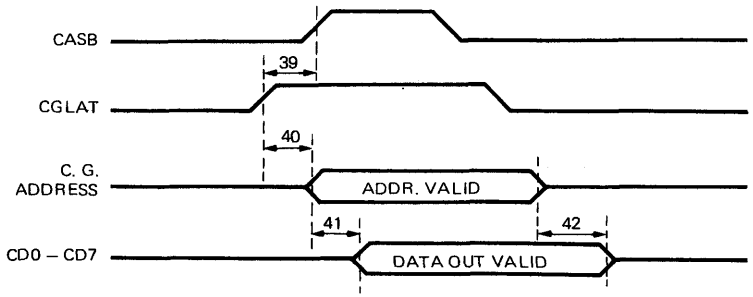
***Page mode Read Cycle**



***Early Write/Read Cycle**



C.G. Interface Timing:



Pin Description

Pin No.	Symbol	I/O	Description
1	CLOCK	I	CPU clock generates built-in 6845 enable signal
3	RESET	I	Chip reset signal, active high
4 ~ 7	CRA0 ~ CRA3	O	Internal 6845 scan line counter, CRA0 is LSB
8 ~ 15 18 ~ 25	A0 ~ A7 A8 ~ A15	I	CPU address bits 0~15, A0 is LSB A15 is MSB
26 ~ 29 31 ~ 34	SQ0 ~ SQ3 SQ4 ~ SQ7	O	Video memory (DRAM) address, SQ0 is LSB
35	WEB	O	Active low, video memory write strobe signal
37	MEMWB	I	Active low, CPU memory write signal
38	IORDY	O	Active high, informs CPU cycle is completed
41	CGLAT	O	Code data latch to C. G. during CGLAT rising edge
42	RASB	O	Video memory row address strobe signal
43	CASB	O	Video memory column address strobe signal
45	IOUT	O	Intensity signal output to RGB monitor
46	BOUT	O	Blue signal output to RGB monitor
47	VIDOT	O	Video dot stream output to monitor
48	ROUT	O	Red signal output to RBG monitor
49	GOUT	O	Green signal output to RBG monitor
52	VOUT	O	Vertical synchronous output to monitor
53	HOUT	O	Horizontal synchronous output to monitor
54 ~ 61	CD0 ~ CD7	I	Character Generator (C. G.) data bus, CD0 is first pixel
64	MOSC	I	MGA mode base clock input (16.257 MHz crystal)
65	OSC	I	CGA mode base clock input (14.318 MHz crystal)
67 ~ 74	MD0 ~ MD7	I/O	Video memory data bus, MD0 is LSB
75 ~ 78 81 ~ 84	D0 ~ D3 D4 ~ D7	I/O	Data bus, D0 is LSB
86	IOWB	I	Active low, CPU I/O write signal
87	82C11CSB	O	Active low, printer controller UM82C11 chip select
88	SWS	I	Active high, to select CGA mode
89	SWR	I	Active high, to select MGA mode
90	JMPO	O	Select CGA/MGA C. G. character font, '0' for MGA
94	PSW	I	Enables primary printer port while PSW is connected to UM82C11 CSB pin
95	DATAGATEB	O	Active low, enables external data transceiver 74LS245

Pin Description (Continued)

Pin No.	Symbol	I/O	Description
96	MEMSELB	I	Active low to select video memory while CPU pins A19 ~ A16 are equal to '1011'
97	DIR	O	Controls external bus transceiver 74LS245 direction '0': from UM487 to CPU during IORB or MEMRB active '1': from CPU to UM487 during IOWB or MEMWB active
98	AEN	I	Active low to enable I/O address
99	IORB	I	Active low, CPU I/O read signal
100	MEMRB	I	Active low, CPU memory read signal
2, 30, 50 51, 62, 79, 80	N. C.	*	No connection
17, 36, 85 39, 44, 93 63, 91	GND	I	Ground
16, 40 66, 92	V_{CC}	I	+5V power supply

* For proper operation, these pins should not be connected.

Register Description

A. Register:

I/O Address		Read/Write	Function	Note
MGA	CGA			
3B4	3D4	W	6845 index register	refer to UM6845R
3B5	3D5	R/W	6845 data register	
3B8	3D8	W	Mode control register	
---	3D9	W	Color select register	
3BA	3DA	R	Status register	
3BB	3DB	W	Light pen reset register	
3B9	3DC	W	Light pen set register	
3BF		W	Configuration register	
3BC		R/W	Primary printer data register	refer to UM82C11
3BD		R	Primary printer status register	
3BE		R/W	Primary printer control word register	

means not used

A-1 Status Register (3?A)

Bit	Logic	MGA (3BA)	CGA (3DA)
0	0 1	Non-horizontal sync. period Horizontal sync. period	Display active period Non-display period
1	0 1	Light pen reset Light pen set	Light pen reset Light pen set
2	0 1	Light pen switch off Light pen switch on	Light pen switch off Light pen switch on
3	0 1	Video dot off Video dot on	Non-vert. sync. period Vertical sync. period
7	0 1	Vertical sync. period Non-vertical sync. period	--- ---

Bits 4, 5 and 6 not used

A-2 Mode Controller Register (3?8)

Bit	Logic	MGA (3B8)	CGA (3D8)
0	0 1	--- ---	40*25 Text 80*25 Text
1	0 1	Text Graphic (while 3BF bit 0 = 1)	Text Graphic
2	0 1	--- ---	Color mode Black/white
3	0 1	Disable video Enable video	Disable video Enable video
4	0 1	--- ---	320*200 Graphic 640*200 Graphic
5	0 1	Disable blink Enable blink	Disable blink Enable blink
6	0 1	Disable change mode Enable change mode	Disable change mode Enable change mode
7	0 1	Page 0 Page 1 (while 3BF bit 1 = 1)	--- ---

A-3 Color Select Register (3D9 CGA Only)

Bit	Function
0	In 40*25 text, select blue of border color In 320*200 graphic, select blue of background color In 640*200 graphic, select blue of foreground color
1	In 40*25 text, select green of border color In 320*200 graphic, select green of background color In 640*200 graphic, select green of foreground color
2	In 40*25 text, select red of border color In 320*200 graphic, select red of background color In 640*200 graphic, select red of foreground color
3	In 40*25 text, select intensity of border color In 320*200 graphic, select intensity of background color In 640*200 graphic, select intensity of foreground color
4	Text mode background color or Graphic mode foreground color
5	Select foreground color pair (only 320*200 graphic)

Bits 6, 7 not used

A-4 Configuration Register (3BF)

Bit	Logic	Function
0	0 1	Disable MGA graphic Enable MGA graphic
1	0 1	Disable MGA page 1 Enable MGA page 1
6	0 1	Select MGA mode (while 3D8 bit6 = 1) Select CGA mode (while 3B8 bit6 = 1)

Other bit not used

A-5 Internal Registers of 6845 (Refer to UM6845R/RA/RB Data Sheet)

Register No.	Function	Unit	Read/ Write
R0	Horizontal total	Char.	W
R1	Horizontal display	Char.	W
R2	Horizontal sync. position	Char.	W
R3	Sync. pulse width	Char.	W
R4	Vertical total	Row	W
R5	Vertical total adjust	Line	W
R6	Vertical display	Row	W
R7	Vertical sync. position	Row	W
R8	Non-interlace mode	---	W
R9	Max. scan line	Line	W
R10	Cursor start	Line	W
R11	Cursor end	Line	W
R12	Start address (H)	---	W
R13	Start address (L)	---	W
R14	Cursor address (H)	---	R/W
R15	Cursor address (L)	---	R/W
R16	Light pen address (H)	---	R
R17	Light pen address (L)	---	R

Functional Description

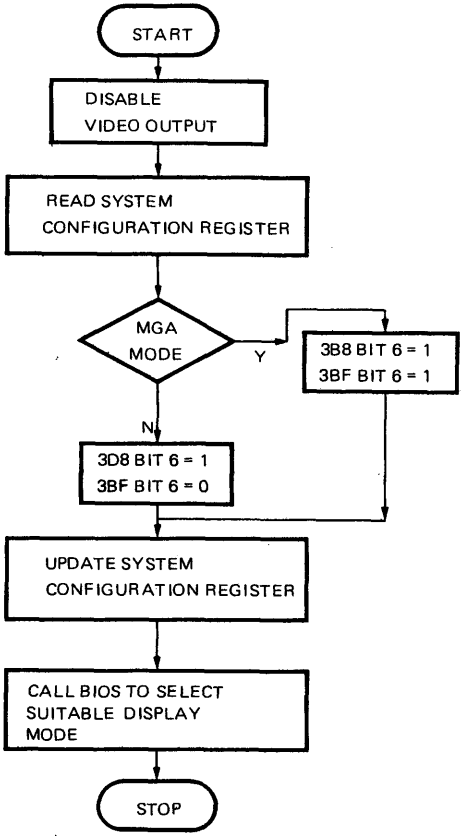
B–1 By HARDWARE

The MGA mode is selected when SW1 pin 2 is connected to pin 3, otherwise CGA mode is active if SW1 pin 2 is connected to pin 1.

B–2 By SOFTWARE

The software changes display mode only if SW3 pin 2 is connected to pin 3 and 3?8 bit 6 is equal to high. (where ? is D or B)

Program Flowchart:

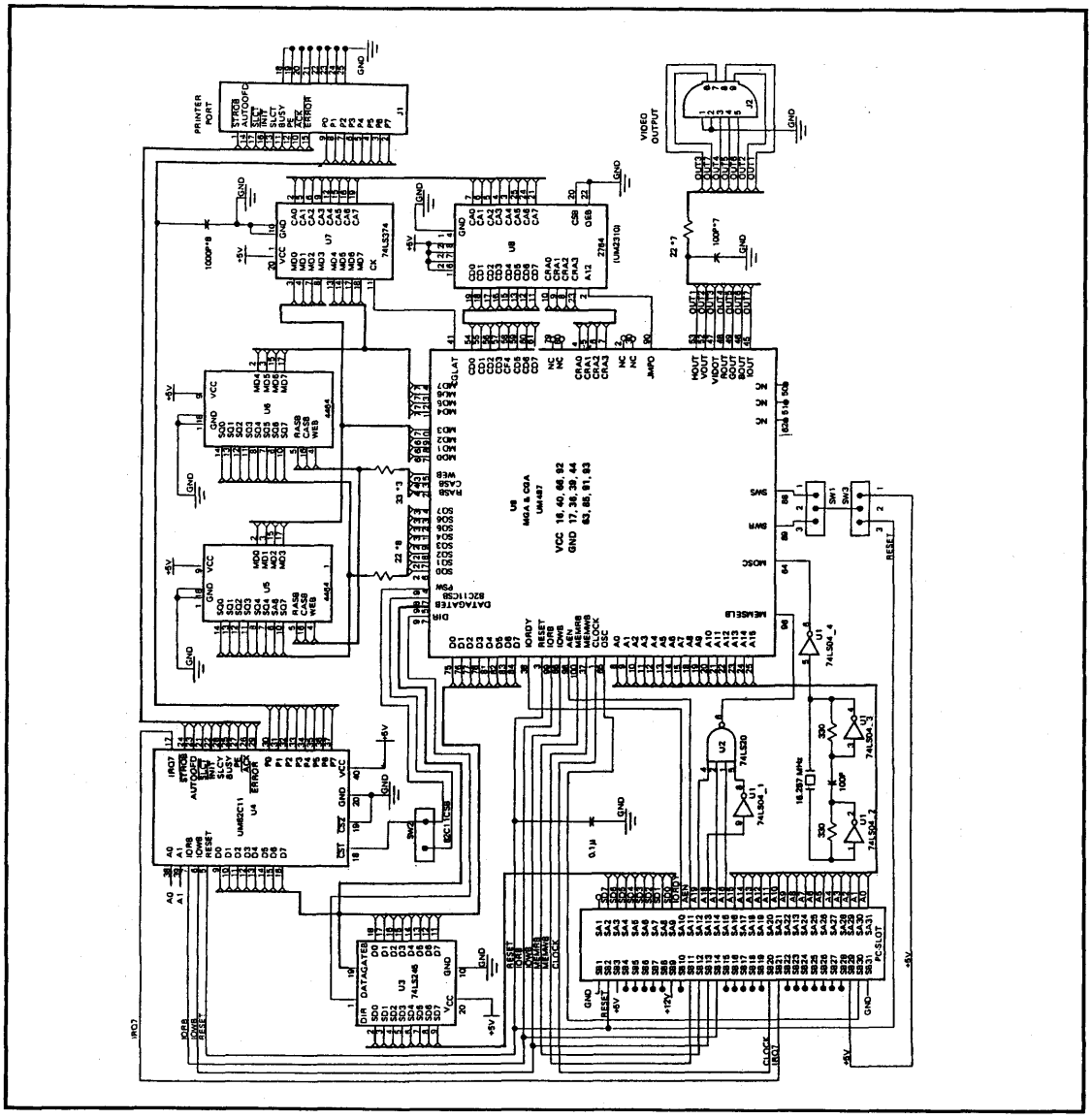


B–3 Program Listing

```
NCOMN   PROC    NEAR
        ASSUME  CS: CODE, DS: DATA, SS: STACK
        PUSH    DS
        MOV     AX, 0
        PUSH    AX
        PUSH    CS
        POP     DS
        MOV     AL, 20H
        MOV     CX, 07D0H
        MOV     BH, 0
        MOV     BL, 07
        MOV     AH, 09          ; clear video memory
        INT     10H
        MOV     AH, 0FH         ; read video state
        INT     10H
        CMP     AL, 07          ; MGA mode?
        JZ      MMM
        JMP     CCC
MMM:    MOV     AL, 40H         ; MGA mode
        MOV     DX, 3B8H        ; enable change mode
        OUT     DX, AL
        MOV     DX, 3BFH
        OUT     DX, AL          ; change to CGA mode
        MOV     AX, 0
        MOV     DS, AX
        MOV     AL, [410]       ; read BIOS configura-
                                  tion register
        AND     AL, CFH         ; isolate bits 4, 5
        OR      AL, 20H         ; update BIOS con-
                                  figuration register
        MOV     [410], AL       ; to CGA mode
        MOV     AH, 0           ; select CGA
        MOV     AL, 3
        INT     10H
        JMP     END
CCC:    MOV     AL, 40H         ; CGA mode
        MOV     DX, 3D8H
        OUT     DX, AL          ; enable change mode
        MOV     AL, 0
        MOV     DX, 3BFH        ; change to MGA mode
        OUT     DX, AL
        MOV     AX, 0
        MOV     DX, AX
        MOV     AL, [410]
        AND     AL, CFH
        OR      AL, 30H         ; update BIOS con-
                                  figuration register
        MOV     [410], AL       ; to MGA mode
        MOV     AH, 0           ; select MGA
        MOV     AL, 7
        INT     10H
END:    RET
NCOMN   ENDP
```

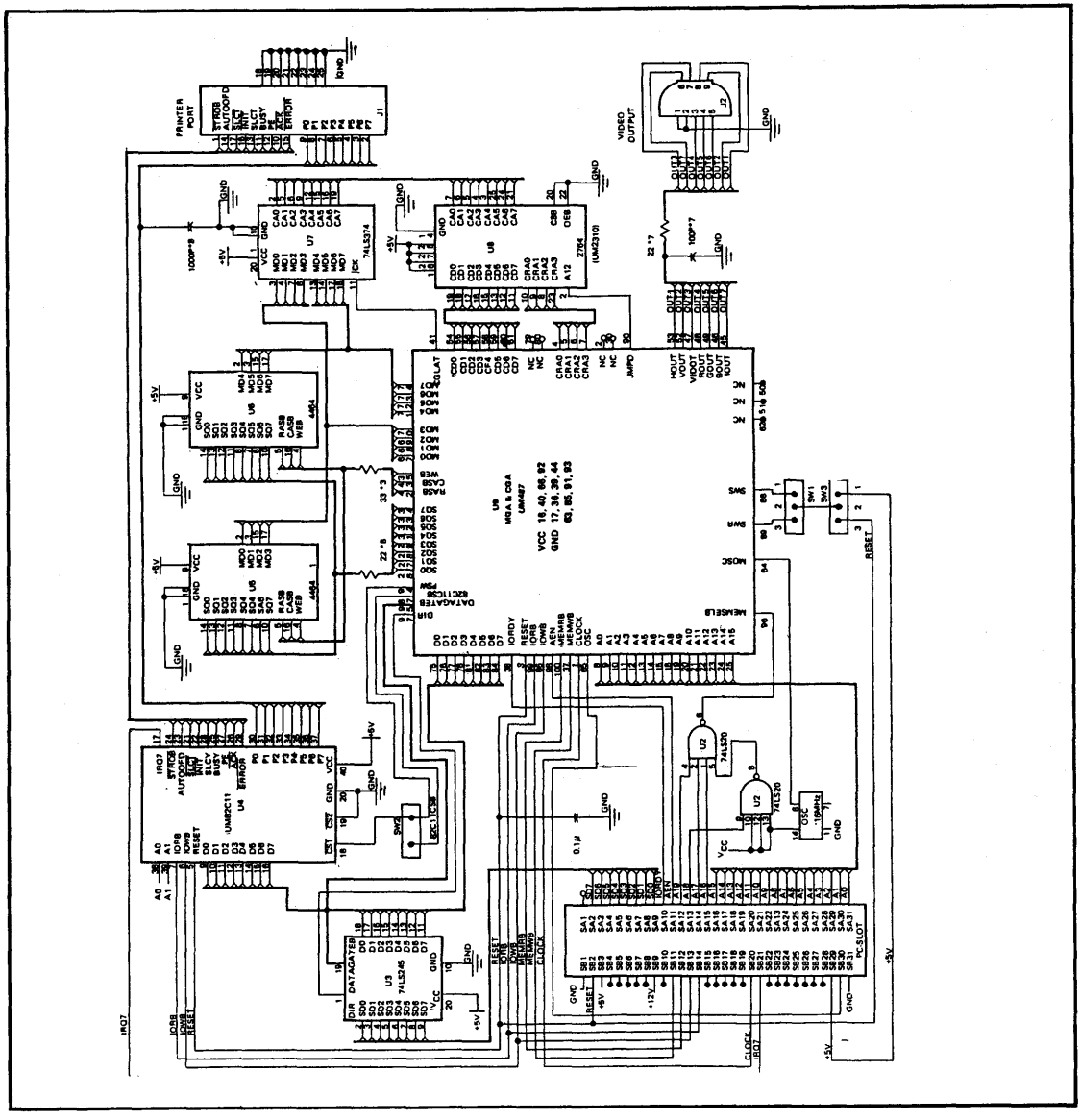
Display

Application Circuits



1. The 74LS04 is used for crystal circuit
2. The 74LS20 decodes CPU A19 ~ A16 to generate MEMCSB while MGA or CGA video memory is selected
3. The 74LS245 is data transceiver between CPU and UM487
4. The 74LS374 latches code data to C. G. during text mode
5. SW1 $\overline{3}\ \overline{2}\ 1$: MGA mode
   SW1 $3\ \overline{2}\ \overline{1}$: CGA mode
6. SW2 is connected while primary printer port is selected
7. SW3 $\overline{3}\ \overline{2}\ 1$: Enable change mode by software
   SW3 $3\ \overline{2}\ \overline{1}$: Disable change mode by software

Application Circuits



1. 16 MHz osc for MGA mode
2. The 74LS20 decodes CPU A19 ~ A16 to generate MEMCSB while MGA or CGA video memory is selected
3. The 74LS245 is data transceiver between CPU and UM487
4. The 74LS374 latches code data to C. G. during text mode
5. SW1 $\overline{3}2\overline{1}$: MGA mode
   SW1 $3\overline{2}\overline{1}$: CGA mode
6. SW2 is connected while primary printer port is selected
7. SW3 $\overline{3}\overline{2}1$: Enable change mode by software
   SW3 $3\overline{2}\overline{1}$: Disable change mode by software

Ordering Information

Part No.	Package
UM487F	100 Pin QFP

UM587

VGA Controller

Features

- Single chip VGA video graphics device fully compatible in the following systems:
  - IBM PC/AT, PC/XT, PS/2
  - IBM VGA (All modes)
  - IBM BIOS (Basic input/output system)
- Provides 800 x 600 element high-resolution graphics with 16 colors
- Flicker-free operation in all video modes
- Supports 132-column text modes
- Supports both digital and analog monitors

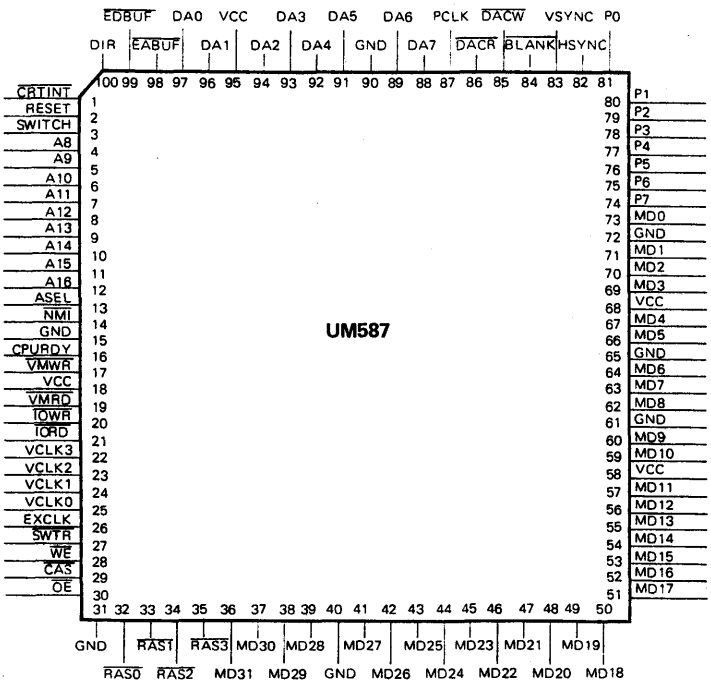
General Description

The UM587 is a single chip, high-integration, high resolution graphics device designed for use in IBM PS/2 model 30, PC/AT and PC/XT compatible systems. It provides high resolution graphics of 800 x 600 elements with 16 colors.

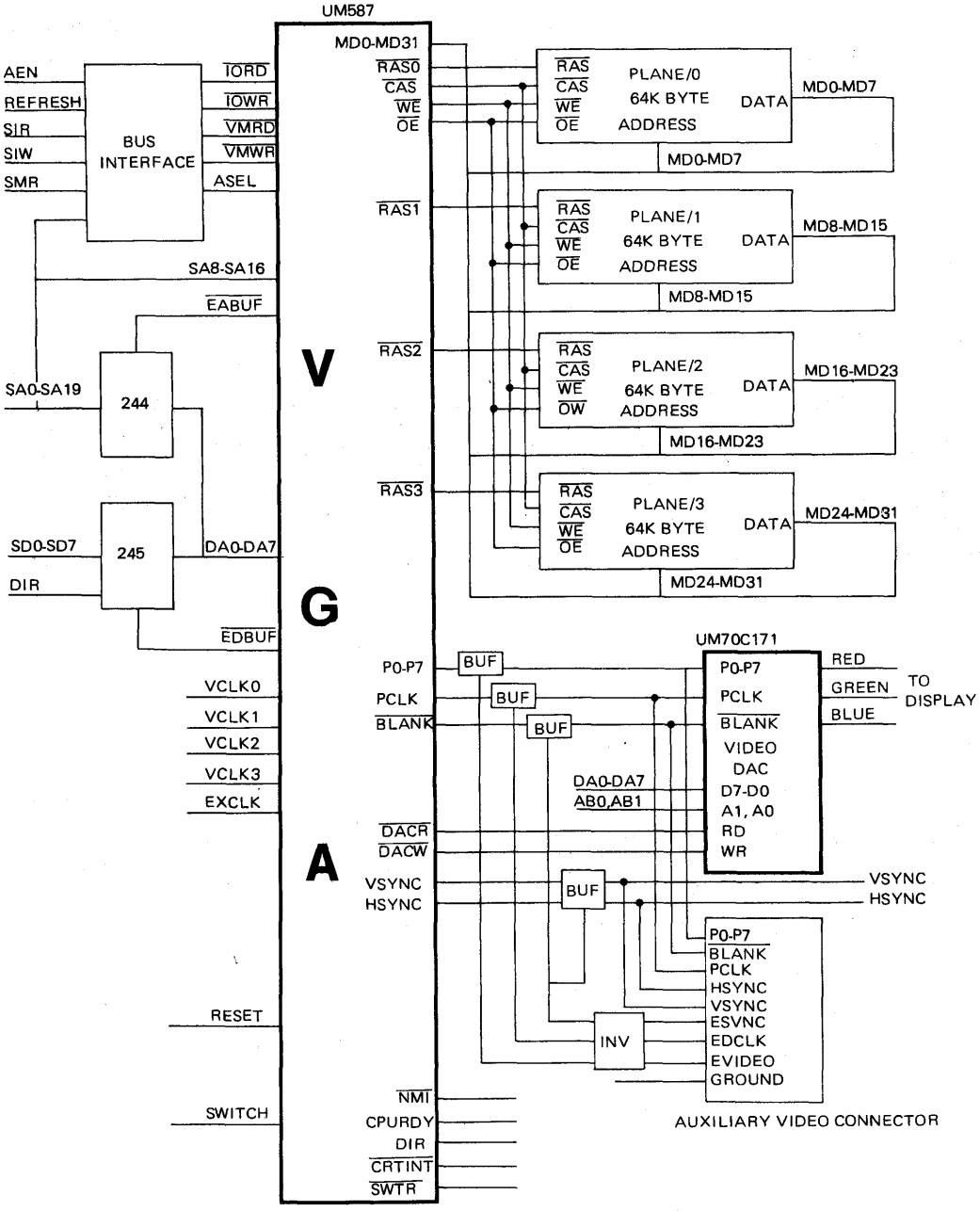
The UM587 also is fully compatible with IBM VGA (all modes). Hercules graphics, EGA, CGA, MDA and IBM BIOS. It is flicker free in all modes and supports an external digital-to-analog look-up table.

Display

Pin Configuration



System Block Diagram



MODE TABLE

Mode	Type	Col x Row	Colors	Pages	Map Addr	CharBox
(HEX)					(HEX)	
00	Text	40 x 25	16	8	B800	8 x 8
01	Text	40 x 25	16	8	B800	8 x 8
02	Text	80 x 25	16	8	B800	8 x 8
03	Text	80 x 25	16	8	B800	8 x 8
00*	Text	40 x 25	16	8	B800	8 x 14
01*	Text	40 x 25	16	8	B800	8 x 14
02*	Text	80 x 25	16	8	B800	8 x 14
03*	Text	80 x 25	16	8	B800	8 x 14
00+	Text	40 x 25	16	8	B800	9 x 16
01+	Text	40 x 25	16	8	B800	9 x 16
02+	Text	80 x 25	16	8	B800	9 x 16
03+	Text	80 x 25	16	8	B800	9 x 16
07	Text	80 x 25	2	8	B000	9 x 14
07+	Text	80 x 25	2	8	B000	9 x 16
04	APA	320 x 200	4	1	B800	8 x 8
05	APA	320 x 200	4	1	B800	8 x 8
06	APA	640 x 200	2	1	B800	8 x 8
0D	APA	320 x 200	16	8	A000	8 x 8
0E	APA	640 x 200	16	4	A000	8 x 8
0F	APA	640 x 350	2	2	A000	8 x 14
10	APA	640 x 350	16	2	A000	8 x 14
11	APA	640 x 480	2	1	A000	8 x 16
12	APA	640 x 480	16	1	A000	8 x 16
13	APA	320 x 200	256	1	A000	8 x 8
50	Text	132 x 25	16	8	B800	8 x 14
51	Text	132 x 43	16	5	B800	8 x 8
52	Text	800 x 600	16	8	A000	8 x 8

Remarks: (1) Modes 0, 1, 2, 3 0*, 1*, 2*, 3* 0+, 1+, 2+, 3+ differ in CharBox size and display scan lines.

(2) Mode 3+ or 7+ is the default mode at power-up time.

Pin Description

Pin No.	Symbol	I/O	Description
1	$\overline{\text{CRTINT}}$	O	Display vertical retrace interrupt. An active low open collector.
2	RESET	I	System reset signal, active high.
3	SWITCH	I	Signal that detects the type of monitor.
4-12	A8-A16	I	CPU address bus bits 8 through 16.
13	ASEL	I	Active high, to select VGA address to decode.
14	$\overline{\text{NM}}$	O	Non maskable interrupt. An active low open collector.
16	CPURDY	O	An open collector active high output. Signals processor that it is ready for memory access.
17	$\overline{\text{VMWR}}$	I	Active low, video memory write signal.
19	$\overline{\text{VMRD}}$	I	Active low, video memory read signal.
20	$\overline{\text{IOWR}}$	I	Active low, I/O write signal.
21	$\overline{\text{IORD}}$	I	Active low, I/O read signal.
22	VCLK3	I	35.5 MHz input clock signal.
23	VCLK2	I	Reserved
24	VCLK1	I	28.322 MHz input clock signal.
25	VCLK0	I	25.175 MHz input clock signal.
26	EXCLK	I	External clock signal.
27	$\overline{\text{SWTR}}$	O	Read DIP switch control signal.
28	$\overline{\text{WE}}$	O	Video memory write enable. An active low signal.
29	$\overline{\text{CAS}}$	O	Column address strobe to all planes. An active low signal.
30	$\overline{\text{OE}}$	O	Output enable signal to memory. It is active low.
32-35	$\overline{\text{RAS0}}$, $\overline{\text{RAS3}}$	O	Row address strobe to planes 0-3. An active low signal.
36-39, 41-44	MD31-24	I/O	Display memory address/data time multiplexed bus line 7-0, interface to video memory plane 3.
45-52	MD23-16	I/O	Display memory address/data time multiplexed bus line 7-0, interface to video memory plane 2.
53-57, 59, 60, 62	MD15-8	I/O	Display memory address/data time multiplexed bus line 7-0, interface to video memory plane 1.
63, 64, 66, 67, 69-71, 73	MD7-0	I/O	Display memory address/data time multiplexed bus line 7-0, interface to video memory plane 0.
74-81	P7-P0	O	Video color look up table address bits 7-0.
82	HSYNC	O	Horizontal SYNC signal for monitor.
83	VSYNC	O	Vertical SYNC signal for monitor.
84	$\overline{\text{BLANK}}$	O	An active low blanking signal to external palette chip.
85	$\overline{\text{DACW}}$	O	An active low I/O write signal for external palette chip (256 color look up table).

Pin Description (Continued)

Pin No.	Symbol	I/O	Description
86	$\overline{DACR}$	O	An active low I/O read signal for external palette chip (256 color look up table).
87	PCLK	O	Pixel clock signal for external palette chip (256 color look up table).
88, 89, 91-94 96, 97	DA7-DA0	I/O	Multiplexed address/data bus bits 7 through 0.
98	$\overline{EABUF}$	O	Active low, enable external address buffer.
99	–EDBUF	O	Active low, enable external data buffer.
100	DIR	O	Control signal for bidirectional data bus transceiver.
18, 58 68, 95	VCC		Power: +5V Supply
15, 31, 40, 61 65, 72, 90	GND		Ground

Functional Description

Introduction

The single chip VGA is a standard video graphic controller for PS/2 model 30 and PC/XT/AT systems. Compared to earlier version video graphic controllers, several new features have been added, including higher resolution (640 x 480), new video mode, 256 color support for 320 x 200 graphics mode, up to 64 shades of grey display for monochrome monitors, and eight fonts loaded into video RAM simultaneously.

The host can access both VGA registers and video memory by setting the bus address and read/write commands to read or write 8-bit data. Video RAM and screen refresh activities occur concurrently and independently by assigning appropriate memory access cycles to each of them.

Most registers are readable so that BIOS and driver software are able to determine current state of video. In the basic configuration, 256K bytes of memory are needed as the display buffer. Four planes of video memory are controlled by four different-RAS (Row Address Strobe) signals and one-CAS (Column Address Strobe), one $\overline{WE}$ (Write Enable), one $\overline{OE}$ (Output Enable) Signal. The Video data bus is time multiplexed with the video address bus in a way that outputs RAS and CAS address early in the memory cycle and inputs 8-bit data for read or outputs 8-bit data for write late in the memory cycle.

NMI (Non-Maskable Interrupt) is generated by trapping some particular I/O ports so that backward compatibility can be done through the BIOS. The VGA chip will provide a 'DIRectional' signal to control the data flow to the system data bus for CPU Read or Write.

Major Components

There are four major components of the UM587 contained in a single 100-pin plastic flatpack. They are described below:

CRT Controller

The UM587 CRT Controller provides synchronization control, timing generation and supplies video memory address to display memory. Flexible timing configuration options are allowed by accessing I/O registers through software control. During the blanking period, an 8-bit refresh counter is placed on the memory address lines. A split screen feature is also provided to allow two windows.

Sequencer

The UM587 Sequencer takes care of basic memory timing for the display memory and the character clock for the control of memory fetches.

The intelligent state machine in the Sequencer automatically assigns appropriate memory access cycles to both the CPU and CRT Controller during active display period. The sequencer can also protect the entire memory plane by selectively masking out planes through the Mask

register.

Graphics Controller

The Graphics Controller provides a data path for both CPU Read/Write and CRT Read access to the display memory. For CRT access it directs data to the Attribute Controller while the CPU access directs data to the system bus instead. It handles two basic modes: alphanumeric and graphics. In the alphanumeric mode, the data is sent in parallel directly to the Attribute Controller. In the graphics mode the memory data is shifted out serially to the Attribute Controller. The data formatting and manipulation are implemented for various modes. Color comparator is provided for fast color comparison in the application of color painting modes. Since the Graphics Controller can process 32-bit data (8-bits from each plane) at a time, a fast color presetting and area fill operation can be achieved.

Attribute Controller

The UM587 Attribute Controller provides video shifting, attribute processing and an internal palette of 16 colors selectable from a possible 64 colors. Pixel panning is also provided for both graphics and text modes. Underline, cursor and blinking logic are interpreted and manipulated here. The final output of the Attribute Controller is an 8-bit wide color data that is sent to the external color look-up table for final color mapping.

Memory and Clock Consideration

In basic configuration, eight 64K x 4-bit dynamic RAM's should be used to configure 256K bytes of video memory. The supported DRAM and CLOCK speeds are related to the graphics resolution as shown in Table 1.

Table 1. Resolution Requirements

Dram	120 ns	120 ns	100 ns
Clock	28 MHz	25 MHz	36 MHz
Resolution	720 x 400	640 x 480	800 x 600
Colors	16	16	16

VGA Registers

All registers in the VGA can be categorized into six groups for the different function blocks in the hardware. In the UM587 VGA chip, the system microprocessor data latches are readable for faster save and restore of the VGA state in the VGA BIOS. The VGA also provides the system microprocessor interface for the video DAC (external color palette chip). The DAC has one address register which can be accessed through address hex 03C7 for read, and hex 03C8 for write. Table 2 lists the registers and the I/O address where they are located. It also lists whether or not they are Read/Write, Read-Only, or Write-Only.

Note that the PEL Mask Register must not be written to by application code or destruction of the color look-up table may occur.

Table 2. VGA Registers

Register Group	R/W	Mono Emulation	Color Emulation
General Registers			
Miscellaneous	W	03C2	03C2
	R	03CC	03CC
Input Status 0	RO	03C2	03C2
Input Status 1	RO	03BA	03DA
Feature Control	W	03BA	03DA
	R	03CA	03CA
VGA Enable	RW	03C3	03C3
DAC State	R	03C7	03C7
Sequencer Registers			
Address Register	RW	03C4	03C4
Data Registers	RW	03C5	03C5
CRTC Registers			
Address Register	RW	03B4	03D4
Data Registers	RW	03B5	03D5
Graphics Registers			
Address Register	RW	03CE	03CE
Data Registers	RW	03CF	03CF
Attribute Registers			
Address Register	RW	03C0	03C0
Data Registers	W	03C0	03C0
	R	03C1	03C1
Extended Registers			
Address Register	RW	03DE	03DE
Data Registers	RW	03DF	03DF
DAC Registers			
PEL Address (Write)	RW	03C8	03C8
PEL Address (Read)	WO	03C7	03C7
PEL Data Registers	RW	03C9	03C9
PEL Mask	RW	03C6	03C6

General Registers

This section describes all the general registers. The output is controlled by bit 0 of the Miscellaneous Output Register.

Miscellaneous Output Register

Read-03CC **Write-03C2**

Bit	Description
7	Vertical Sync Polarity
6	Horizontal Sync Polarity
5	Page Bit for Odd/Even
4	Reserved
3	Clock Select bit 1
2	Clock Select Bit 0
1	Enable RAM
0	I/O Address Select

Table 3. General Registers

Name	Read Port	Write Port	Index
Miscellaneous Output	03CC	03C2	–
Input Status 0	03C2	–	–
Input Status 1	03?A	–	–
Feature Control	03CA	03?A	–
VGA Enable	03C3	03C3	–
DAC State	03C7	–	–

Table 4. Vertical Size Registers

Bit 7	Bit 6	Vertical Size
0	0	Reserved
0	1	400 lines
1	0	350 lines
1	1	480 lines

Bits 7, 6 The Polarity of Vertical/Horizontal Sync is used to select the vertical size as shown in Table 4.

Bit 5 Selects between two pages of memory when in the Odd/Even modes (modes 0-5, 7). A logic 0 selects the low page of memory; a logic 1 selects the high page of memory. This bit is provided for diagnostic use.

Bit 4 Reserved

Bits 3, 2 These two bits select the clock source. In UM587 VGA the third bit is defined in extended register and used with these two bits to select a wider range of clock sources for different video modes. See Table 5.

Bit 1 A logic 0 disables Video RAM address decode from the system microprocessor; a logic 1 enables Video RAM to the system microprocessor

Bit 0 A logic 0 sets CRTC addresses to Hex 03BX and Input Status Register 0's address to 03BA for Monochrome emulation. A logic 1 sets CRTC addresses to Hex 03DX and Input Status Register 0's address to Hex 03DA for color emulation.

Table 5. Clock Registers

CSEL2	CSEL1	CSEL0	Clock
0	0	0	25.175 MHz
0	0	1	28.322 MHz
0	1	0	External Input Clock
0	1	1	Reserved
1	0	0	14.318 MHz
1	0	1	16.257 MHz
1	1	0	Reserved
1	1	1	35.5 MHz

Input Status Register 0

Read-Only **Address = 03C2**

Bits	Description
7	CRT Interrupt
6, 5	Reserved
4	Switch Sense Bit
3-0	Reserved

Bit 7 A logic 1 indicates a vertical retrace interrupt is pending. A logic 0 indicates the vertical retrace interrupt is cleared.

Bit 6, 5 Reserved

Bit 4 This bit allows the power-on initialization to determine if a monochrome or color monitor is connected to the system.

Bit 3-0 Reserved

Input Status Register 1

Read-Only **Address = 03?A**

Bit	Description
7, 6	Reserved
5	Diagnostic 0
4	Diagnostic 1
3	Vertical Retrace
2, 1	Reserved
0	Display Enable

Bits 7, 6 Reserved

Bits 5, 4 These two bits are used for diagnostics. They are connected to two of the eight color out-

Display

puts of the Attribute Controller. The two bits defined in the Color Plane Enable Register to control the multiplexer for color output wiring as described in Table 6.

Bit 3 A logic 1 occurs during a vertical retrace interval. A logic 0 shows the video information is being displayed.

Bits 2, 1 Reserved

Bit 0 A logic 1 indicates a horizontal or vertical retrace interval. A logic 0 indicates that the internal Display Enable Signal is active. To avoid glitches in the display, some programs use this status bit to restrict screen updates to de-activate display intervals. The VGA has been designed to eliminate this software requirement, so display screen updates may be made at any time.

Table 6. Register Bits

Color Plane Register		Input Status 1 Register	
Bit 5	Bit 4	Bit 5	Bit 4
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

Feature Control Register

Read = 03CA **Write = 03?A**

Bit	Description
7-4	Reserved
3	Vertical Sync Select
2-0	Reserved

Bits 7-4 Reserved

Bits 3 This bit should always be set to 0 to enable normal vertical sync output to the monitor; when bit 3 = 1, the "vertical sync" output is the logical OR of "vertical sync" and "vertical display enable".

Bits 2-0 Reserved

Video Subsystem Enable Register

Read-03C3 **Write-03C3**

Bit	Description
7-1	Reserved
0	Video Subsystem Enable

Bits 7-1 Reserved

Bit 0 A logic 1 enables video I/O and memory address decoding. A 0 disables the video I/O and memory address decoding.

Sequencer Registers

This section describes registers in the Sequencer Control block. See Table 7.

Table 7. Sequencer Registers

Register Name	I/O Port	Index
Sequencer Address	03C4	–
Reset	03C5	00
Clocking Mode	03C5	01
Map Mask	03C5	02
Character Map Select	03C5	03
Memory Mode	03C5	04

Sequencer Address Register

Read-03C4 **Write-03C4**

Bit	Description
7-3	Reserved
2-0	Sequencer Address

Bits 7-3 Reserved

Bits 2-0 A binary value pointing to the register where data is to be written or read.

Reset Register

Port = 03C5 **Index 0**

Bit	Description
7-2	Reserved
1	Synchronous Reset
0	Asynchronous Reset

Bits 7-2 Reserved

Bit 1 A logic 0 directs the sequencer to synchronously clear and halt. Bits 1 and 0 must be 1 to allow the sequencer to operate. This bit must be set to 0 before changing either bit 3 or bit 0 of the Clocking Mode register, or bit 3 or bit 2 of the Miscellaneous Output Register, or bit 5, bit 4 or bit 3 of the Bandwidth Control Register.

Bit 0 A logic 0 directs the sequencer to asychronously clear and halt. Bits 1 and 0 must both be 1 to allow the sequencer to operate. Resetting the sequencer with this bit can cause data loss in dynamic RAMs.

Clocking Mode Register

Port = 03C5 **Index 1**

Bit	Description
7, 6	Reserved
5	Screen Off
4	Shift 4
3	Dot Clock
2	Shift Load
1	Reserved
0	8/9 Dot Clocks

Bits 7, 6 Reserved

Bit 5 When set to 1, this bit turns off the video screen and assigns maximum memory bandwidth to the system CPU. A logic 0 puts the screen into normal operation. When this bit is set the screen is blanked. The synchronization pulses are maintained. This bit is used for fast full-screen updates.

Bit 4 When set to 1, the internal shift load registers are loaded every fourth character clock. When set to 0, they are loaded every character clock. When 32 bits are fetched each cycle and used together in the shift registers, this mode is useful.

Bit 3 A logic 0 selects normal dot clock directly from the sequencer master clock input. A logic 1 will select master clock divided by two as dot clock. Normally, dot clock divided by two is used for 320 and 360 horizontal resolution modes.

Bit 2 When set to 1, the internal shift load registers are loaded every other character clock. When set to 0, and bit 4 is set to 0, the internal shift load registers are loaded every character clock. This mode is useful when 16 bits are fetched per cycle and chained together in the shift load registers.

Bit 1 Reserved

Bit 0 A logic 0 directs the sequencer to generate nine dot wide character clocks. A logic 1 generates eight dot wide character clocks from the sequencer. Nine dots are selected for alphanumeric modes only. For nine dot modes, the ninth dot equals the eighth dot for ASCII codes C0 through DF hex. Also, see the Line Graphics bit in Mode Control Register in the Attribute section.

Map Mask Register

Port = 03C5 **Index = 02**

Bit	Description
7-4	Reserved
3	Map 3 Enable
2	Map 2 Enable
1	Map 1 Enable
0	Map 0 Enable

Bits 7-4 Reserved

Bits 3-0 A logic 1 enables the CPU to write to the corresponding memory map. These bits are used to write protect any memory map. When all four bits are logic 1, a 32-bit write operation can be performed by the CPU with only one memory cycle. This is useful for intensive screen updates in graphics modes. For odd/even modes, maps 0 and 1, and maps 2 and 3 should have the same map mask value. When chain 4 mode is selected, all maps should be enabled. This is a read-modify-write operation for CPU write.

Table 8. Map Select (1)

Bit 5	Bit 3	Bit 2	Map	Table Location
0	0	0	0	1st 8K of Map 2
0	0	1	1	3rd 8K of Map 2
0	1	0	2	5th 8K of Map 2
0	1	1	3	7th 8K of Map 2
1	0	0	4	2nd 8K of Map 2
1	0	1	5	4th 8K of Map 2
1	1	0	6	5th 8K of Map 2
1	1	1	7	8th 8K of Map 2

Table 9. Map Select (2)

Bit 4	Bit 1	Bit 0	Map	Table Location
0	0	0	0	1st 8K of Map 2
0	0	1	1	3rd 8K of Map 2
0	1	0	2	5th 8K of Map 2
0	1	1	3	7th 8K of Map 2
1	0	0	4	2nd 8K of Map 2
1	0	1	5	4th 8K of Map 2
1	1	0	6	6th 8K of Map 2
1	1	1	7	8th 8K of Map 2

Character Map Select Register

Port = 03C5 **Index = 03**

Bit	Description
7, 6	Reserved
5	Character Map Select High Bit A
4	Character Map Select High Bit B
3, 2	Character Map Select A

1,0 Character Map Select B

Bits 7,6 Reserved

Bits 5,3,2 Selects font table from map 2 according to Table 8 when attribute bit 3 is a 1.

Bits 4,1,0 Selects font table from map 2 according to Table 9 when attribute bit 3 is a 0.

Note: Bit 3 of the attribute byte normally controls the ON/OFF of the foreground intensity in text modes. This bit however, may be redefined as a switch between character sets. For this feature to be enabled, the following statement must be true:

- The setting value of Character Map Select A does not equal the value of Character Map Select B.

Memory Mode Register

Port = 03C5 **Index = 04**

Bit	Description
7-4	Reserved
3	Chain 4
2	Odd/Even
1	Extended Memory
0	Reserved

Bits 7-4 Reserved

Bit 3 A logic 0 enables the CPU to access data sequentially within a bit map by use of the Map Mask Register. A logic 1 causes two low-order address bits (A0, A1) to select the map that will be accessed in Table 10.

For read operation from the CPU, these two bits are also used to select the read maps in the graphics section.

Bit 2 A logic 0 directs even CPU addresses to access maps 0 and 2, while odd CPU addresses access maps 1 and 3, A logic 1 causes access to data within a bit map sequentially.

Bit 1 A logic 1 shows that greater than 64K bytes of video memory is being used. This is set to permit the VGA to use the 256K bytes of video memory. This also enables the character map selection. (See Character Map Select Register.)

Bit 0 Reserved

Table 10. Map Select (3)

A1	A0	Map Selected
0	0	Map 0
0	1	Map 1
1	0	Map 2
1	1	Map 3

CRT Controller Registers

This section describes all the registers in the CRT Controller. See Table 11.

Table 11. CRT Controller Registers

Register Name	Port	Index
CRT Controller Address Register	03?4	–
Horizontal Total	03?5	00
Horizontal Display Enable End	03?5	01
Start Horizontal Blanking	03?5	02
End Horizontal Blanking	03?5	03
Start Horizontal Retrace	03?5	04
End Horizontal Retrace	03?5	05
Vertical Total	03?5	06
Overflow	03?5	07
Preset Row Scan	03?5	08
Maximum Scan Line	03?5	09
Cursor Start	03?5	0A
Cursor End	03?5	0B
Start Address High	03?5	0C
Start Address Low	03?5	0D
Cursor Location High	03?5	0E
Cursor Location Low	03?5	0F
Start Vertical Retrace	03?5	10
End Vertical Retrace	03?5	11
Vertical Display Enable End	03?5	12
Offset	03?5	13
Underline Location	03?5	14
Start Vertical Blank	03?5	15
End Vertical Blank	03?5	16
CRTC Mode Control	03?5	17
Line Compare	03?5	18

? = B of D in accordance with Bit 0 of Miscellaneous Output register.

CRT Controller Address Register

Port = 3?4

Bit	Description
7-6	Reserved
5	Test Bit, must = 0
4-0	CRTC Address

Bits 7, 6 Reserved

Bit 5 Test bit, must remain 0.

Bit 4-0 Binary value programmed in these bits selects one of the CRT Controller registers where data is to be accessed.

Note: All CRT Controller Registers are Read/Write registers.

Horizontal Total Register

Port = 03?5 **Index = 0**

Bit	Description
7-0	Horizontal Total (-5)

In the CRT Controller, there is a horizontal character counter which counts character clock inputs generating from the Sequencer and compares against the value of the horizontal registers to provide horizontal timings. The horizontal total defines the total number of characters in the horizontal scan interval including the retrace time.

Bits 7-0 The total number of characters minus 5.

Horizontal Display Enable End Register

Port = 03?5 **Index = 01**

Bit	Description
7-0	Horizontal Display Enable End (-1)

This register defines the length of the horizontal display enable signal. It determines the number of displayed character positions per horizontal line.

Bits 7-0 Total number of displayed characters minus 1.

Start Horizontal Blanking Register

Port = 03?5 **Index = 02**

Bit	Description
7-0	Start Horizontal Blanking

Bit 7-0 These 8-bit values determine when to start the internal horizontal blanking output signal. When the internal character counter reaches this value, the horizontal blanking signal becomes active.

End Horizontal Blanking Register

Port = 03?5 **Index = 03**

Bit Description

7 Test Bit

6-5 Display Enable Skew Control

4-0 End Blanking

Bit 7 Test Bit

Bits 6, 5 Bits 6 and 5 indicate the magnitude of display enable skew. Display enable skew control is necessary to give adequate time for the CRT Controller to interrogate the display buffer in order to obtain a character and attribute code. It must also access the character generator font, and subsequently access the Horizontal PEL Panning register in the Attribute Controller. The display enable signal must be skewed one character clock unit for every access. This allows the video output to be in synchronization with the horizontal and vertical retrace signals. See Table 12.

Bits 4-0 A binary value programmed in these bits is compared to the six least-significant bits of the horizontal character counter to determine the status of the horizontal blanking signal. The comparison is equal at the time the horizontal blanking signal becomes inactive. Use the following algorithm to calculate the width W of blanking signal:

Value of Start Blanking register + width of blanking signal in character clock units = 6-bit result to be programmed into these bits. Bit number 5 is located in the End Horizontal Retrace register.

Table 12. Skew

Bit 6	Bit 5	Amount of Skew
0	0	Zero
0	1	One
1	0	Two
1	1	Three

Start Horizontal Retrace Register

Port = 03?5 **Index = 04**

Bit	Description
7-0	Start Horizontal Retrace

Bits 7-0 This register is used to center the screen horizontally and to specify the character position at which the Horizontal Retrace Pulse becomes active. The value programmed is a binary count of the character position number at which the signal becomes active.

End Horizontal Retrace Register

Port = 03?5 **Index = 05**

Bit	Description
7	End Horizontal Blanking, bit 5
6, 5	Horizontal Retrace Delay
4-0	End Horizontal Retrace

This register specifies the character position at which the Horizontal Retrace Pulse becomes inactive.

Bit 7 This is bit number 5 of End Horizontal Blanking. The first four bits are located in the End Horizontal Blanking register (index hex 03).

Bits 6, 5 These bits control the skew of the Horizontal Retrace signal. See Table 12.

Bits 4-0 A value programmed here is compared to the five least-significant bits of the horizontal character counter. When they are equal, the horizontal retrace signal becomes inactive. Use the following algorithm to calculate the width W of the retrace signal:

Value of Start Horizontal Retrace Register + Width of Horizontal Retrace signal in character clock units = 5-bit result to be programmed into the End Horizontal Retrace Register.

Vertical Total Register

Port = 03?5 **Index = 06**

Bit	Description
7-0	Vertical Total (–2)

The 8-bit binary value gives the number of horizontal scan lines on the CRT screen, minus 2, including vertical retrace. This is the low-order 8-bits of a 10-bit register. Bit 8 or this register is located in the CRT Controller Overflow register (hex 07, bit 0). Bit 9 of this register is located in the CRT Controller Overflow register (hex 07, bit 5).

Bits 7-0 Total number of horizontal scan lines, minus 2.

Overflow Register

Port = 03?5 **Index = 07**

Bit	Description
7	Start Vertical Retrace Bit 9
6	Vertical display Enable End Bit 9
5	Vertical Total Bit 9
4	Line Compare Bit 8
3	Start Vertical Blank Bit 8
2	Start Vertical Retrace Bit 8
1	Vertical display Enable End Bit 8
0	Vertical Total Bit 8

Bit 7 Bit 9 of the Start Vertical Retrace register.

Bit 6 Bit 9 of the Vertical display Enable End Register.

Bit 5 Bit 9 of the Vertical Total Register.

Bit 4 Bit 8 of the Line Compare Register.

Bit 3 Bit 8 of the Start Vertical Blank Register.

Bit 2 Bit 8 of the Start Vertical Retrace Register.

Bit 1 Bit 8 of the Vertical Display Enable End Register.

Bit 0 Bit 8 of the Vertical Total Register.

Preset Row Scan Register

Port = 03?5 **Index = 08**

Bit	Description
7	Reserved
6, 5	Byte Panning Control
4-0	Starting Row Scan Count after a Vertical Retrace

Bit 7 Reserved

Bits 6, 5 Bits 6 and 5 control byte panning when programmed as multiple shift modes. (This is currently not used.) The PEL Panning register in the attribute section allows panning of up to eight single PELs. When in single byte shift modes the CRT Controller start address is increased by one, while attribute panning is reset to 0. This is done to pan the next higher PEL. When used for multiple shift modes, the byte pan bits are extensions to the attribute PEL Panning register. In this manner, panning across the width of the video output shift is achieved. In the 32-bit shift mode, the byte pan and PEL panning bits provide up to 31 bits of panning capability. To pan from position 31 to 32, the CRT Controller start address is incremented and PEL and byte panning is reset to 0. These bits should normally be set to 0.

Bits 4-0 A binary value to specify the starting row scan count after a vertical retrace. The row scan counter increments each horizontal retrace time until a maximum row scan occurs.

Table 13. Clock Skew

Bit 6	Bit 5	Function
0	0	Zero-character clock skew
0	1	One-character clock skew
1	0	Two-character clock skew
1	1	Three-character clock skew

At maximum row scan compare time, the row scan is cleared (not preset).

Maximum Scan Line Register

Port = 03?5 **Index = 09**

Bit	Description
7	200 → 400 Line Conversion
6	Line Compare Bit 9
5	Start Vertical Blank Bit 9
4-0	Maximum Scan Line

Bit 7 A logic 1 causes the clock to the row scan counter to be divided by 2 and enables 200 to 400 line conversion. This allows the older 200-line modes to be displayed as 400 lines on the display (i. e. each line is displayed twice). When this bit is a 0, the clock to the row scan counter is equal to the horizontal scan rate.

Bit 6 Bit 9 of the Line Compare Register.

Bit 5 Bit 9 of the Start Vertical Blank Register.

Bit 4-0 These bits specify the number of lines per character row. The number to be programmed is the maximum row scan number minus 1.

Cursor Start Register

Port = 03?5 **Index = 0A**

Bit	Description
7, 6	Reserved
5	Cursor Off
4-0	Cursor Starts

Bits 7, 6 Reserved

Bit 5 A logic 1 turns off the cursor, a logic 0 turns on the cursor.

Bits 4-0 The value of these five bits tells the row scan line of a character where cursor is to begin.

Note that when Cursor Start is programmed with a value greater than the Cursor End, no cursor is generated.

Cursor End Register

Port = 03?5 **Index = 0B**

Bit	Description
7	Reserved
6, 5	Cursor Skew Control
4-0	Cursor Ends

Bit 7 Reserved

Bits 6, 5 These bits control the skew of the cursor signal. Cursor skew delays the cursor by the selected number of clocks. Each additional skew moves the cursor right one position on the screen. See Table 13.

Bits 4-0 These bits specify the row scan line of a character where the cursor is to end.

Start Address High Register

Port = 03?5 **Index = 0C**

Bit	Description
7-0	High Order 8-bit Start Address

Bits 7-0 These are the high order 8 bits of the start address. The 16-bit value, from the high-order and low-order Start Address Registers, is the first address after the vertical retrace on each screen refresh.

Start Address Low Register

Port = 03?5 **Index = 0D**

Bit	Description
7-0	Low Order Start Address

Bits 7-0 These are the low-order 8 bits of the start address.

Cursor Location High Register

Port = 03?5 **Index = 0E**

Bit	Description
7-0	High Order Cursor Location

Bits 7-0 These are the high-order 8 bits of the cursor location.

Cursor Location Low Register

Port = 03?5 **Index = 0F**

Bit	Description
7-0	Low Order Cursor Location

Bits 7-0 These are the low-order 8 bits of the cursor location.

Start Vertical Retrace Register

Port = 03?5 **Index = 10**

Bit	Description
7-0	Low Order 8-bit Vertical Retrace Pulse

Bits 7-0 These are the low-order 8 bits of the vertical retrace pulse start position in horizontal scan lines. Bits 8 and 9 are in the CRTC Overflow register.

End Vertical Retrace Register

Port = 03?5 **Index 11**

Bit	Description
7	Protect R0-R7
6	Select 5 Refresh Cycles
5	0 = Enable Vertical Interrupt

4	0 = Clear Vertical Interrupt
3-0	End Vertical Retrace

Bit 7 A logic 0 enables writing to CRTC registers 0-7. A logic 1 disables writing these registers. Note that the line comparing bit 4 in register 07 is not protected.

Bit 6 A logic 0 selects three refresh DRAM cycles. A logic 1 selects five refresh cycles per horizontal line. Five refresh cycles are used for slow (15.75 KHz) sweep rate displays.

Bit 5 A logic 0 enables a vertical retrace interrupt. This occurs on IRQ2. Since this may be a "shared" interrupt level, the Input Status register 0, bit 7, must be checked to determine if the VGA caused the interrupt to occur.

Bit 4 A logic 0 clears a vertical retrace interrupt. An interrupt handler has to reset an internal flip-flop by writing a 0 to this bit, then setting the bit to 1 so that the flip-flop does not hold interrupts inactive. Note that you do not change the other bits in this register when changing this bit. Read this register first before resetting this flip-flop so that the value of the other bits can be determined and saved for later use.

Bits 3-0 These bits determine the horizontal scan count value when the vertical retrace output signal becomes inactive. Use the following algorithm to calculate the width of vertical retrace signal:

Value of Start Vertical Retrace register + width of vertical retrace signal in horizontal scan line units = 4-bit result to be programmed into the End Vertical Retrace register.

Vertical Display Enable End Register

Port = 03?5 **Index = 12**

Bit	Description
7-0	Low Order Vertical Display Enable End (−1)

Bits 7-0 These are the low-order 8 bits of a 10-bit register that determines the vertical display enable end position. Bits 8 and 9 of this register are contained in the CRT Controller Overflow register bits 1 and 6 respectively.

Offset Register

Port = 03?5 **Index = 13**

Bit	Description
7-0	Logic Line Width of the Screen

Bits 7-0 This register defines the logic line width of the screen. Starting memory address for the next character row is larger than the current character row by a factor of 2X or 4X this value. A word address programs the Offset Register. This word address may be a word or double word address, determined by the means of clocking the CRT Controller.

Underline Location Register

Port = 03?5 **Index = 14**

Bit	Description
7	Reserved
6	Doubleword Mode
5	Count by 4
4-0	Horizontal row scan where underline will occur

Bit 7 Reserved

Bit 6 A logic 1 enables double-word mode for memory addresses. Also, see the description of the CRT Controller Mode Control register bit 6.

Bit 5 When this bit is set to 1, the memory address counter is clocked with the character clock divided by 4. This bit is used when double-word addresses are used.

Bits 4-0 This register determines the horizontal row scan of a character row where an underline occurs. The scan line number desired is a value one greater than the number programmed.

Start Vertical Blanking Register

Port = 03?5 **Index = 15**

Bit	Description
7-0	Start Vertical Blanking (−1)

Bits 7-0 These are the low-order 8 bits of a 10-bit register. The value of this register determines when the vertical blanking signal becomes active. Bit 8 is located in the CRT Controller Overflow register bit 3. Bit 9 is contained in the CRT Controller Maximum Scan Line register bit 5. The horizontal scan line count (at which the vertical blanking signal becomes active) is one greater than the value of these 10 bits.

End Vertical Blanking Register

Port = 03?5 **Index = 16**

Bit	Description
7-0	End Vertical Blanking

Bits 7-0 This register defines the horizontal scan count value at the time the vertical blank output signal goes inactive. The register must be

programmed in whole units of horizontal scan lines. Use the following algorithm to obtain the width of the vertical blank signal.

(Value of Start Vertical Blank register–1) + width of vertical blank signal in horizontal scan unit = 8-bit result to be programmed into the End Vertical Blank register.

CRTC Mode Control Register

Port = 03?5 **Index = 17**

Bit	Description
7	Hardware Reset
6	Word/Byte Mode
5	Address Wrap
4	Reserved
3	Count by Two
2	Horizontal Retrace Select
1	Select Row Scan Counter
0	CMSO

Bit 7 A logic 0 clears horizontal and vertical retrace. A logic 1 enables horizontal and vertical retrace. This bit does not reset any other registers or outputs.

Bit 6 A logic 0 selects the word address mode which shifts all memory address counter bits down one bit, and the most significant bit of the counter appears on the least significant bit of the memory address output. A logic 1 selects the byte address mode. Note that bit 6 of the Underline Location register also controls the addressing. When it is a 0, bit 6 of this register has control. When it is a 1, the addressing is forced to be shifted by two bits.

Bit 5 This bit selects the memory address counter bit MA13 or bit MA15, and it appears on the MA0 of CRT address output in the word address mode. A logic 1 selects MA15. MA13 is selected for the case where only 64K memory is installed. Since 256K memory is always installed for UM587, MA15 should be selected in odd/even mode.

Bit 4 Reserved

Bit 3 A logic 0 causes the memory address counter clocked with the normal character clock input. A logic 1 clocks the memory address counter with the character clock input divided by 2. This bit is used to create either a byte or word refresh address for the display buffer.

Bit 2 A logic 0 selects normal horizontal retrace. A logic 1 selects horizontal retrace divided by 2 as the clock that controls the vertical timing counter. This bit can be used to effectively double the vertical resolution capability of the CRT Controller. The 10-bit vertical counter has a maximum of 1024 scan lines. If the vertical counter is clocked with the horizontal retrace divided by 2, then the vertical resolution is doubled to 2048 horizontal scan lines.

Bit 1 A logic 0 selects row scan counter bit 1 for CRT memory address bit MA14. A logic 1 selects MA14 counter bit for CRT memory address bit MA14.

Bit 0 When this bit is a logic 0, row scan address bit 0 is substituted for memory address bit 13 during active display time. A logic 1 enables memory address bit 13 to appear on the memory address output bit 13 of the CRT Controller.

Table 14. Register Modes

Memory Address	Byte Mode	Word Mode	Double-word Mode
MA0/RFA0	MA0	MA15/MA13	MA12
MA1/RFA1	MA1	MA0	MA13
MA2/RFA2	MA2	MA1	MA0
MA3/RFA3	MA3	MA2	MA1
MA4/RFA4	MA4	MA3	MA2
MA5/RFA5	MA5	MA4	MA3
MA6/RFA6	MA6	MA5	MA4
MA7/RFA7	MA7	MA6	MA5
MA8/RFA8	MA8	MA7	MA6
MA9	MA9	MA8	MA7
MA10	MA10	MA9	MA8
MA11	MA11	MA10	MA9
MA12	MA12	MA11	MA10
MA13	MA13	MA12	MA11
MA14	MA14	MA13	MA12
MA15	MA15	MA14	MA13

Line Compare Register

Port = 03?5 **Index = 18**

Bit	Description
7-0	Line Compare Target

Bits 7-0 This register is the lower byte of the line compare target. When the vertical counter achieves this value, the internal start of the line counter is reset. This causes an area of the screen to not be affected by scrolling. Bit 9 is in the Maximum Scan Line register. Bit 8 of this register is in the Overflow Register.

Graphics Controller Registers

This section describes all the registers located in the Graphics Controller. See Table 15.

Table 15. Graphics Controller Registers

Register Name	Port	Index
Graphics Address	03CE	–
Set/Reset	03CF	00
Enable Set/Reset	03CF	01
Color Compare	03CF	02
Data Rotate	03CF	03
Read Map Select	03CF	04
Graphics Mode	03CF	05
Miscellaneous	03CF	06
Color Don't Care	03CF	07
Bit Mask	03CF	08

Graphics Address Register

Port = 03CE

Bit	Description
7-4	Reserved
3-0	Graphics Address

Bits 7-4 Reserved

Bits 3-0 A binary value in these bits points to the other registers in the Graphics Controller section.

Set/Reset Register

Port = 03CF **Index = 00**

Bit	Description
7-4	Reserved
3	Set/Reset Map 3
2	Set/Reset Map 2
1	Set/Reset Map 1
0	Set/Reset Map 0

Bits 7-4 Reserved

Bits 3-0 During CPU memory write with write mode 0, the value of these bits will be written to all eight bits of the respective memory map if Set/Reset mode is enabled for the corresponding map.

Enable Set/Reset Register

Port = 03CF **Index = 01**

Bit	Description
7-4	Reserved
3	Enable Set/Reset Map 3
2	Enable Set/Reset Map 2
1	Enable Set/Reset Map 1
0	Enable Set/Reset Map 0

Bits 7-4 Reserved

Bits 3-0 A logic 1 enables the Set/Reset function. When enabled, the respective memory map is written with the value of the Set/Reset register, if write mode 0 is selected. However, when write mode is 0 and Set/Reset is not enabled on a map, that map is written with the value of the system microprocessor data.

Color Compare Register

Port = 03CF **Index = 02**

Bit	Description
7-4	Reserved
3	Color Compare Map 3
2	Color Compare Map 2
1	Color Compare Map 1
0	Color Compare Map 0

Bits 7-4 Reserved

Bits 3-0 These bits represent a 4-bit color value to be compared if the system microprocessor sets read mode 1 and does a memory read, the data returned from the memory cycle will be a 1 in each bit position where the four maps equal the color compare register.

The color compare bit is the value that all bits of the corresponding map's byte are compared with. Each of the eight bit positions of the selected byte are then compared across the four maps and a 1 is returned in each bit position where the bits of all four maps equal their respective color compare values.

Data Rotate Register

Port = 03CF **Index = 03**

Bit	Description
7-5	Reserved
4	Function Select
3	Function Select
2	Rotate Count 2
1	Rotate Count 1
0	Rotate Count 0

Bits 7-5 Reserved

Bits 4, 3 Data in the system microprocessor latches can operate logically with data written to memory. If rotate function is selected, it is applied before the logic function. See Table 17.

Bits 2-0 These bits specify the number of positions to right-rotate the system microprocessor data bus during system microprocessor memory writes. This operation is done when the write mode is 0. To write nonrotated data, the bits should be set to 0. See Table 17.

Table 16. Data Functions

Bit 4	Bit 3	Function
0	0	Data unmodified
0	1	Data ANDed with latched data
1	0	Data ORed with latched data
1	1	Data XORed with latched data

Table 17. Rotate Functions

Bit 2	Bit 1	Bit 0	Function
0	0	0	No Rotate
0	0	1	Rotate 1 Position
0	1	0	Rotate 2 Positions
0	1	1	Rotate 3 Positions
1	0	0	Rotate 4 Positions
1	0	1	Rotate 5 Positions
1	1	0	Rotate 6 Positions
1	1	1	Rotate 7 Positions

Read Map Select Register

Port = 03CF **Index = 04**

Bit Description
7-2 Reserved
1 Map Select 1
0 Map Select 0

Bits 7-2 Reserved

Bits 1, 0 These bits select the memory map number from which the system microprocessor reads data. This register has no effect on the color compare read mode. In odd/even modes the value may be 00 or 01 (10 or 11) for chained maps 0, 1 (2, 3). See Table 18.

Table 18. Map Data

MS1	MS0	Function
0	0	Read data from Map 0
0	1	Read data from Map 1
1	0	Read data from Map 2
1	1	Read data from Map 3

Graphics Mode Register

Port = 03CF **Index = 05**

Bit Description
7 Reserved
6 256 Color Mode
5 Shift Register Mode
4 Odd/Even
3 Read Type
2 Reserved
1, 0 Write Mode

Bit 7 Reserved

Bit 6 A logic 0 permits bit 5 to handle the loading of the Shift Registers. A logic 1 supports the 256 color mode (only for 320x200 320x 400 resolution).

Bit 5 A logic 1 instructs the Shift Registers in the graphic section to format the serial data with odd-numbered bits from both maps on the odd-numbered maps and even-numbered bits from both maps on the even-numbered maps. This bit is also used in modes 4 and 5.

Bit 4 A logic 1 enables the odd/even addressing mode, which can emulate the IBM CGA compatible mode. The value programmed is the value of the Memory Mode register bit 2 of the Sequencer.

Bit 3 A logic 0 causes the system microprocessor to read data from the memory map selected by the Read Map Select register unless chain 4, link 4, or link 8 is set to 1. In this case the Read Map Select register has no effect. When this bit is a logic 1, the system microprocessor reads the results of the comparison of the four memory maps and the Color Compare register.

Bit 2 Reserved

Bits 1, 0 Write Mode (See Table 19.)

Miscellaneous Register

Port = 03CF **Index = 06**

Table 19. Function Decode

Bit-1	Bit-0	Function
0	0	The system microprocessor data is rotated by the number or counts in the Rotate Register that each memory map is written with, unless Set/Reset is enabled for the map. When the map Set/Reset is enabled, they are written with 8-bits of the value in the Set/Reset Register for that map.
0	1	The contents of the system microprocessor latches are written to each memory map. A system read operation loads these latches.
1	0	8-bits of the value of data bit n fills memory map n (0-3).
1	1	The maps are written by the 8-bits contained in the Set/Reset Register for that specific map (Enable Set/Reset Register is a "don't care"). Rotated system microprocessor data is logically ANDed with Bit Mask Register data and forms an 8-bit value. This is the function that the Bit Mask Register performs in write modes 0 and 2. (See Bit Mask Register.)

Note that the logic function specified by the Function Select register is applied to data being written to memory following modes 0, 2, and 3 described above.

Bit	Description
7-4	Reserved
3	Memory Map 1
2	Memory Map 0
1	Odd/Even
0	Graphics Mode

Bits 7-4 Reserved

Bits 3, 2 These bits control the mapping between regenerative buffer and the CPU address space. The bit functions are defined in Table 20.

Bit 1 When set to a logic 1, this bit instructs the system microprocessor address bit 0 to be replaced by a higher-order bit. The odd/even maps will be selected with odd/even values of the system microprocessor A0 bit, respectively.

Bit 0 This is the text mode addressing control. A logic 1 enables the graphics mode. The character generator address latches are disabled, when set to graphics mode.

Table 20. Byte Select

Bit 3	Bit 2	Function
0	0	Hex A0000 for 128K bytes
0	1	Hex A0000 for 64K bytes
1	0	Hex B0000 for 32K bytes
1	1	Hex B8000 for 32K bytes

Color Don't Care Register

Port = 03CF **Index = 07**

Bit	Description
7-4	Reserved
3	Map 3 = Don't Care
2	Map 2 = Don't Care
1	Map 1 = Don't Care
0	Map 0 = Don't Care

Bits 7-4 Reserved

Bit 3 1 - Do the color compare for map 3.
0 - Don't Care for map 3.

Bit 2 1 - Do the color compare for map 2.
0 - Don't Care for map 2.

Bit 1 1 - Do the color compare for map 1.
0 - Don't Care for map 1.

Bit 0 1 - Do the color compare for map 0.
0 - Don't care for map 0.

Bit Mask Register

Port = 03CF **Index = 08**

Bit Description

7-0 Bit Mask for 8-bits of data

Bits 7-0 Bits programmed to a 1 allow writes to the corresponding bits in the maps. A logic 0 permits the corresponding bit n in each map to be locked at its current state, providing the location being written was the final location read by the system's microprocessor.

Note that the bit mask applies to write modes 0 and 2. To preserve bits using the bit mask, data must be latched internally by reading the location. When data is written to preserve the bits, the most current data in the latches is written in those positions. The bit mask applies to all maps simultaneously.

Attribute Controller Registers

This section describes all the registers located in Attribute Controller section. See Table 21.

Table 21. Attribute Controller Registers

Register Name	Port	Index
Address Register	03C0	–
Palette Registers	03C0	00-0F
Attribute Mode Control Register	03C0	10
Overscan Color Register	03C0	11
Color Plan Enable Register	03C0	12
Horizontal PEL Panning Register	03C0	13
Color Select Register	03C0	14

Attribute Address Register

Port = 03C0

Bit	Description
7, 6	Reserved
5	Palette Address Source
4-0	Attribute Address

Bits 7, 6 Reserved

Bit 5 Bit 5 must be cleared to 0 before loading the Color Palette registers. Normal operation of the Attribute Controller requires that bit 5 be set to 1. This allows the video memory data to access the palette registers.

Bits 4-0 A binary value in these bits points to the Attribute Data register where data is to be written.

The Address and Data registers can not be selected by the Attribute Controller register. An internal address flip-flop controls this selection. To initialize the flip-flop, an I/O Read instruction must be sent to the Attribute Controller at address 03BA or 03DA. This clears the flip-flop, and then selects the Address register. The Address register is then loaded with an I/O Write to 03C0. The following I/O Write instruction to 03C0 loads the Data register. The flip-flop changes state each time an I/O Write instruction is sent to the Attribute Controller. It does not change when an I/O Read to 03C1 occurs.

Palette Registers

Write-03C0 Read-03C1 Index-00-0F

Bit	Description
7, 6	Reserved
5	P5
4	P4
3	P3
2	P2
1	P1
0	P0

Bits 7, 6 Reserved

Bits 5-0 The attribute byte of text or graphic color value is indexed to these 16 Color Palette registers. The contents of the pointed Palette registers are then used as values sent off the chip to the video DAC, where they in turn serve as addresses into the DAC internal registers. A logic 1 selects the appropriate color.

The Palette registers should be modified only during the vertical retrace interval to avoid problems with the displayed image.

Attribute Mode Control

Port - 03C0(R), 03C1(W) **Index = 10**

Bit	Description
7	P5, P4 Select
6	PEL Width
5	PEL Panning Compatibility
4	Reserved
3	Select Background Intensity or Enable Blink
2	Enable Line Graphics Character Code
1	Mono Emulation
0	Graphics/Alphanumeric Mode

Bit 7 A logic 0 selects the output of the Palette register as P5, P4. A logic 1 selects bits 1, 0 of the Color Select register as P5, P4 which are digital video bits that go off the chip.

Bit 6 A logic 1 causes the video pipeline to be sampled so that eight bits are available to select a color in the 256 color mode (hex 13). This bit must be a logic 0 in all other modes.

Bit 5 A logic 0 makes line compare and has no effect on the output of the PEL Panning register. A logic 1 causes a line compare

in the CRTC to force the output of the PEL Panning register to 0. When VSYNC occurs, the output reverts to its programmed value. This bit allows part of the screen to be panned.

Bit 4 Reserved

Bit 3 This bit is set to 1 for blinking graphics modes. A logic 1 enables the blink function in alphanumeric modes. A logic 0 selects the background intensity of the input. Previously, this mode was on the MDA and CGA modes.

Bit 2 A logic 1 enables the special line graphics character codes for the Monochrome emulation mode. A logic 0 causes the ninth dot the same as the background. When this bit is enabled it forces the ninth dot of a line graphic character to be the same as the eighth dot of a line graphic character. Graphics character codes are hex C0 through hex DF. For character fonts that do not use the line graphics character codes in this range (hex C0 through hex DF) bit 2 should be a 0. If not, unwanted video information will be shown on the CRT screen.

Bit 1 A logic 1 sets monochrome emulation mode. A logic 0 sets color emulation mode.

Bit 0 A logic 0 selects text mode. A logic 1 selects graphics mode.

Overscan Color Register

Port = 03C0(R), 03C1(W) **Index = 11**

Bit	Description
7	P7
6	P6
5	P5
4	P4
3	P3
2	P2
1	P1
0	P0

Bits 7-0 A binary value in this register determines the border color displayed on the CRT screen. The border color is displayed right after the Display Enable signal goes low and before the start of blanking period. The border is not supported in the 40-column text modes or the 320-PEL graphics modes. except for mode hex 13.

Color Plane Enable

Port = 03C0(R), 03C1(W) **Index = 12**

Bit	Description
7, 6	Reserved
5, 4	Video Status MUX
3-0	Enable Color Plane

Bits 7, 6 Reserved

Bits 5, 4 Two of the eight color outputs will be selected, according to these two bits, to reflect the real time status on bits 4 and 5 of Input Status Register 1. See Table 22.

Bits 3-0 A logic 1 for each bit enables the respective display memory color plane. A logic 0 disables color plane.

Table 22. Color Plane And Status

Color Plane Register Bit 5	Color Plane Register Bit 4	Input Status Register 1 Bit 5	Input Status Register 1 Bit 4
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

Horizontal PEL Panning

Port = 3C0(W), 3C1(R) **Index = 13**

Bit	Description
7-4	Reserved
3-0	Horizontal PEL Panning

Bits 7-4 Reserved

Bits 3-0 These four bits select the number of pixels that will shift the video data to the left. PEL panning is available in both graphics and text modes. In modes 0+, 1+, 2+, 3+, 7 and 7+, the maximum shift is eight pixels. Mode 13 allows a maximum of three pixels. In the rest of the modes, the image can be shifted a maximum of seven pixels. The order for shifting the image is shown in Table 23.

Table 23. PEL Register

PEL Panning Register Value	Number of PELs Shifted to the Left: 0+, 1+, 2+ 3+, 7, 7+	Number of PELs Shifted to the Left: All Other Modes	Number of PELs Shifted to the Left: Mode 13
0	1	0	0
1	2	1	–
2	3	2	1
3	4	3	–
4	5	4	2
5	6	5	–
6	7	6	3
7	8	7	–
8	0	–	–

Color Select Register

Port = 03C0(W), 03C1(R) **Index = 14**

Bit	Description
7-4	Reserved
3	Select Color 7
2	Select Color 6
1	Select Color 5
0	Select Color 4

Bits 7-4 Reserved

Bits 3, 2 These bits are the two high-order bits of the 8-bit digital color value sent off-chip in all modes except the 256 color graphics. In the 256 color modes, the 8-bit attributes are stored in video memory. This becomes the 8-bit digital color value to be sent off-chip to the video DAC. These bits are also used to switch quickly among sets of colors in the video DAC.

Bits 1, 0 These two bits can be used to replace the P4 and P5 bits from the Attribute Palette registers to form the 8-bit digital color value sent off-chip. This is controlled by bit 7 of Attribute Mode Control register. By using this feature, sets of colors can be rapidly switched in the video DAC.

Extended Registers

A set of new registers have been added into the basic version of the VGA to perform new features. They are grouped under the assignment of I/O ports 3DE and 3DF for address and data access respectively. All, except the NMI Data Cache registers, have both read and write access. A summary of new registers is given in Table 24.

Table 24. Extended Registers

Port	Index	R/W	Bits	Register
3DE	–	R/W	5	Extension Address Register
3DF	D	R/W	6	Bandwidth Control
3DF	E	R/W	4	I/O Trap Control
3DF	F	R	8	NMI Data Cache (FIFO)
3DF	10	R	8	Read DIP Switch

3DE-Extension Address Register

Bit	Description
0-4	5-bit index pointer to the extension data registers.
5-7	Reserved

The contents of this register need to be programmed before the data register is accessed. The I/O port assigned is 3DE for both read and write access.

3DF-Bandwidth Control

Index D

Bit	Description
0-2	Reserved
3-4	Bandwidth Control (See Table 25.)
5	Clock select bit 2 (CSEL2).

Used with bits 2 and 3 of Miscellaneous Register. One of eight different clock inputs can be selected. (See Table 26.)

Table 25. Bandwidth

Bit 4	Bit 3	Bandwidth
0	0	1-4
1	0	1-7
0	1	1-9
1	1	Reserved

Table 26. Clock

CSEL2	CSEL1	CSEL0	Clock
0	0	0	25.175 MHz
0	0	1	28.322 MHz
0	1	0	External Input Clock
0	1	1	Reserved
1	0	0	14.318 MHz
1	0	1	16.257 MHz
1	1	0	Reserved
1	1	1	35.5 MHz

3DF-I/O Trap Control **Index E**

Bit	Description
0	When set to 1, the trap is activated and generates NMI for downward compatibility emulation. When set to 0, the NMI logic is turned off.
1-2	Backward Compatibility Mode (See Table 27.)
3-6	Reserved = 0
7	Graphics Latch read compatibility.

Table 27. Graphics Mode

Bit 2	Bit 1	Mode
0	0	VGA
0	1	EGA
1	0	CGA
1	1	MCGA (MDA & HERC)

3DF - NMI Data Cache **Index F**

Bit	Description
0-7	First read of this register gets the address of the trapped I/O. Second read gets the data of the trapped I/O. The size of the cache is two bytes wide and five rows deep. Each read causes the read pointer to autoincrement resets at the end of information. Note that only the first 8-bits of I/O address are saved into cache. That means the first digit "3" is ignored. The trapped software should take care of this after receiving the address from cache. Since bit 7 of the first read of this register is always 1 if there is an address saved at this position, the trapped software should check this bit to determine whether this is a last read or not. Note that this is a read only register.

3DF - Read DIP Switch **Index 10**

Bit	Description
7	Reserved
6	DIP Switch 6
5	DIP Switch 5
4	DIP Switch 4
3	DIP Switch 3
2	DIP Switch 2
1	DIP Switch 1
0	DIP Switch 0

These bits will be read in during BIOS initialization to determine the type of monitor currently attached.

AC Characteristics: $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$, GND = 0V

I/O Read/Write, DAC Read/Write, Switch Read (See Figures 1, 2, 8, 9 & 10.)

Symbol	Parameter	Min.	Max.	Unit	Conditions
tACS	Address Setup Time	60	–	ns	
tCCS	ASEL Setup Time	30	–	ns	
tCAH	Address Hold Time	0	–	ns	
tCCH	ASEL Hold Time	0	–	ns	
tCPW	Command Pulse Width (Note)	200	–	ns	
tDWD	Write Data Delay	–	80	ns	
tDWH	Write Data Hold Time	0	–	ns	
tCED	$\overline{EDBUF}$ and $\overline{EABUF}$ Delay	–	50	ns	
tRDD	Read Data Valid Delay	–	120	ns	
tRDH	Read Data Hold Time	10	–	ns	
tRDIRD	Read to DIR Delay	–	45	ns	
tDRDD	$\overline{DACR}$ Delay	–	50	ns	
tDWDD	$\overline{DACW}$ Delay	–	50	ns	
tRDACD	Read to DAC Read Delay	–	40	ns	
tWDACD	Write to DAC Write Delay	–	40	ns	
tRSWTR	Read to Switch Read Delay	–	40	ns	

Memory Read/Write (See Figures 3 & 4.)

Symbol	Parameter	Min.	Max.	Unit	Conditions
tACS	Address Setup Time	60	–	ns	
tCCS	ASEL Setup Time	30	–	ns	
tCAH	Address Hold Time	0	–	ns	
tCCH	ASEL Hold Time	0	–	ns	
tDWD	Write Data Delay	–	80	ns	
tDWH	Write Data Hold Time	0	–	ns	
tCED	$\overline{EDBUF}$ and $\overline{EABUF}$ Delay	–	50	ns	
tRDIRD	Read to DIR Delay	–	45	ns	
tMRIOLD	Command to CPURDY Low Delay	–	40	ns	
tMRIOHD	RD Data to CPURDY High Delay	–	15	ns	
tVDH	Valid RD Data Hold Time	–	45	ns	

Clock and Video (See Figure 5.)

Symbol	Parameter	Min.	Max.	Unit	Conditions
tCLK	CLKIN/DOTCLK Cycle	28	–	ns	
tPEL	P0-P7 Delay	–	80	ns	
tBNK	$\overline{BLANK}$ Delay	–	80	ns	
tSYNC	HSYNC/VSYNC Delay	–	80	ns	
tPCLK	CLKIN to PCLK Delay	–	60	ns	

DRAM Read/Write (See Figures 6 & 7.)

Symbol	Parameter	Min.	Max.	Unit	Conditions
tRS	Row Address Setup	10	–	ns	
tRH	Row Address Hold Time	0.5 tCLK	–	ns	
tRPW	$\overline{RAS}$ Low Time	4 tCLK - 10	–	ns	
tRPC	$\overline{RAS}$ High Time	3 tCLK	–	ns	
tCS	Column Address Setup Time	10	–	ns	
tCH	Column Address Hold Time	tCLK	–	ns	
tCPW	$\overline{CAS}$ Low Time	4.5 tCLK	–	ns	
tCPC	$\overline{CAS}$ High Time	2.5 tCLK - 10	–	ns	
tROED	$\overline{RAS}$ to $\overline{OE}$ Delay	2.5 tCLK - 10	–	ns	
tRWE	$\overline{RAS}$ to $\overline{WE}$ Delay	2.5 tCLK - 10	–	ns	
tWER	$\overline{WE}$ to $\overline{RAS}$ High	tCLK	–	ns	
tRC	$\overline{RAS}$ to $\overline{CAS}$ Reference	1.5 tCLK - 10	–	ns	
tDWS	Data to $\overline{WE}$ Setup Time	10	–	ns	
tDWH	Data to $\overline{WE}$ Hold Time	tCLK	–	ns	

Timing Waveforms

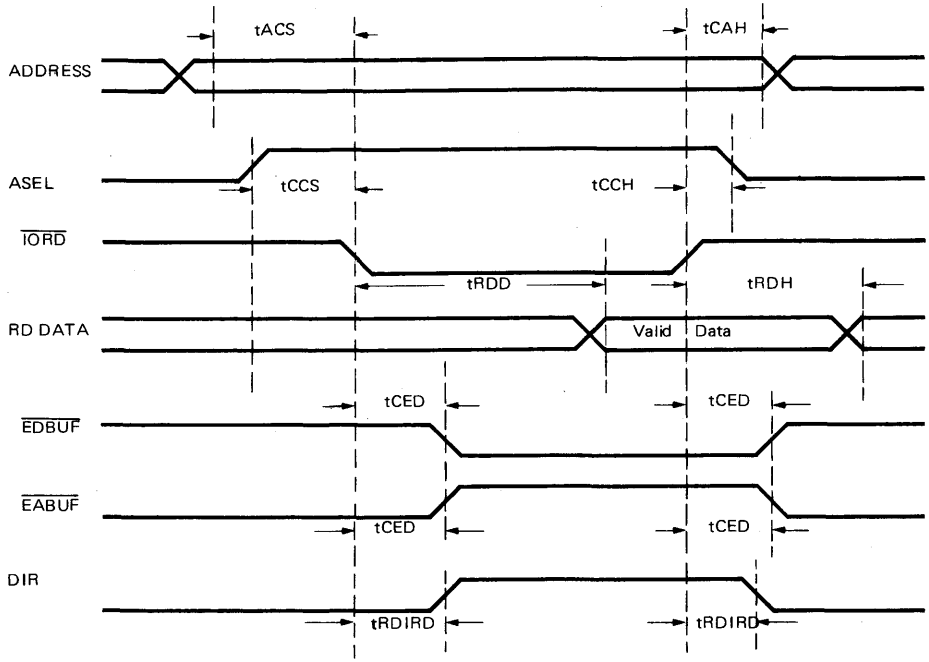


Figure 1. I/O READ TIMING

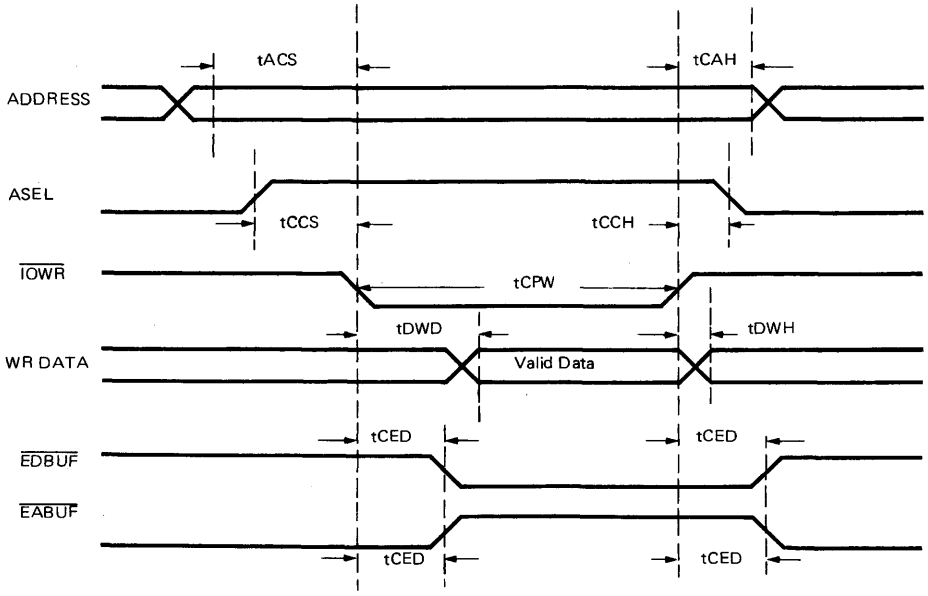


Figure 2. I/O WRITE TIMING

Timing Waveforms (Continued)

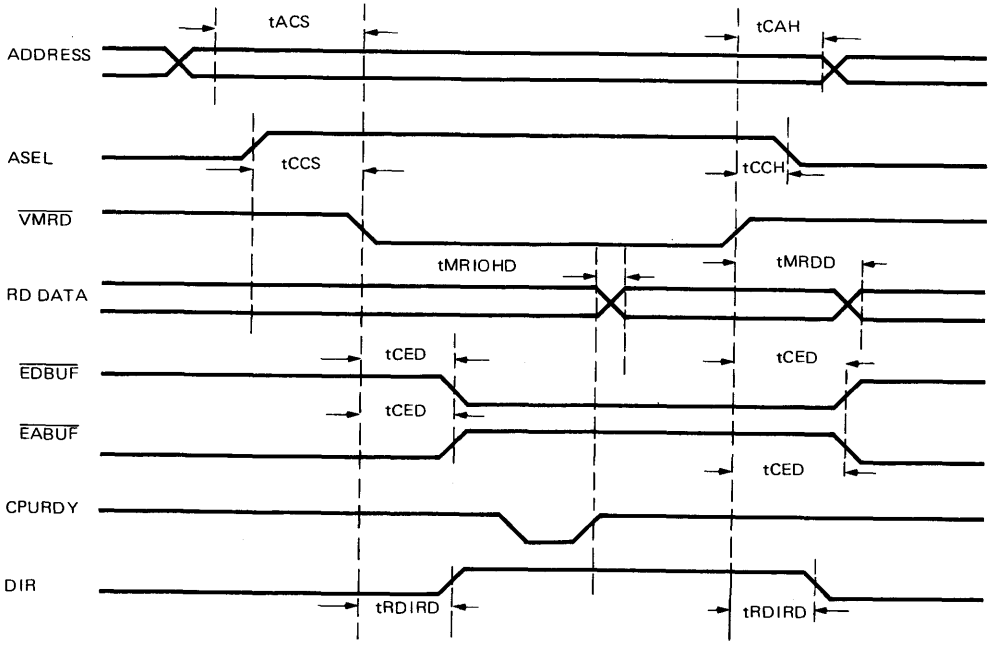


Figure 3. MEMORY READ TIMING

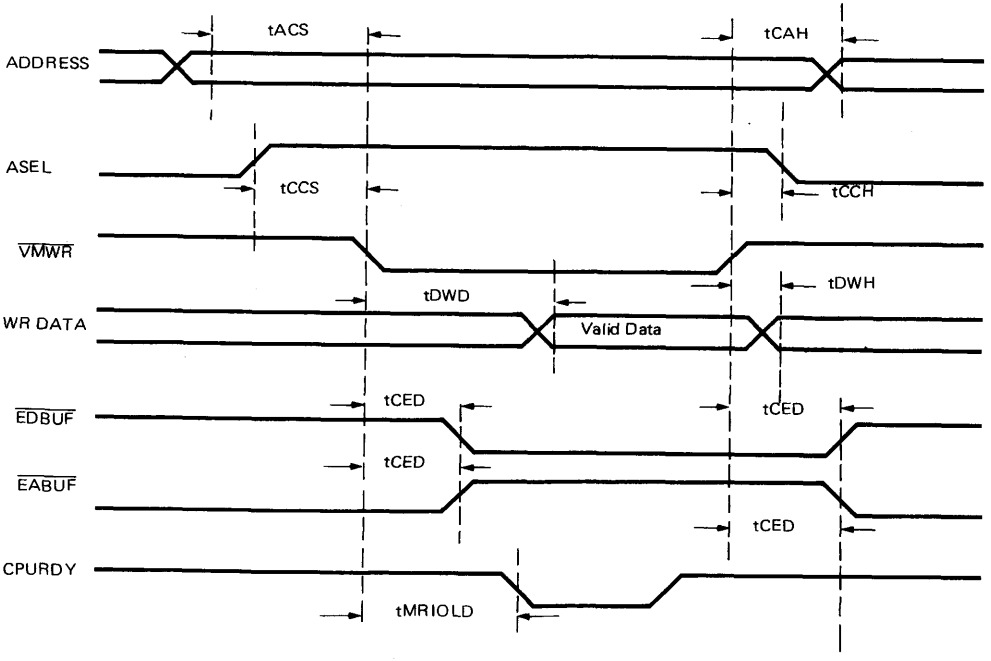


Figure 4. MEMORY WRITE TIMING

Timing Waveforms (Continued)

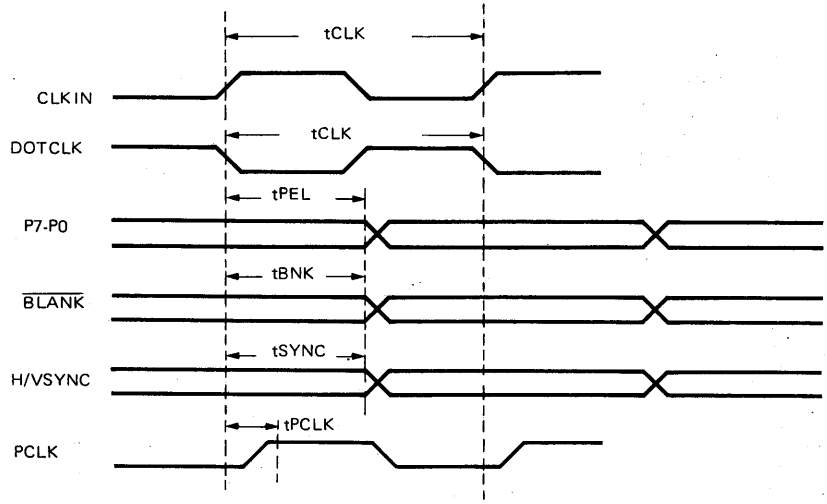


Figure 5. CLOCK AND VIDEO TIMING

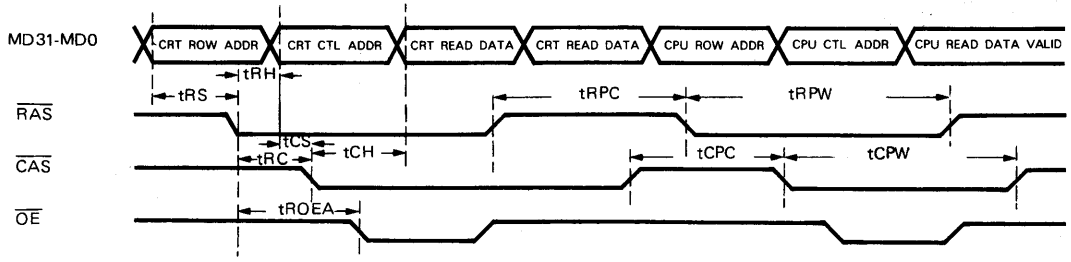


Figure 6. DRAM READ TIMING

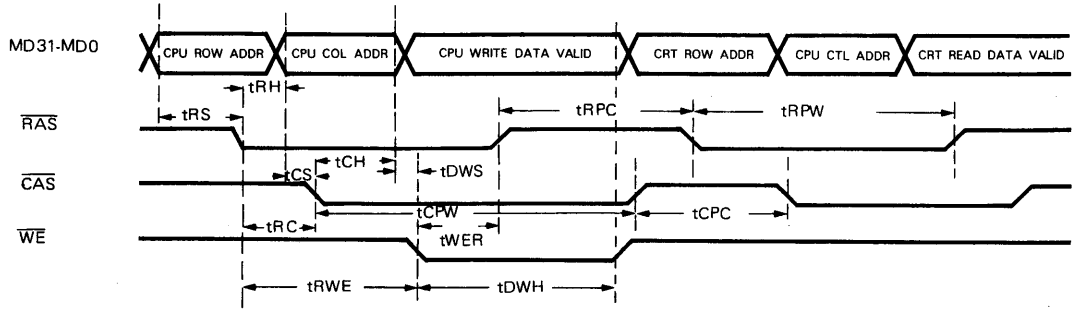


Figure 7. DRAM WRITE TIMING

Timing Waveforms (Continued)

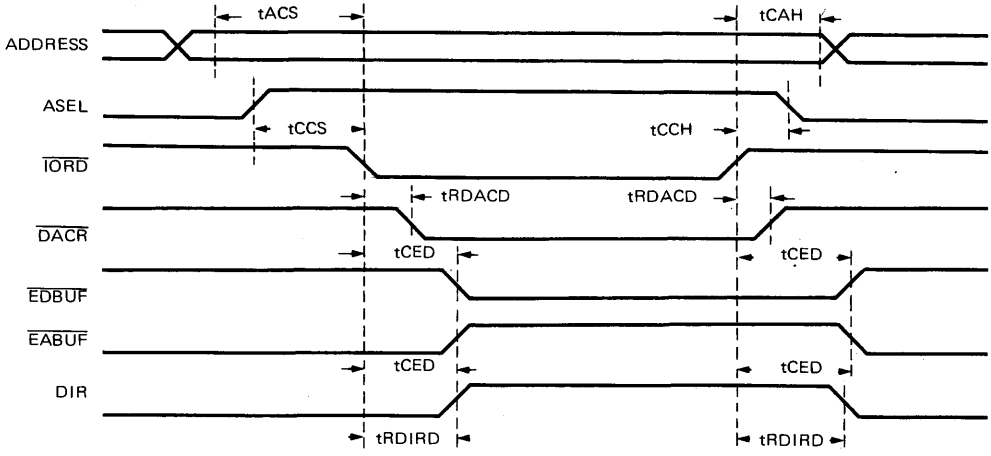


Figure 8. DAC Read Timing

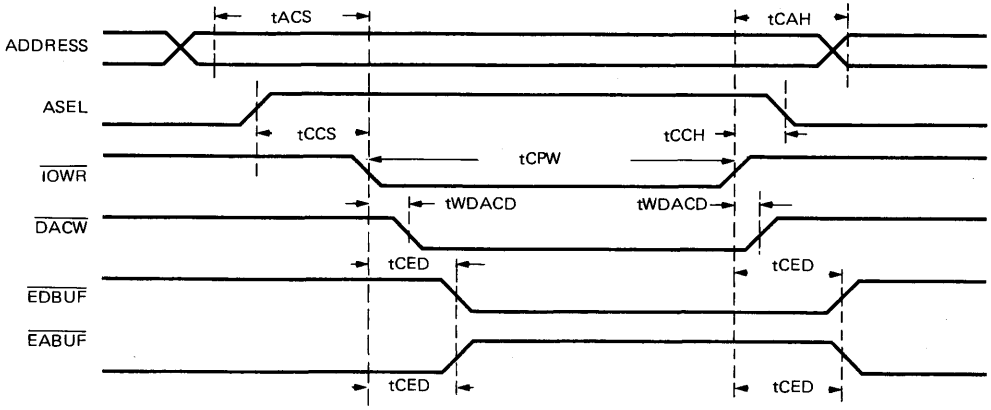


Figure 9. DAC Write Timing

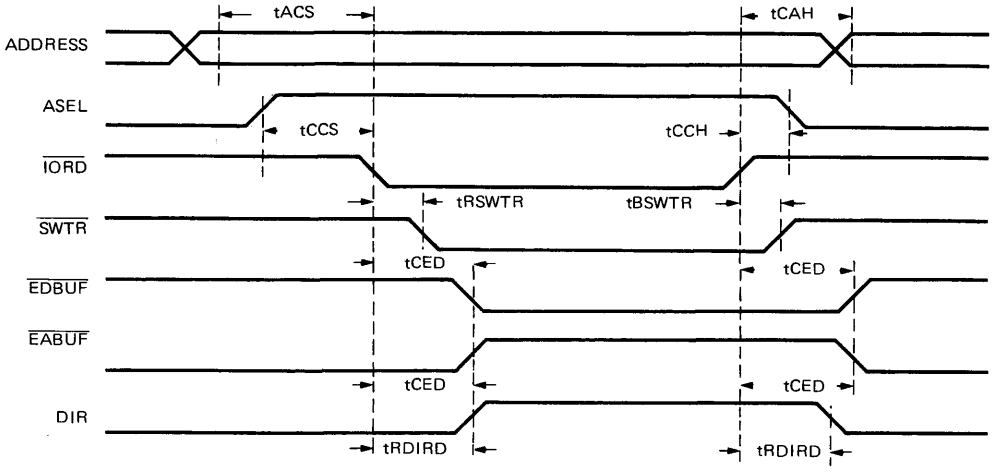


Figure 10. Switch Read Timing

Absolute Maximum Ratings *

Ambient Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +150°C
Supply Voltage to Ground Potential
. . . . . −0.5V to V_{CC} +7.0V
Applied Input Voltage . . . . . −0.5V to V_{CC} +7.0V

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics: T_A = 25°C, V_{CC} = 5V ± 5%, GND = 0V

Symbol	Parameter	Min.	Max.	Unit	Conditions
V_{OH}	Output High Voltage	2.4		V	I_{OH} = 400 μA
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 20 mA, Note 1
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 12 mA, Note 1
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 8 mA, Note 1
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 4 mA, Note 1
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2 mA, Note 1
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	TTL
V_{IL}	Input Low Voltage	−0.5	0.8	V	TTL
CO	Output Capacitance		8	pF	
CI	Input Capacitance		8	pF	
C_{IO}	Input/Output Capacitance		16	pF	
I_{LI}	Input Leakage Current	−10	10	μA	
O_{LI}	Output Leakage Current	−10	10	μA	
I_{CC}	Operating Supply Current		80	mA	VIN = V_{CC} or GND V_{CC} = 5.25V Outputs Unloaded

Note 1: 2 mA output pads: $\overline{EABUF}$, $\overline{EDBUF}$, DIR, $\overline{CRTINT}$, $\overline{NMI}$, CPURDY, $\overline{SWTR}$, HSYNC, VSYNC, $\overline{BLANK}$, $\overline{DACR}$, $\overline{DACW}$

4 mA output pads: P7-P0, DA7-DA0, MD31-MD0.

8 mA output pads: $\overline{RAS0}$, $\overline{RAS3}$, $\overline{WE}$

12 mA output pads: $\overline{OE}$

20 mA output pads: $\overline{CAS}$

UMC

UM6845/A/B

CRT Controller

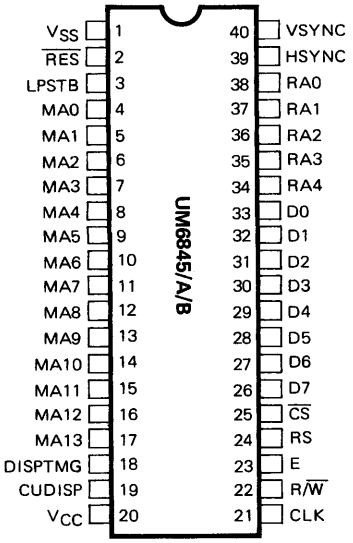
Features

- Applications including smart, programmable, intelligent CRT terminals; video games; information display
- Alphanumeric, semi-graphic, and full graphic capabilities
- Fully programmable via processor data bus with timing generation for almost any alphanumeric screen density
- Single +5 volt supply; TTL compatible I/O; NMOS technology
- Hardware scrolling by page, line, or character
- Provides CPUs with synchronous signals to external device
- Programmable cursor format
- Light pen registers and input strobe signal to latch light pen position on screen
- Operates without line buffer or external DMA; reading screen memory mutliplexed between CRTC and CPU
- Programmable interlace or non-interlace scan
- 14-bit display memory reading address width

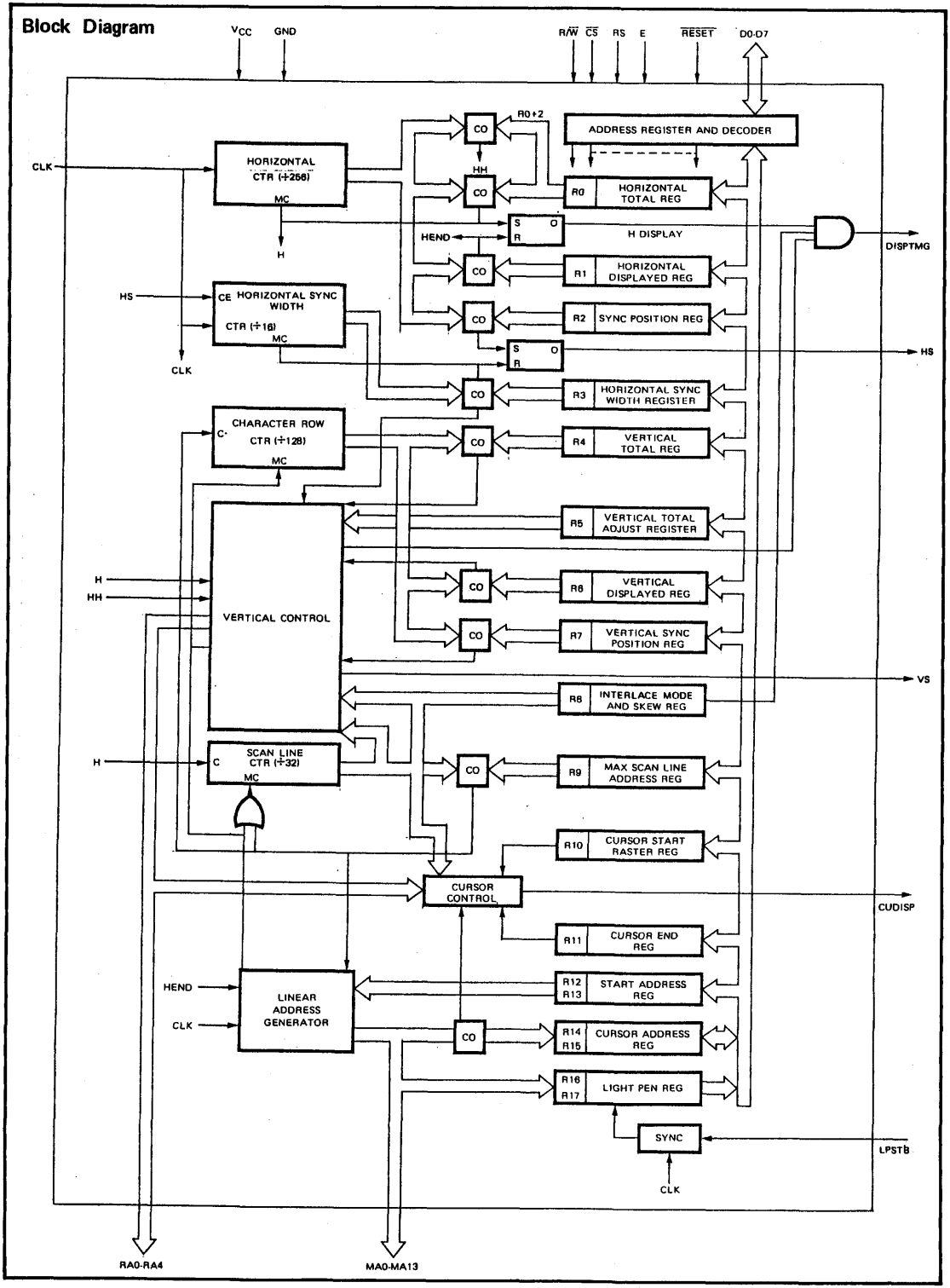
General Description

The CRTC UM6845/A/B comprises LSI controllers designed to provide interface between microcomputers and raster-scan-type CRT displays. The CRTC belongs to the MC6800 LSI family and is fully compatible with CPUs in both data lines and control lines. Its primary function is to generate timing signals which are necessary for raster-scan type CRT displays according to the specifications programmed by the CPU.

Pin Configuration



Block Diagram



Absolute Maximum Ratings *

Supply Voltage, V_{CC}** . . . . . −0.3~+7.0V
Input Voltage, V_{IN}** . . . . . −0.3~+7.0V
Operating Temperature, T_{OPR} . . . . . 0°~70°C
Storage Temperature, T_{STG} . . . . . −55°~+150°C

**With respect to V_{SS} (SYSTEM GND)

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(V_{CC} = 5V ± 5%, T_A = 0°C ~ 70°C)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	–		4.75	5.0	5.25	V
Input Voltage	V_{IL}	–		−0.3	–	0.8	V
	V_{IH}	–		2.0	–	V_{CC}	V
Input Leakage Current	I_{IN}	V_{IN} = 0 – 5.25V (Except D0 – D7)		−2.5	–	2.5	μA
Three-State Input Current (Off-State)	I_{TSI}	V_{IN} = 0.4 – 2.4V V_{CC} = 5.25V (D0 – D7)		−10	–	10	μA
Output "High" Voltage	V_{OH}	I_{LOAD} = 205A (D0 – D7)		2.4	–	–	V
		I_{LOAD} = −100μA (Other Outputs)					
Output "Low" Voltage	V_{OL}	I_{LOAD} = 1.6mA		–	–	0.4	V
Input Capacitance	C_{IN}	V_{IN} = 0 T_A = 25°C F = 1.0 MHz	D0 – D7	–	–	12.5	pF
			Other Inputs	–	–	10.0	pF
Output Capacitance	C_{OUT}	V_{IN} = 0V, T_A = 25°C, f = 1.0 MHz		–	–	10.0	pF
Power Dissipation	P_D	T_A = 25°C, V_{CC} = 5.0V		–	–	1000	mW

Display

AC Characteristics

(V_{CC} = 5V ± 5%, T_A = 0°C ~ 70°C)

BUS TIMING CHARACTERISTIC

MPU READ TIMING*

Item	Symbol	UM6845			UM6845A			UM6845B			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Enable Cycle Time	$t_{cyc}E$	1.0	–	–	0.666	–	–	0.5	–	–	μs
Enable "High" Pulse Width	PW_{EH}	0.45	–	–	0.280	–	–	0.22	–	–	μs
Enable "Low" Pulse Width	PW_{EL}	0.40	–	–	0.280	–	–	0.21	–	–	μs
Enable Rise and Fall Time	t_{Er}, t_{Ef}	–	–	25	–	–	25	–	–	25	μs
Address Set-up Time	t_{AS}	140	–	–	140	–	–	70	–	–	ns
Data Delay Time	t_{DDR}	–	–	320	–	–	200	–	–	180	ns
Data Hold Time	t_H	10	–	–	10	–	–	10	–	–	ns
Address Hold Time	t_{AH}	10	–	–	10	–	–	10	–	–	ns
Data Access Time	t_{ACC}	–	–	460	–	–	360	–	–	250	ns

* See Fig. 1

MPU WRITE TIMING*

Item	Symbol	UM6845			UM6845A			UM6845B			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Enable Cycle Time	$t_{cyc}E$	1.0	–	–	0.666	–	–	0.5	–	–	μs
Enable "High" Pulse Width	PW_{EH}	0.45	–	–	0.280	–	–	0.22	–	–	μs
Enable "Low" Pulse Width	PW_{EL}	0.40	–	–	0.280	–	–	0.21	–	–	μs
Enable Rise and Fall Time	t_{Er}, t_{Ef}	–	–	25	–	–	25	–	–	25	ns
Address Set-up Time	t_{AS}	140	–	–	140	–	–	70	–	–	ns
Data Set-up Time	t_{DSW}	195	–	–	80	–	–	60	–	–	ns
Data Hold Time	t_H	10	–	–	10	–	–	10	–	–	ns
Address Hold Time	t_{AH}	10	–	–	10	–	–	10	–	–	ns

* See Fig. 2

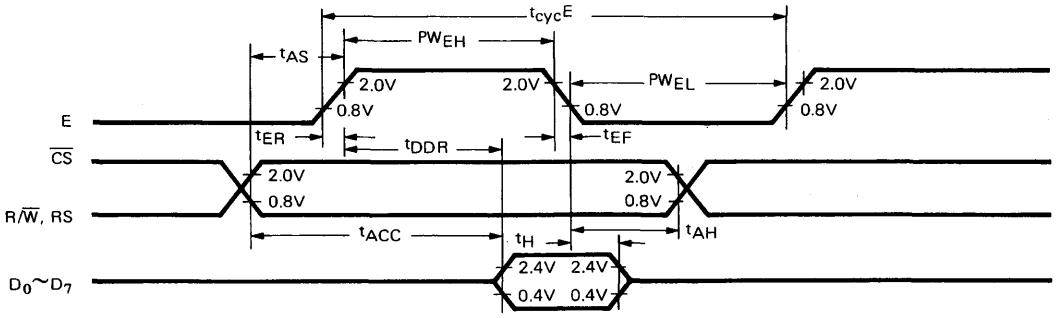


Figure 1. Read Sequence

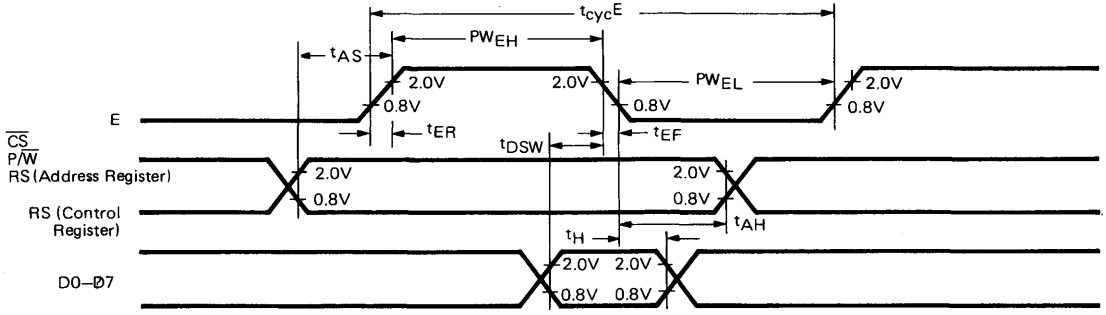


Figure 2. Write Sequence

CRTC SIGNAL TIMING*

Item	Symbol	Min.	Typ.	Max.	Unit
Clock Cycle Time	$t_{cyc}C$	270	–	–	ns
Clock "High" Pulse Width	PW_{CH}	130	–	–	ns
Clock "Low" Pulse Width	PW_{CL}	130	–	–	ns
Rise and Fall Time for Clock Input	t_{Cr}, t_{Cf}	–	–	20	ns
Memory Address Delay Time	t_{MAD}	–	–	160	ns
Raster Address Delay Time	t_{RAD}	–	–	160	ns
DISPTMG Delay Time	t_{DTD}	–	–	250	ns
CUDISP Delay Time	t_{CDD}	–	–	250	ns
Horizontal Sync Delay Time	t_{HSD}	–	–	200	ns
Vertical Sync Delay Time	t_{VSD}	–	–	250	ns
Light Pen Strobe Pulse Width	PW_{LPH}	60	–	–	ns
Light Pen Strobe	t_{LPD1}	–	–	70	ns
Uncertain Time of Acceptance	t_{LPD2}	–	–	0	ns

* See Fig. 3; Fig. 4

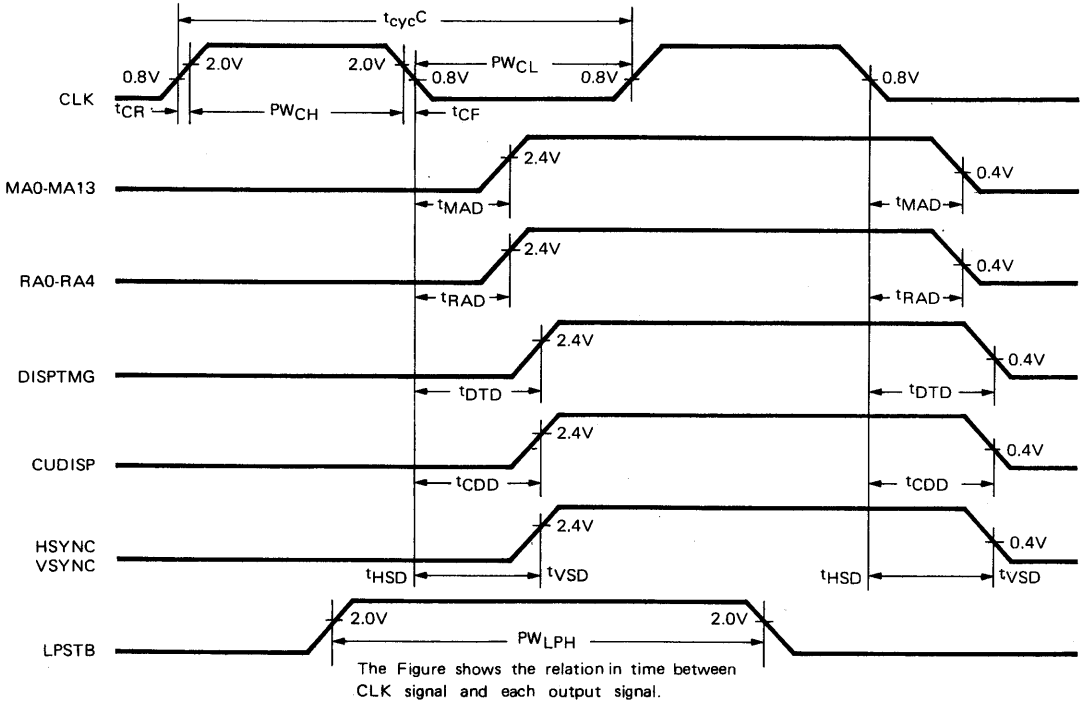
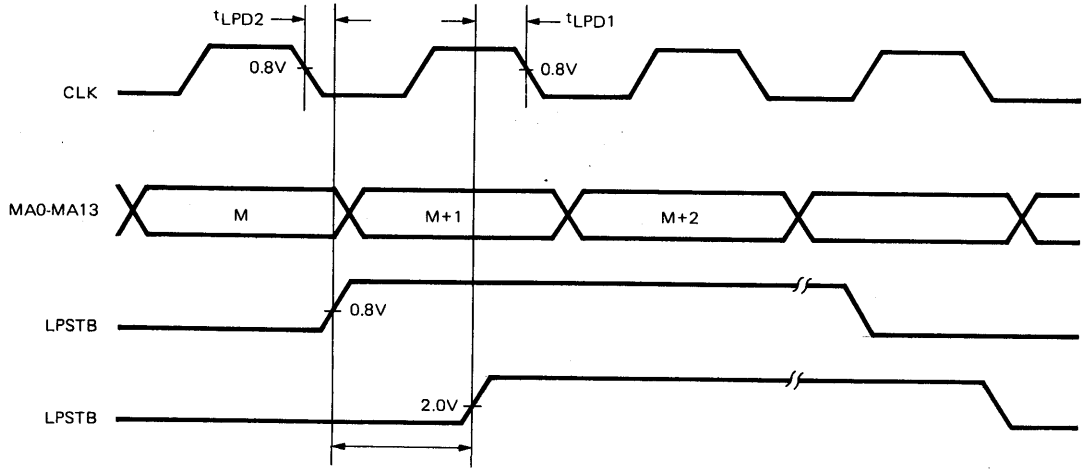


Figure 3. CRTC Timing Chart



t_{LPD1}, t_{LPD2}: LPSTB's uncertain time of acceptance.

When LPSTB rises in this period, Display Memory Address "M+2" is set into the light pen register.

Figure 4. LPSTB Input Timing & Display Memory Address is Set Into the Light Pen Register.

Typical CRT Controller Application Block Diagram

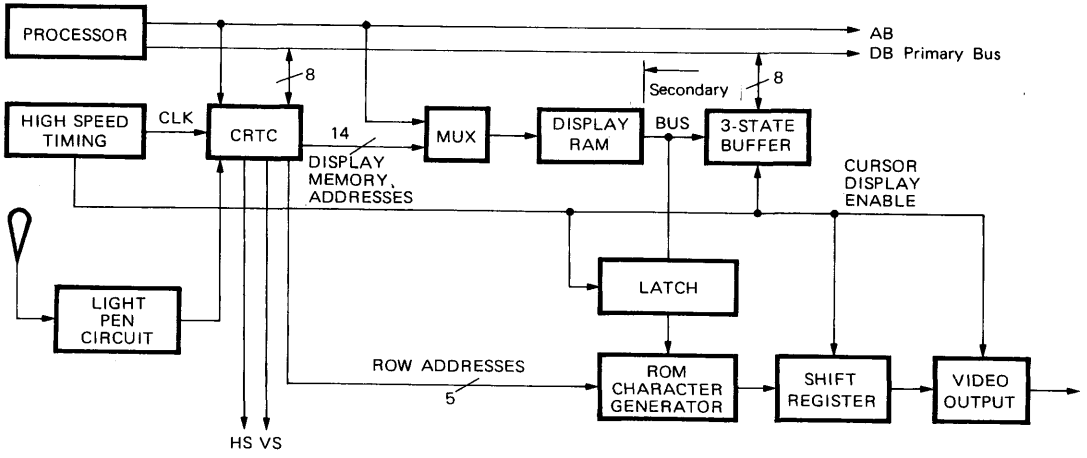


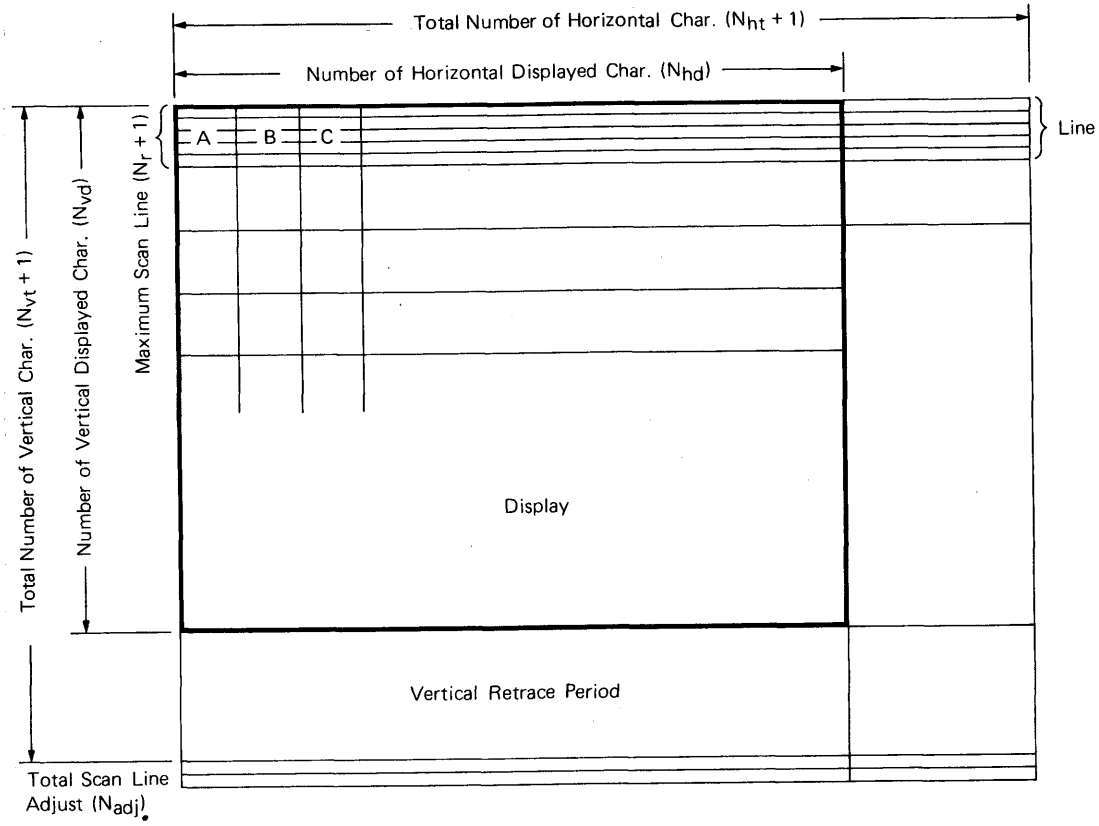
Figure 5. Typical CRT Controller Application

CRT Screen Format and Time Chart

REGISTER PROGRAMMED VALUES

Register	Register Name	Specified Value	Programmed (Written) Value
R0	Horizontal Total	$N_{ht}+1$	N_{ht}
R1	Horizontal Displayed	N_{hd}	N_{hd}
R2	Horizontal Sync Position	$N_{hsp}+1$	N_{hsp}
R3	Sync Width	N_{vsw}, N_{hsw}	N_{vsw}, N_{hsw}
R4	Vertical Total	$N_{vt}+1$	N_{vt}^{*}
R5	Vertical Total Adjust	N_{adj}	N_{adj}
R6	Vertical Displayed	N_{vd}	N_{vd}
R7	Vertical Sync Position	$N_{vsp}+1$	N_{vsp}
R8	Interlace & Skew		
R9	Maximum Raster Address	N_r+1/N_r+2	N_r
R10	Cursor Start Raster	N_{CSTART}	
R11	Cursor End Raster	N_{CEND}	
R12	Start Address (H)	0	
R13	Start Address (L)	0	
R14	Cursor (H)		
R15	Cursor (L)		
R16	Light Pen (H)		
R17	Light Pen L (L)		

SCREEN FORMAT



RESTRICTIONS ON PROGRAMMING INTERNAL REGISTER

(1) $0 < N_{hd} < N_{ht} + 1 \leqslant 256$

(2) $0 < N_{vd} < N_{vt} + 1 \leqslant 128$

(3) $0 \leqslant N_{hsp} \leqslant N_{ht}$

(4) $0 \leqslant N_{vsp} \leqslant N_{vt}$

(5) $0 \leqslant N_{CSTART} \leqslant N_{CEND} \leqslant N_r$ (Non-Interlace, Interlace Sync Modes)

$0 \leqslant N_{CSTART} \leqslant N_{CEND} \leqslant N_r + 1$ (Interlace Sync & Video Modes)

(6) $2 \leqslant N_r \leqslant 30$

(7) $3 \leqslant N_{ht}$ (Except Non-Interlace Mode)

$5 \leqslant N_{ht}$ (Non-Interlace Mode Only)

CRTC ADDRESSING FOR READING DISPLAY MEMORY

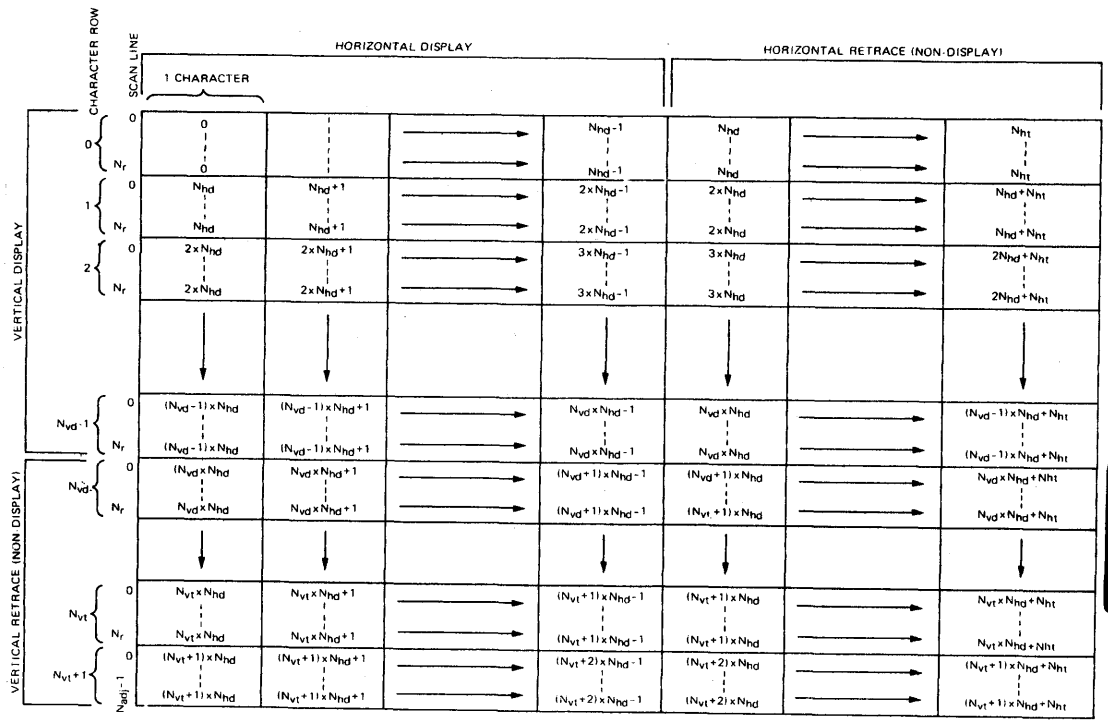


Figure 6. Display Memory Addressing (MA0-MA13) Stage Chart

Note: The initial MA is determined by the contents of state address register R12/R13. Timing is shown for R12/R13 = 0. Only Non-Interlace-and Interlace Sync Modes are shown.

CRTC HORIZONTAL TIMING

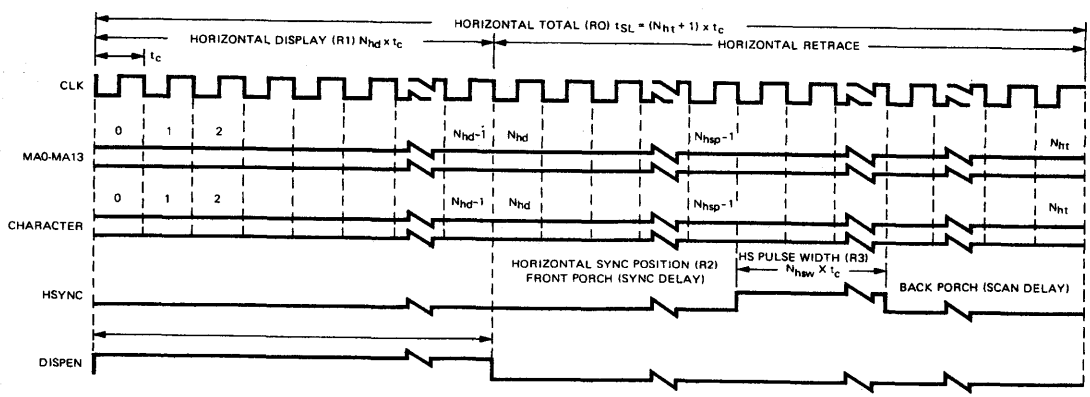


Figure 7. CRTC Horizontal Timing

CRTC VERTICAL TIMING

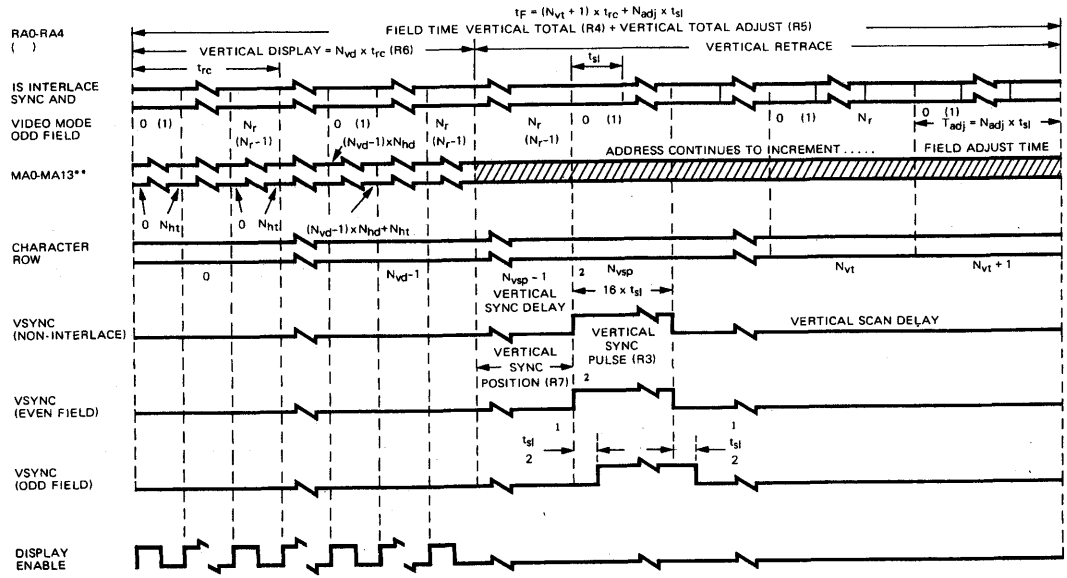


Figure 8. CRTC Vertical Timing

Notes: 1. The odd field is offset ½ horizontal scan time.

2. Vertical sync pulse may be programmed from 1 to 16 scan line times.

CURSOR DISPLAY TIMING

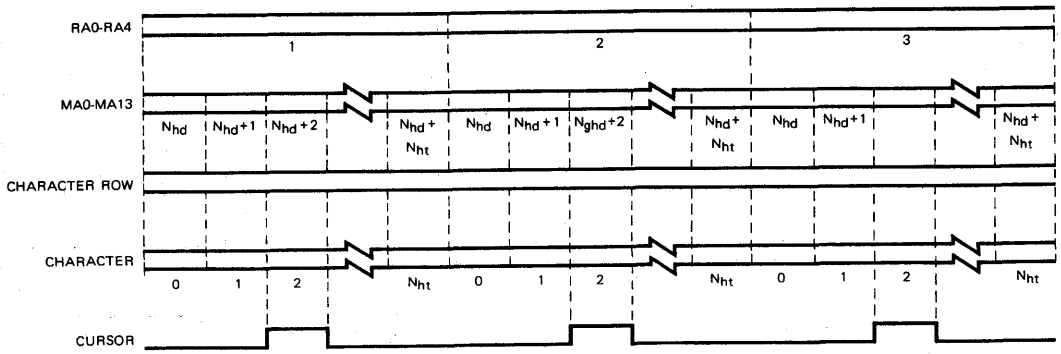


Figure 9. Cursor Timing

Notes: 1. Timing is shown for non-interlace and interlace modes.

2. Cursor Register = N_{hd} + 2.
3. Cursor start = 1.
4. Cursor end = 3.
5. R12/R13 = 0 for start address registers.

Example of Raster Scan Display

Fig. 10 shows an example where the same character is displayed in the non-interlace, interlace sync, and interlace sync and video modes.

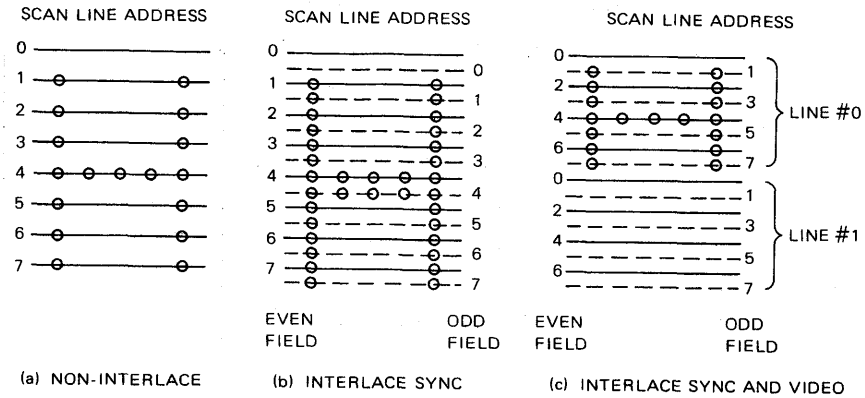


Figure 10. Interlace Control

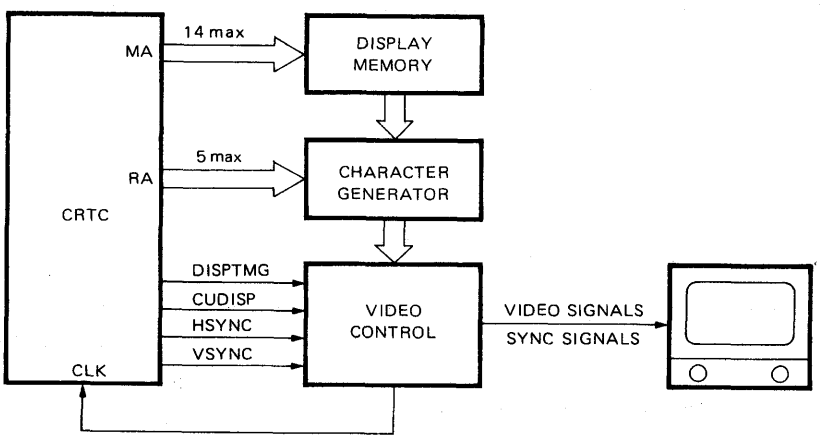


Figure 11. Interface to Display Control Unit

Fig. 11 shows the interface between the CRTC and the display control unit. The display control unit is mainly composed of Display Memory, Character Generator, and Video Control circuit. For display memory, 14 Memory Address lines (0-16383) are provided and for character generator, 5 Raster Address lines (0-31) are provided. For the video control circuit, DISPTMG signal is used to control the blank period of video signal. CUDISP signal is used as video signal to display the cursor on the CRT screen. Moreover, HSYNC and VSYNC signals are used as drive signals respectively for CRT horizontal and vertical deflection circuits.

Outputs from video control circuit (video signals and sync signals) are provided to CRT display unit to control the deflection and brightness of CRT, and thus characters displayed on the screen.

Circuitry Standards of Display Control Units

Fig. 12 shows a detailed schematic diagram of the display control unit. This diagram shows how to use CUDISP and DISPTMG signals. CUDISP and DISPTMG signals should be latched at least one time at external flip-flop F1 and F2, which creates a one-character delay time, so as to synchronize with the video signal from the parallel-serial converter. A high-speed D-type flip-flop as TTL is used for this purpose. After being delayed at F1 and F2, the DISPTMG signal is OR-ed with output from AND gate. By using this circuitry, blanking of horizontal and vertical retrace time is controlled and the cursor video is mixed with the character video signal.

Fig. 12 shows an example in which both display memory and CG can be accessed for horizontal one-character time. A time chart for this case is shown in Fig. 15 This method is used when a few characters need to be displayed horizontally on the screen.

When many characters are displayed horizontally on the screen and horizontal one-character time is so short that neither display memory nor CG can be accessed, the circuitry shown in Fig. 13 should be used. In this case, display memory output is latched and the CG is accessed at the next cycle. The time chart in this case is shown in Fig. 16 CUDISP and DISPTMG signals should be provided after being delayed by one-character time by using the skew bit of interface and the skew register (RS). Moreover, when there are troubles in the delay time of MA during horizontal one-character time on high speed display operation, the system shown in Fig. 14 should be adopted. The time chart in this case is shown in Fig. 17 Character video signal is delayed for a two-character time because each MA output and display memory outputs are latched and are made to be in phase with CUDISP and DISPTMG signals by delaying for a two-character time. Table 1 shows the circuitry selection standard of display units.

Table 1. Circuitry Standard of Display Control Unit

Case	Relation among t_{CH}, RM and CG	Timing Diagram	Interlace & Skew Register Bit Programming			
			C1	C0	D1	D0
1	$t_{CH} >$ RM Access + CG Access + t_{MAD}	Fig. 15	0	0	0	0
2	RM Access + CG Accwss + $t_{MAD} \geqslant t_{CH} >$ RM Access + t_{MAD}	Fig. 16	0	1	0	1
3	RM Access + $t_{MAD} \geqslant t_{CH} >$ RM Access	Fig. 17	1	0	1	0

t_{CH}: CHCP Period: t_{MAD}: MA Delay

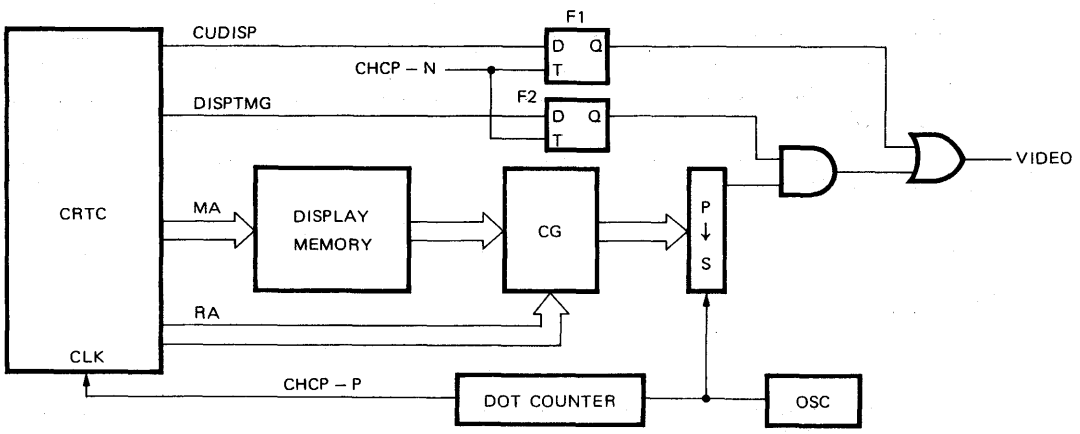


Figure 12. Display Control Unit (1)

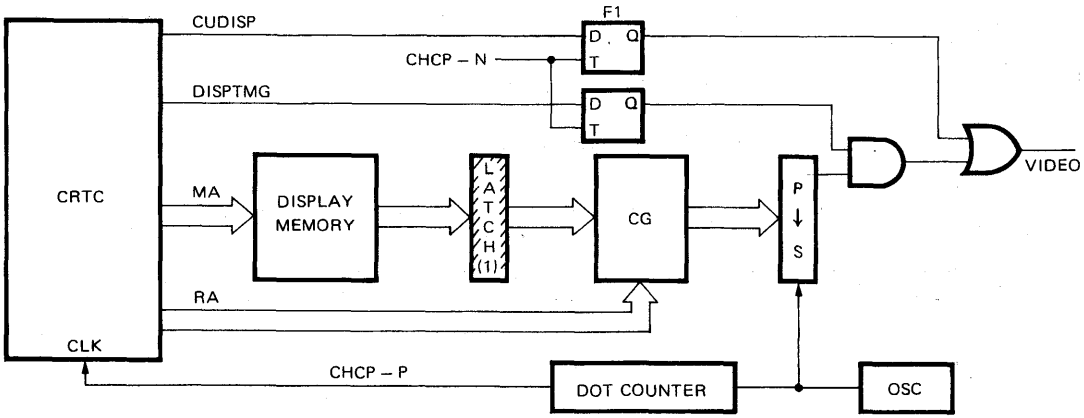


Figure 13. Display Control Unit (2)

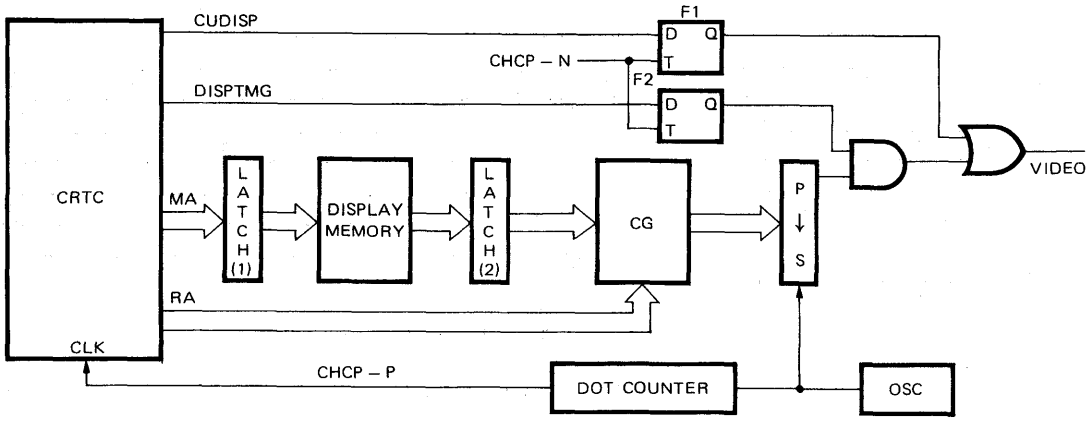


Figure 14. Display Control Unit (for high-speed display operation) (3)

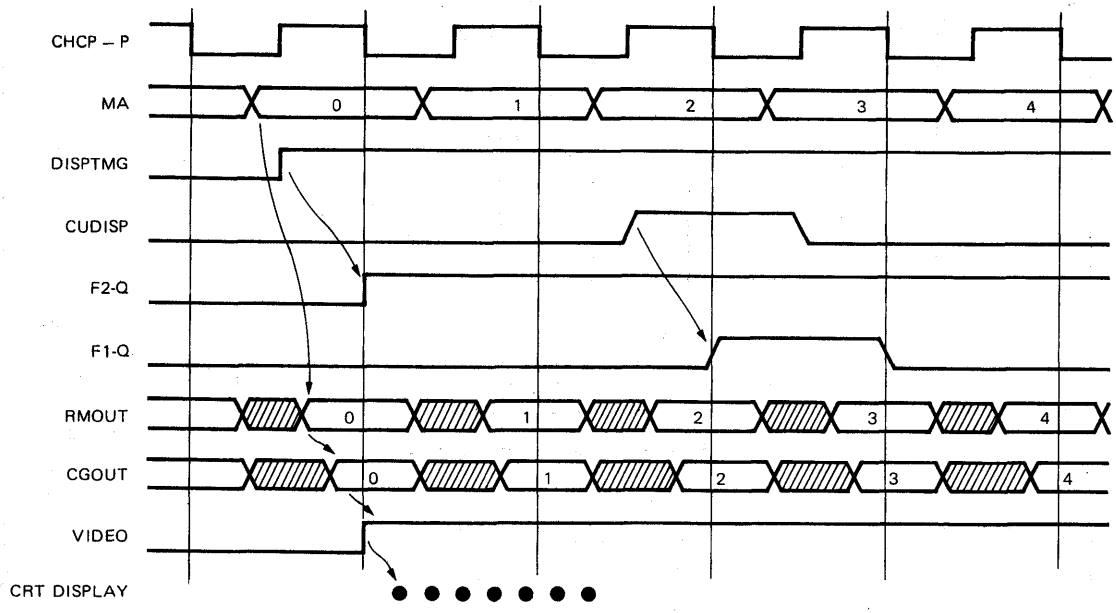


Figure 15. Time Chart of display Control Unit (1)

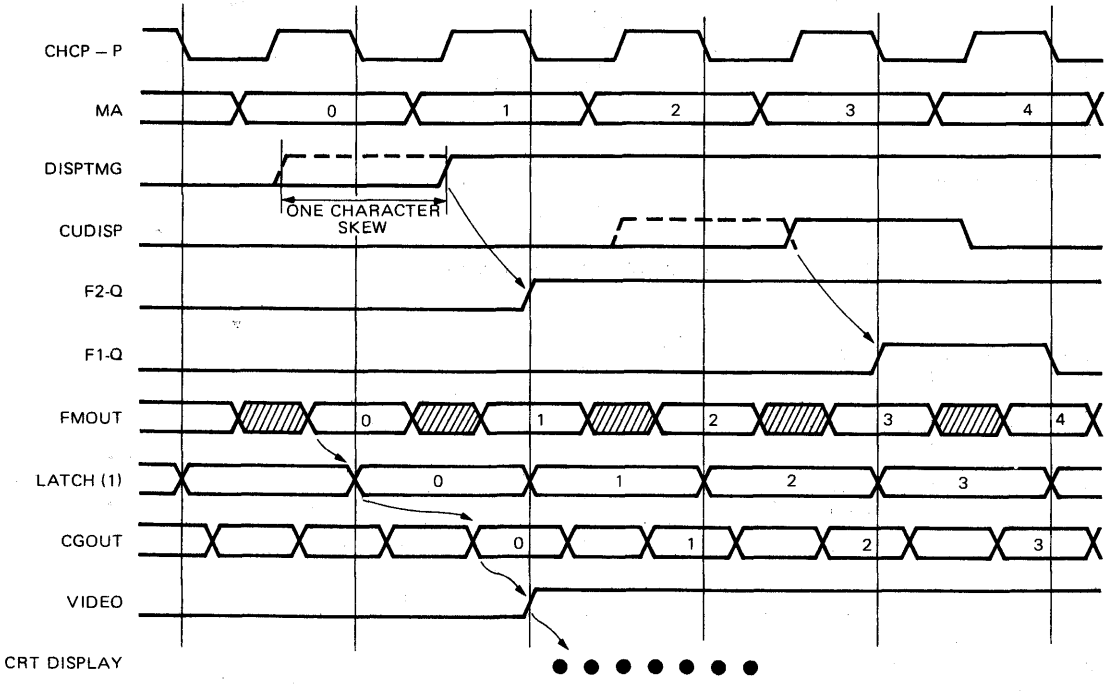


Figure 16. Time Chart of Display Control Unit (2)

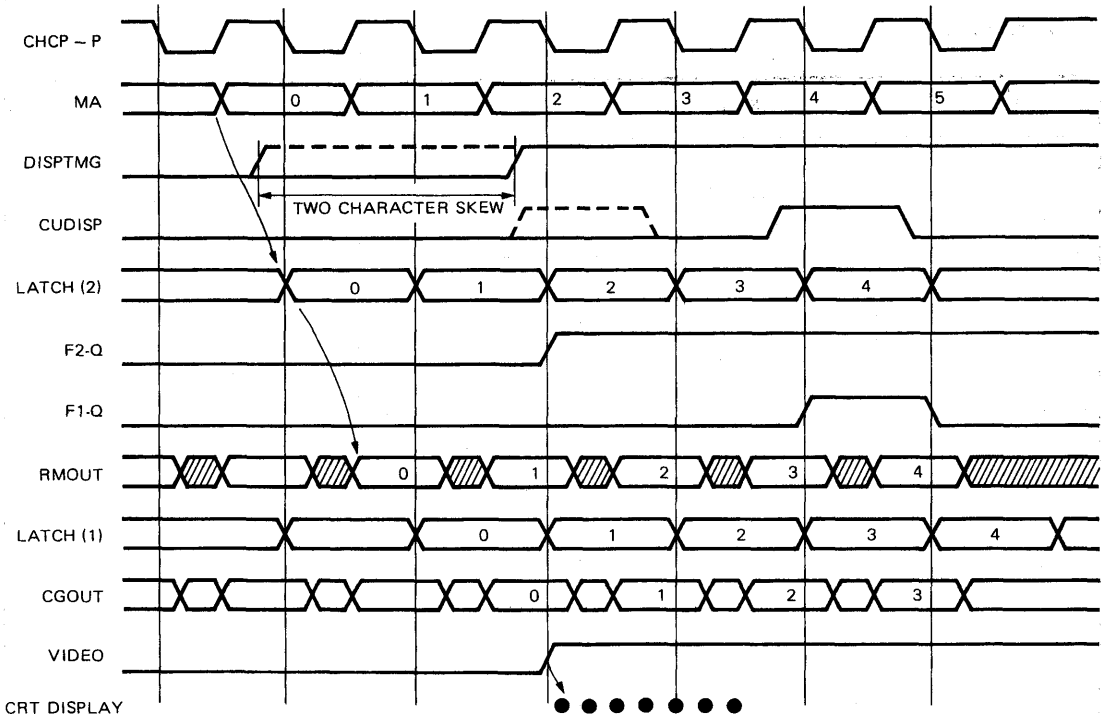


Figure 17. Time Chart of Display Unit (3)

How to Decide Parameters on the CRTC

Before the determination of parameters on the CRTC and the dot frequency of crystal, we must check the Specification of CRT Display Unit (Monitor) and the Screen Format. The output signal timing of CRTC, must be in the monitor specification for the normal display. (Such as DISPTMG, HSYNC, VSYNC.). Screen format includes:

(1) Horizontal display characters column number. (N_{hd})
(2) Vertical display row number. (N_{vd})
(3) Horizontal dot numbers per character. (Dot counter ($\div N\alpha$)).
(4) Vertical raster lines per row. ($N_r + 1$)

Example: for non-interlace mode one frame = 60Hz
then one raster line frequency
$= 60Hz \times [(N_{vt} + 1)(N_r + 1) + N_{adj}]$
CLK frequency of CRTC = raster line frequency $\times (N_{ht} + 1)$

dot frequency of crystal = $N\alpha \times$ CLK frequency of CRTC
$= 60Hz \times [(N_{vt} + 1)(N_r + 1) + N_{adj}] \times [N_{ht} + 1] \times N\alpha$

* Relation between R0-R7 is in Figure 18.

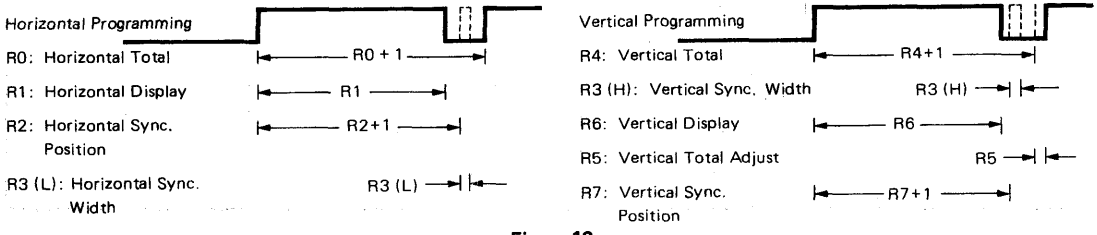


Figure 18.

Pin Description

Pin No.	Symbol	Name	Description
33, 32, 31, 30 29, 28, 27, 26	D0 –D7	Data Bus	Processor Interface
23	E	Enable	
25	$\overline{CS}$	Chip Select	
24	RS	Register Select	
22	R/$\overline{W}$	Read/Write	
40	VSYNC	Vertical Sync	CRT Control
39	HSYNC	Horizontal Sync	
18	DISPTMG	Display Enable	
4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17	MA0-MA13	Reading Memory Addresses	Reading Display Memory / Character Generator Addressing
38, 37, 36, 35, 34	RA0-RA4	Raster Addresses	
19	CUDISP	Cursor	Other Pins
21	CLK	Clock	
3	LPSTB	Light Pen Strobe	
20, 1	V_{CC} (+) V_{SS} (–)	Power	
2	$\overline{RES}$	Reset	

PROCESSOR INTERFACE

The CRTC interfaces to a processor bus on the bidirectional data bus (D0-D7) using $\overline{CS}$. RS. E. and R/$\overline{W}$ as control signals.

Data Bus (D0-D7)
The bidirectional data lines (D0-D7) allow data transfers between the CRTC internal register file and the processor. The data bus output drivers are 3-state buffers which remain in the high impedance state except when the processor performs a CRTC read operation.

Enable (E)
The Enable pin is a high impedance TTL/MOS compatible input which enables the data bus input/output buffers and clocks data to and from the CRTC. This signal is usually derived from the processor clock and the high to low transition is the active edge.

Chip Select ($\overline{CS}$)
The $\overline{CS}$ line is a high impedance TTL/MOS compatible input which selects the CRTC, when low, to read or write the internal Register File. This signal should only be active when there is a valid stable address being decoded from the processor.

Register Select (RS)
The RS line is a high impedance TTL/MOS compatible input which selects either the Address Register (RS = "0") or one of the Data Registers (RS = "1") of the internal Register File.

Read/Write (R/$\overline{W}$)
The R/$\overline{W}$ line is a high impedance TTL/MOS compatible input which determines whether the internal Register File gets written or read. A write is active at low ("0").

CRT CONTROL

The CRTC provides Horizontal Sync (HS), Vertical Sync (VS), and Display Enable (DISPTMG) signals.

Vertical Sync (V SYNC)
The TTL compatible output is an active high signal which drives the monitor directly or is fed to Video Processing Logic for composite signal generation. This signal determines the vertical position of the displayed text.

Horizontal Sync (H SYNC)
This TTL compatible output is an active high signal which drives the monitor directly or is fed to Video Processing Logic for composite generation. This signal determines the horizontal position of the displayed text.

Display Enable (DISPTMG)
This TTL compatible output is an active high signal which indicates the CRTC is providing addressing in the active display area.

READING DISPLAY/CHARACTER GENERATOR ADDRESSING

The CRTC provides Memory Addresses (MA0-MA13) to scan the display RAM. Also provided are Raster Addresses (RA0-RA4) for the character ROM.

Reading Memory Addresses (MA0-MA13)
These 14 outputs are used to read the display memory.

Raster Addresses (RA0-RA4)
These 5 outputs from the internal Raster Counter address the character ROM for the row of a character.

OTHER PINS

Cursor (CUDISP)
This output signal indicates the cursor display signal sent to the video processing logic to display in the proper area.

Clock (CLK)
CLK, TTL/MOS compatible input is used to synchronize all CRT control signals. An external dot counter is used to derive this signal which is usually the character rate in an alphanumeric CRT. The active transition is high to low.

Light Pen Strobe (LPSTB)
This high impedance TTL/MOS compatible input latches the current display memory address in the register file. Latching is on the low to high edge and is synchronized internally to character clock.

V_{CC}, Gnd (V_{CC}, V_{SS}) Power Supply Pins.
Reset ($\overline{RES}$)
The $\overline{RES}$ input is used to reset the CRTC. An input low level on $\overline{RES}$ forces CRTC into the following status:

(a) All the counters in CRTC are cleared and the device stops the display operation.
(b) All the outputs go to low level.
(c) Control registers in CRTC remain unchanged.

This signal is different from other MC 6800 family in the following functions:

(a) $\overline{RES}$ signal has capability of reset function only when LPSTB is at low level.
(b) The CRTC starts the display operation immediately after the release of $\overline{RES}$ signal.

CRTC INTERNAL REGISTER ASSIGNMENT

Table 2. CRTC Internal Registers

$\overline{CS}$	RS	Address Register 4	3	2	1	0	Register #	Register File	Program Unit	Read	Write	Number of Bits 7	6	5	4	3	2	1	0
1	X	X	X	X	X	X	X	–	–	–	–								
0	0	X	X	X	X	X	AR	Address Register	–	No	Yes								
0	1	0	0	0	0	0	R0	Horizontal Total *	Char.	No	Yes								
0	1	0	0	0	0	1	R1	Horizontal Displayed	Char.	No	Yes								
0	1	0	0	0	1	0	R2	H. Sync Position*	Char.	No	Yes								
0	1	0	0	0	1	1	R3	Sync Width	V-Raster H-Char.	No	Yes	V1	V1	V1	V1	H	H	H	H
0	1	0	0	1	0	0	R4	Vertical Total *	Char. Row	No	Yes								
0	1	0	0	1	0	1	R5	V. Total Adjust	Scan Line	No	Yes								
0	1	0	0	1	1	0	R6	Vertical Displayed.	Char. Row	No	Yes								
0	1	0	0	1	1	1	R7	V. Sync Position*	Char. Row	No	Yes								
0	1	0	1	0	0	0	R8	Interface Mode and Skew	–	No	Yes	C_1	C_0	D_1	D_0			I_1	I_0
0	1	0	1	0	0	1	R9	Max Scan Line Address	Scan Line	No	Yes								
0	1	0	1	0	1	0	R10	Cursor Start Raster	Scan Line	No	Yes		B	P					
0	1	0	1	0	1	1	R11	Cursor End Raster	Scan Line	No	Yes								
0	1	0	1	1	0	0	R12	Start Address (H)	–	Yes	Yes	0	0						
0	1	0	1	1	0	1	R13	Start Address (L)	–	Yes	Yes								
0	1	0	1	1	1	0	R14	Cursor (H)	–	Yes	Yes	0	0						
0	1	0	1	1	1	1	R15	Cursor (L)	–	Yes	Yes								
0	1	1	0	0	0	0	R16	Light Pen (H)	–	Yes	No	0	0						
0	1	1	0	0	0	1	R17	Light Pen (L)	–	Yes	No								

Table 2. Shows The Register File In CRTC, The Registers Marked* (Written Value) = (Specified Value) – 1

REGISTER DESCRIPTION

Address Register (AR)

The Address Register is a 5-bit write-only register used as an "indirect" or "pointer" register. Its contents are the address of one of the other 18 registers in the file. When RS and $\overline{CS}$ are low, the Address Register itself is addressed. When RS is high, the register file is accessed. (see Table 2).

Horizontal Total Register (R0)

This 8 bit Register determines the horizontal frequency of H Sync output. It is the total of displayed plus non-displayed character time units minus one.

Horizontal Displayed Register (R1)

This 8 bit register determines the number of displayed characters per horizontal line.

Horizontal Sync Position Register (R2)

This 8 bit register determines the horizontal sync position on the horizontal line.

Sync Width Register (R3)

V	V	V	V	H	H	H	H

This 8 bit write-only register determines the width of the Vertical Sync (VS) pulse and the Horizontal Sync (HS) pulse.

The HS pulse width may be programmed from 1-to-15 character clock periods. The VS pulse width may be programmed from 1-to-16 Raster scan lines. (see Table 3).

Vertical Total Register (R4) and Vertical Total Adjust Register (R5)

The vertical frequency of VSYNC is determined by both R4 and R5. The calculated number of character line times is usually an integer plus a fraction to get exactly a 50 or 60 Hz vertical refresh rate. The integer number of Character line times minus one is programmed in the 7 bit write-only Vertical Total Register, the fraction is programmed in the 5 bit write-only Vertical Scan Adjust Register as a number of scan line times.

Vertical Displayed Register (R6)

This 7-bit write-only register specifies the number of displayed character rows on the CRT screen, and is programmed in character row times. Any number smaller than the contents of R4 may be programmed into R6.

Vertical Sync Position (R7)

This 7-bit write-only register controls the position of vertical sync with respect to the reference. It is programmed in character row times. Any number equal to or less than the vertical total (R4) may be used.

Interlace Mode and Skew Register (R8)

C_1	C_0	D_1	D_0			I_1	I_0

This is a register used to program raster scan mode and skew of CUDISP signals and DISPTMG signals. In the non-interlace mode, the rasters of even number field and odd number field are scan duplicated. In the interlace sync mode, the rasters of odd number field are scanned in the middle of even number fields. Thus, the same character pattern is displayed in both fields. In the interlace sync and video mode, the raster scan method is the same as the interlace sync mode, but it is controlled to display different character patterns in two fields. Skew function is used to delay the output timing of CUDISP and DISPTMG signals such that they are synchronized with serial video output signals. This is due to the time delay from display memory data to serial output character pattern. (see Table 4).

Table 3. Sync Width Register

VSW				Pulse Width Unit: H
2^7	2^6	2^5	2^4	
0	0	0	0	16H
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

H: Raster Period

HSW				Pulse Width Unit: CH
2^3	2^2	2^1	2^0	
0	0	0	0	Not Used
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

CH: Character Clock Period

Table 4. Interlace Mode and Skew Register

Interlace Mode (2^1, 2^0)	I_1	I_0	Raster Scan Mode
	0	0	Non-Interlace Mode
	1	0	Non-Interlace Mode
	0	1	Interlace Sync Mode
	1	1	Interlace Sync & Video Mode
Cursor Skew Bit (2^7, 2^6)	C_1	C_0	CUDISP Signal
	0	0	Non-Skew
	0	1	One-Character Skew
	1	0	Two-Character Skew
	1	1	Non-Output
DISPTMG Skew Bit (2^5, 2^4)	D_1	D_0	DISPTMG Signal
	0	0	Non-Skew
	0	1	One-Character Skew
	1	0	Two-Character Skew
	1	1	Non-Ouptut

Maximum Raster Address Register (R9)

This is a register used to program maximum raster addresses within 5-bits. This register defines total number of rasters per character including space. This register is programmed as follows.

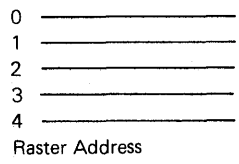
For Non-interlace Mode, Interlace Sync Mode

When total number of rasters is RN, (RN-1) shall be programmed.

For Interlace Sync & Video Mode

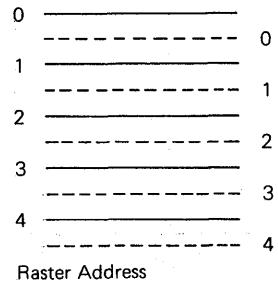
When total number of rasters is RN, (RN-2) shall be programmed.

Non-Interlace Mode



Total Number of Rasters 5
Programmed Value $N_r = 4$
(The same as displayed total number of rasters)

Interlace Sync Mode



Total Number of Rasters 5
Programmed Value $N_r = 4$
(In the interlace sync mode, total number of rasters in both the even and odd fields is ten. On programming, half of it is defined as total number of rasters).

Interlace Sync & Video Mode

0 ——————————
---------- 1
2 ——————————
---------- 3
4 ——————————

Total Number of Rasters 5
Programmed Value $N_r = 3$
(Total number of rasters is displayed in the even field and the odd field)

Cursor Start Raster Register (R10)

	B	P					

This is a register used to program the cursor start raster address by lower 5-bits (2^0-2^4) and the cursor display mode higher 2-bits (2^5, 2^6). (see Table 5).

Table 5. Cursor Display Mode

Cursor Display Mode	B	P	Cursor Display Mode
(2^6, 2^5)	0	0	Non-blink
	0	1	Cursor Non-display
	1	0	Blink, 16 Field Period
	1	1	Blink, 32 Field Period

Cursor End Raster Register (R11)
This is a register used to program to cursor end raster address.

Start Address Register (R12, R13)
These are used to program the first address of refresh memory to read out. Paging and Scrolling is easily performed using this register. This register can be read but the higher 2-bits (2^6, 2^7) of R12 are always '0 ".

Cursor Register (R14, R15)
These two read/write registers store the cursor location. The higher 2-bits (2^6, 2^7) of R14 are always "0".

Light Pen Register (R16, R17)
These read-only registers are used to catch the detection address of the light pen. The higher 2-bits (2^6, 2^7) of R16 are always "0". Its value needs to be corrected by software because there is time delay from the address output of the CRTC to the signal input LPSTB pin of the CRTC. In the process raster is lit after the address output and the light pen detects it.

CRTC Register Comparison Table

NON-INTERLACE

Register	UM6845R/RA/RB MC6845 MC6845*1	MC6845R HD6845R	UM6845/A/B HD6845S	UM6845E/EA/EB
R0 Htotal	Total-1	Total-1	Total-1	Total-1
R1 Hdisp	Actual	Actual	Actual	Actual
R2 Hsync	Actual	Actual	Actual	Actual
R3 Sync Width	Horizontal (& Vertical *1)	Horizontal	Horizontal & Vertical	Horizontal & Vertical
R4 Vtotal	Total-1	Total-1	Total-1	Total-1
R5 Vtotal Adjustment	Any Value	Any Value	Any Value	Any Value
R6 Vdisp	Any Value <R4	Any Value <R4	Any Value <R4	Any Value <R4
R7 Vsync	Actual-1	Actual-1	Actual-1	Actual-1
R8 B0-B1	Interlace	Interlace	Interlace	Interlace
Mode Select B2	–	–	–	Row/Column or Binary Addr.
B3	–	–	–	Shared or Transparent Addr.
B4	(Display Enable Skew *1)	–	Display Enable Skew	Display Enable Skew
B5	(Display Enable Skew *1)	–	Display Enable Skew	Cursor Skew
B6	(Cursor Skew *1)	–	Cursor Skew	RA4/
B7	(Cursor Skew *1)	–	Cursor Skew	Transparent
R9 Scan Lines	Total-1	Total-1	Total-1	Total-1
R10 Cursor Start	Actual	Actual	Actual	Actual
R11 Cursor End	Actual	Actual	Actual	Actual
R12/R13 Display Addr.	Write Only Read/Write (MC6845 & *1)	Read/Write	Read/Write	Write Only
R14/R15 Cursor Position	Read/Write	Read/Write	Read/Write	Read/Write
R16/R17 Position	Read Only	Read Only	Read Only	Read Only
R18/R19 Update Addr. Register	N/A	N/A	N/A	Transparent Mode Only
R31 Dummy Register	N/A	N/A	N/A	Transparent Mode Only
Status Register	Yes (UM6845R)	No	No	Yes

CRTC Register Comparison Table (Continued)

INTERLACE SYNC

Register	UM6845R/RA/RB MC6845 MC6845*1	MC6845R HD6845R	UM6845/A/B HD6845S	UM6845E/EA/EB
R0 Htotal	Total-1 = Odd or Even	Total-1 = Odd	Total-1 = Odd	Total-1 = Odd or Even

INTERLACE SYNC AND VIDEO

R4 Vtotal	Total-1	Total-1	Total-1	Total-1
R6 Vdisp	Total	Total/2	Total	Total
R7 Vsync	Actual-1	Actual-1	Actual-1	Actual-1
R9 Scan Lines	Total-1 Odd/Even	Total-1 Only Even	Total-1 Odd/Even	Total-1 Odd/Even
R10 Cursor Start	Odd/Even	Both Odd	Odd/Even	Odd/Even
R11 Cursor End	Odd/Even	Both Even	Odd/Even	Odd/Even
Cclk	2.5 MHz	2.5 MHz	3.7 MHz	3.7 MHz

Ordering Information

Part Number	CPU Clock Rate	Package
UM6845	1MHz	40L DIP
UM6845A	1.5MHz	40L DIP
UM6845B	2MHz	40L DIP

UMC

UM6845R/RA/RB

CRT Controller

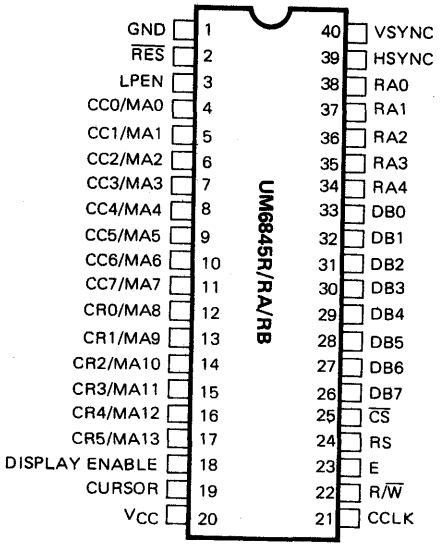
Features

- Single + 5 volt (±5%) power supply
- Alphanumeric and limited graphics capabilities
- Fully programmable display (rows, columns, blanking, etc.)
- Interlaced or non-interlaced scan
- 50/60 Hz operation
- Fully programmable cursor
- External light pen capability
- Capable of addressing up to 16K character Video Display RAM.
- No DMA required
- Straight-binary addressing for Video Display RAM

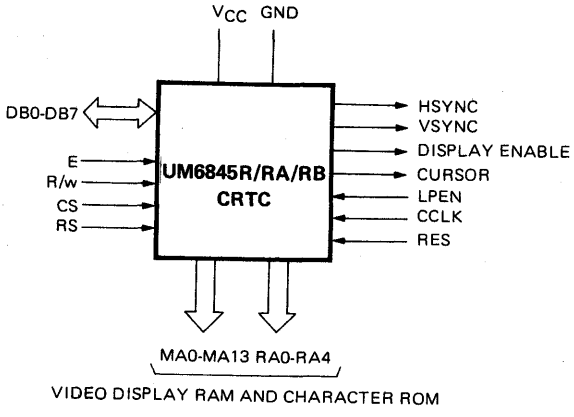
General Description

The UM6845R/RA/RB is a CRT Controller intended to provide capability for interfacing any microprocessor family to CRT or TV-type raster scan displays. A unique feature is the inclusion of several modes of operation, so that the system designer can configure the system with a wide assortment of techniques.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Supply Voltage, V_{CC} . . . . . −0.3V to + 7.0V
Input/Output Voltage, V_{IN} . . . . . −0.3V to + 7.0V
Operating Temperature, T_{OP} . . . . . 0°C to 70°C
Storage Temperature, T_{STG} . . . . . −55°C to 150°C
Notice:
All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

*Comments

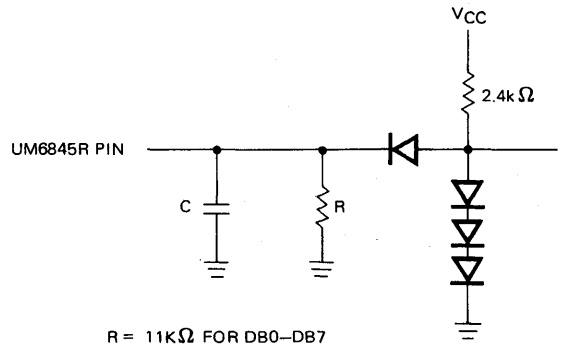
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(V_{CC} = 5.0V ± 5%, T_A = 0 – 70°C, unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage	2.0		V_{CC}	V
V_{IL}	Input Low Voltage	−0.3		0.8	V
I_{IN}	Input Leakage (ϕ2, R/$\overline{w}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK)	–		2.5	μA
I_{TSI}	Three-State Input Leakage (DB0-DB7) V_{IN} = 0.4 to 2.4V	−10.0		+10.0	μA
V_{OH}	Output High Voltage I_{LOAD} = −205 μA (DB0-DB7) I_{LOAD} = −100 μA (all others)	2.4		–	V
V_{OL}	Output Low Voltage I_{LOAD} = 1.6mA	–		0.4	V
P_D	Power Dissipation	–	325	650	mW
C_{IN}	Input Capacitance ϕ2, R/$\overline{w}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK DB0-DB7	– –		10.0 12.5	pF pF
C_{OUT}	Output Capacitance	–		10.0	pF

TEST LOAD

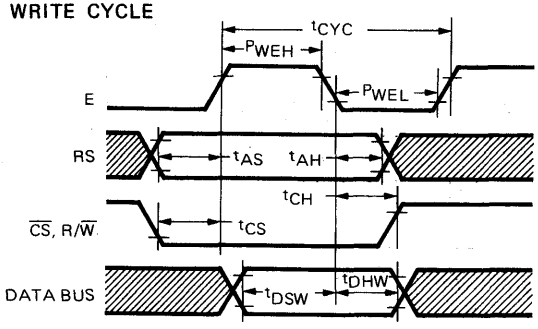


R = 11KΩ FOR DB0–DB7
R = 24KΩ FOR ALL OTHER OUTPUTS
C = 130pF TOTAL FOR DB0–DB7
C = 30 pF ALL OTHER OUTPUTS

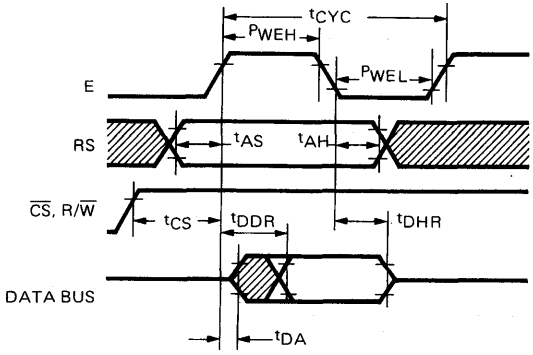
AC Characteristics

MPU BUS INTERFACE CHARACTERISTICS

WRITE CYCLE



READ CYCLE



WRITE TIMING CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = 0 – 70°C, unless otherwise noted)

Symbol	Parameter	UM6845R		UM6845RA		UM6845RB		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	–	0.5	–	0.33	–	μs
P_{WEH}	E Pulse Width, High	440	–	200	–	150	–	ns
P_{WEL}	E Pulse Width, Low	420	–	190	–	140	–	ns
t_{AS}	Address Set-Up Time	80	–	40	–	30	–	ns
t_{AH}	Address Hold Time	0	–	0	–	0	–	ns
t_{CS}	R/$\overline{W}$, $\overline{CS}$ Set-Up Time	80	–	40	–	30	–	ns
t_{CH}	R/$\overline{W}$, $\overline{CS}$ Hold Time	0	–	0	–	0	–	ns
t_{DSW}	Data Bus Set-Up Time	165	–	60	–	60	–	ns
t_{DHW}	Data Bus Hold Time	10	–	10	–	10	–	ns

(t_r and t_f = 10 to 30 ns)

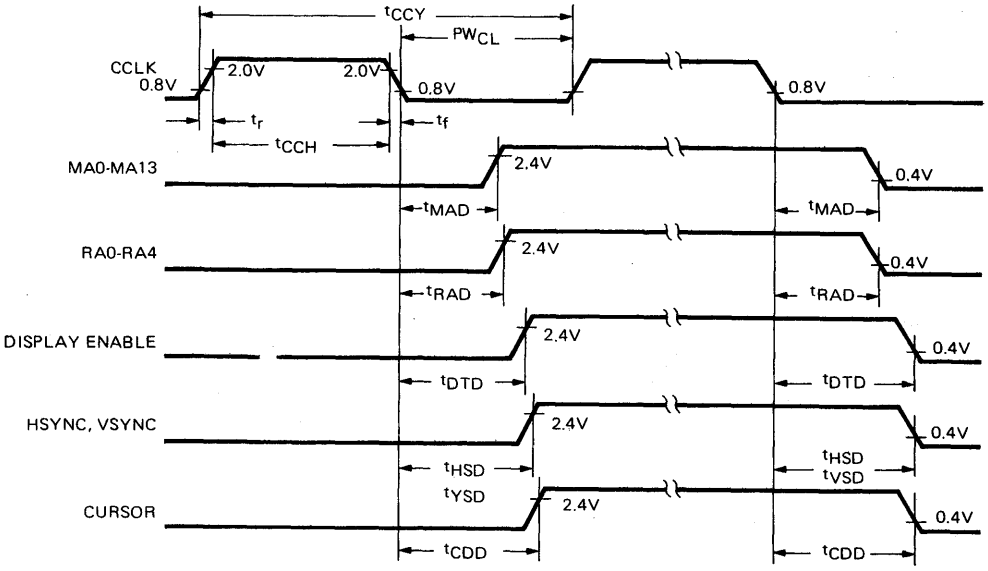
READ TIMING CHARACTERISTICS . (V_{CC} = 5.0V ± 5%, T_A = 0 – 70°C, unless otherwise noted)

Symbol	Parameter	UM6845R		UM6845RA		UM6845RB		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	–	0.5	–	0.33	–	μs
P_{WEH}	E Pulse Width, High	440	–	200	–	150	–	ns
P_{WEL}	E Pulse Width, Low	420	–	190	–	140	–	ns
t_{AS}	Address Set-Up Time	80	–	40	–	30	–	ns
t_{AH}	Address Hold Time	0	–	0	–	0	–	ns
t_{CS}	R/$\overline{W}$, $\overline{CS}$ Set-Up Time	80	–	40	–	30	–	ns
t_{DDR}	Read Access Time (Valid Data)	–	290	–	150	–	100	ns
t_{DHR}	Read Hold Time	20	60	20	60	20	60	ns
t_{DA}	Data Bus Active Time (Invalid Data)	40	–	40	–	40	–	ns

(t_r and t_f = 10 to 30 ns)

MEMORY AND VIDEO INTERFACE CHARACTERISTICS

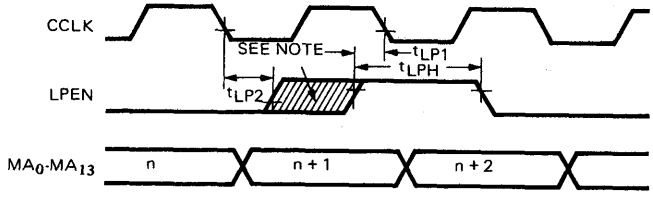
(V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)



Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{CCH}	Minimum Clock Pulse Width, High	200			ns
T_{CCY}	Clock Frequency			2.5	MHz
T_r, t_f	Rise and Fall Time for Clock Input			20	ns
t_{MAD}	Memory Address Delay Time		100	160	ns
t_{RAD}	Raster Address Delay Time		100	160	ns
t_{DTD}	Display Timing Delay Time		160	300	ns
t_{HSD}	Horizontal Sync Delay Time		160	300	ns
t_{VSD}	Vertical Sync Delay Time		160	300	ns
t_{CDD}	Cursor Display Timing Delay Time		160	300	ns

LIGHT PEN STROBE TIMING

NOTE:
"Safe" time position for LPEN positive edge to cause address n+2 to load into Light Pen Register. t_{LP2} and t_{LP1} are time positions causing uncertain results.



Symbol	Parameter	UM6845R		UM6845RA		UM6845RB		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{LPH}	LPEN Strobe Width	100	–	100	–	100	–	ns
t_{LP1}	LPEN to CCLK Delay	–	120	–	120	–	120	ns
t_{LP2}	CCLK to LPEN Delay	–	0	–	0	–	0	ns

t_r and t_f = 20 ns (max.)

Pin Description

MPU INTERFACE SIGNAL DESCRIPTION

E (Enable)
The enable signal is the system input and is used to trigger all data transfers between the system microprocessor and the UM6845R/RA/RB. Since there is no maximum limit to the allowable E cycle time, it is not necessary for it to be a continuous clock. This capability permits the UM6845R/RA/RB to be easily interfaced to non-6500-compatible microprocessors.

R/$\overline{W}$ (Read/Write)
The R/$\overline{W}$ signal is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the UM6845R/RA/RB. A low on the R/$\overline{W}$ pin allows a write to the UM6845R/RA/RB.

$\overline{CS}$ (Chip Select)
The Chip Select input is normally connected to the processor address bus either directly or through a decoder. The UM6845R/RA/RB is selected when $\overline{CS}$ is low.

RS (Register Select)
The Register Select input is used to access internal registers, A low on this pin permits writes into the Address Register and reads from the Status Register. The content of the Address Register is the identity of the register accessed when RS is high.

DB0–DB7 (Data Bus)
The DB0–DB7 pins are the eight data lines used for transfer of data between the processor and the UM6845R/RA/RB. These lines are bi-directional and are normally high-impedance except during read/write cycles when the chip is selected.

VIDEO INTERFACE SIGNAL DESCRIPTION

HSYNC (Horizontal Sync)
The HSYNC signal is an active-high output used to determine the horizontal position of displayed text. It may drive a CRT monitor directly or may be used for composite video generation. HSYNC time position and width are fully programmable.

VSYNC (Vertical Sync)
The VSYNC signal is an active-high output used to determine the vertical position of displayed text. Like HSYNC, VSYNC may be used to drive a CRT monitor or composite video generation circuits. VSYNC position and width are both fully programmable.

DISPLAY ENABLE
The DISPLAY ENABLE signal is an active-high output and is used to indicate when the UM6845R/RA/RB is generating active display information. The number of horizontal displayed characters and the number of vertical displayed characters are both fully programmable and together are used to generate the DISPLAY ENABLE signal.

CURSOR
The CURSOR signal is an active-high output and is used to indicate when the scan coincides with the programmed cursor position. The cursor position may be programmed to be any character in the address field. Furthemore, within the character, the cursor may be programmed to be any block of scan lines, since the start scan line and the end scan line are both programmable.

LPEN
The LPEN signal is an edge-sensitive input and is used to load the internal Light Pen Register with the contents of the Refresh Scan Counter at the time the active edge occurs. The active edge of LPEN is the low-to-high transition.

CCLK
The CCLK signal is the character timing clock input and is used as the time base for all internal count/control functions.

$\overline{RES}$
The $\overline{RES}$ signal is an active-low input used to initialize all internal scan counter circuits. When the $\overline{RES}$ is low, all internal counters are stopped and cleared, all scan and video outputs are low, and control registers are unaffected. The $\overline{RES}$ must stay low for at least one CCLK period. All scan timing is initiated when the $\overline{RES}$ goes high. In this way, the $\overline{RES}$ can be used to synchronize display frame timing with line frequency.

MEMORY ADDRESS SIGNAL DESCRIPTION

MA0–MA13 (Video Display RAM Address Lines)
These signals are active-high outputs and are used to address the Video Display RAM for character storage and display operations. The starting scan address is fully programmable and the ending scan address is determined by the total number of characters displayed, which is also programmable, in terms of characters/line and lines/frame.

- **Binary Addressing**
  Characters are stored in successive memory locations. Thus, the software must be developed so that row and column co-ordinates are translated to sequentially-numbered addresses for video display memory operations.

RA0-RA4 (Raster Address Lines)
These signals are active-high outputs and are used to select each raster scan within an individual character row. The number of raster scan lines is programmable and determines the character height, including spaces between character rows.

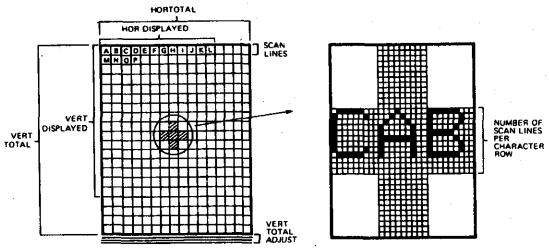


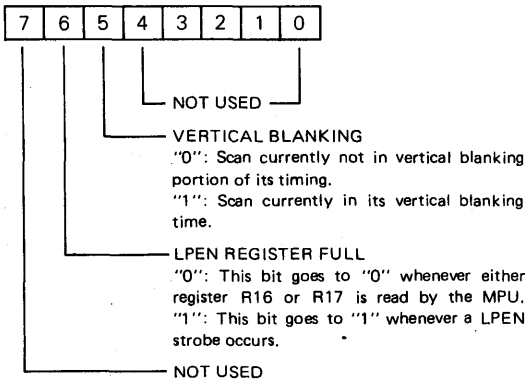
Figure 1. Video Display Format

Description of Internal Registers

Figure 1 illustrates the format of a typical video display and shows the functions of the various UM6845R/RA/RB internal registers. Figure 2 illustrates vertical and horizontal timing. Figure 3 summarizes the internal registers and indicates their address-selection and read/write capabilities.

Address Register
This is a 5-bit register which is used as a "pointer" to direct UM6845R/RA/RB data transfers to and from the system MPU using the number of the desired register (0-31). When RS is low, this register may be loaded; when RS is high, the register selected is the one whose identity is stored in this register.

Status Register
This 2-bit register is used to monitor the status of the CRTC, as follows:

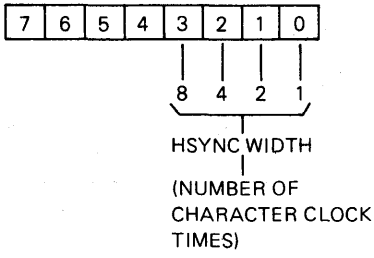


Horizontal Total (R0)
This 8-bit register contains the total of displayed and non-displayed characters, minus one, per horizontal line. The frequency of HSYNC is thus determined by this register.

Horizontal Displayed (R1)
This 8-bit register contains the number of displayed characters per horizontal line.

Horizontal Sync Position (R2)
This 8-bit register contains the position of the HSYNC on the horizontal line, in terms of the character location number on the line. The position of the HSYNC determines the left-to-right location of the displayed text on the video screen. In this way, the side margins are adjusted.

Horizontal and Vertical SYNC Widths (R3)
This 4-bit register programs the width of HSYNC.



VSYNC width is set to 16 scan line times.

Vertical Total (R4)
The Vertical Total Register is a 7-bit register containing the total number of character rows in a frame, minus one. This register, along with R5, determines the overall frame rate, which should be close to the line frequency to ensure flicker-free appearance. If the frame time is adjusted to longer than the period of the line frequency, then $\overline{RES}$ may be used to provide absolute synchronization.

Vertical Total Adjust (R5)
The Vertical Total Adjust Register is a 5-bit write-only register containing the number of additional scan lines needed to complete an entire frame scan and is intended as a fine adjustment for the video frame time.

Vertical Displayed (R6)
This 7-bit register contains the number of displayed character rows in each frame. In this way, the vertical size of the displayed text is determined.

Vertical Sync Position (R7)
This 7-bit register is used to select the character row time at which the VSYNC pulse is desired to occur and, thus, is used to position the displayed text vertically.

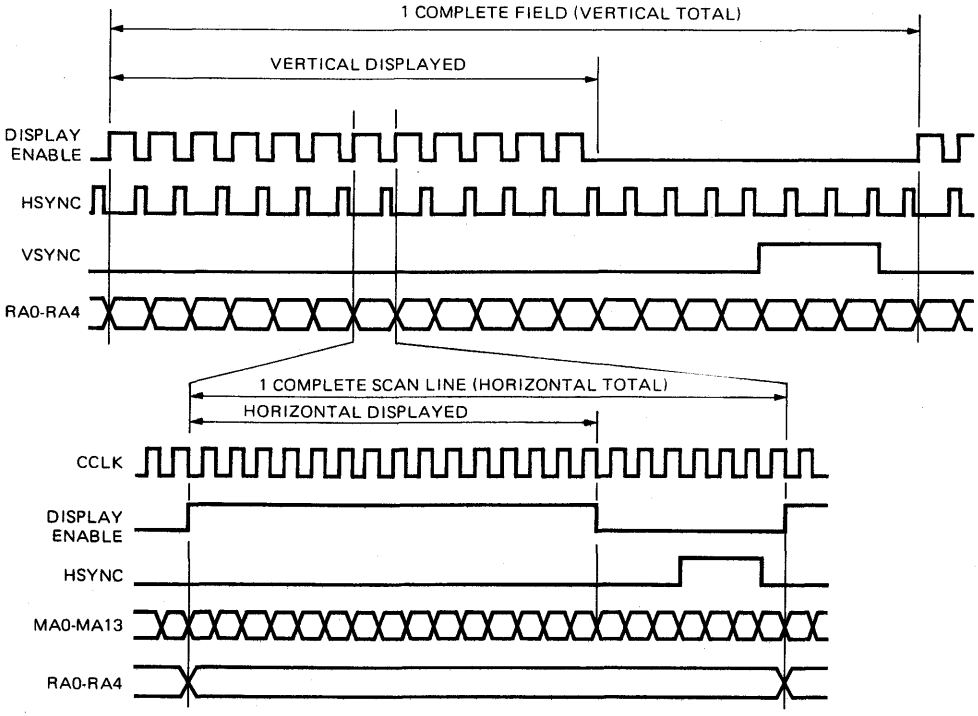
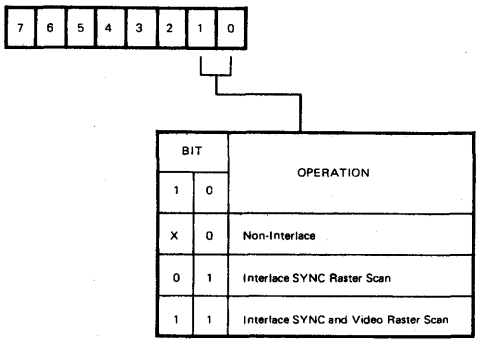


Figure 2. Vertical and Horizontal Timing

Mode Control (R8)

This register is used to select the operating modes of the UM6845R/RA/RB and is configured as follows:



Scan Line (R9)

This 5-bit register contains the number of scan lines per character row, including spacing minus one.

Cursor Start (R10) and Cursor End (R11)

These 5-bit registers select the starting and ending scan lines for the cursor. In addition, bits 5 and 6 of R10 are used to select the cursor mode, as follows:

BIT		CURSOR MODE
6	5	
0	0	No Blinking
0	1	No Cursor
1	0	Blink at 16 x field period
1	1	Blink at 32 x field period

Note that the ability to program both the start and end scan line for the cursor enables either block cursor or underline to be accommodated. Registers R14 and R15 are used to control the character position of the cursor over the entire 16K address field.

Display Start Address High (R12) and Low (R13)

These registers together comprise a 14-bit register containing the memory address of the first character of the displayed scan (the character on the top left of the video display, as in Figure 4). Subsequent memory addresses are generated by the UM6845R/RA/RB as a result of CCLK input pulses. Scrolling of the display is accomplished by changing R12 and R13 to the memory address associated with the first character of the desired line of text to be displayed first. Entire pages of text may be scrolled or changed as well via R12 and R13.

Cursor Position High (R14) and Low (R15)

These registers together comprise a 14-bit register containing the memory address of the current cursor position. When the video display scan counter (MA lines) matches the contents of this register, and when the scan line counter (RA lines) falls within the bounds set by R10 and R11, then the CURSOR output becomes active. Bit 5 of the Mode Control Register (R8) may be used to delay the CURSOR output by a full CCLK time to accommodate slow access memories.

LPEN High (R16) and Low (R17)

These registers together comprise a 14-bit register whose contents is the light pen strobe position, in terms of the video display address at which the strobe occurred. When the LPEN input changes from low to high, on the next negative-going edge of CCLK the contents of the internal scan counter are stored in registers R16 and R17.

CS	RS	Address Reg. 4	3	2	1	0	Reg. No.	Register Name	Stored Info.	RD	WR	Register Bit. 7	6	5	4	3	2	1	0
1		–	–	–	–	–	–												
0	0	–	–	–	–	–	–	Address Reg.	Reg. No.		√				A_4	A_3	A_2	A_1	A_0
0	0	–	–	–	–	–	–	Status Reg.		√			L	V					
0	1	0	0	0	0	0	R0	Horiz. Total	#Charac, -1		√	●	●	●	●	●	●	●	●
0	1	0	0	0	0	1	R1	Horiz. Displayed	#Charac.		√	●	●	●	●	●	●	●	●
0	1	0	0	0	1	0	R2	Horiz. Sync Position	#Charac.		√	●	●	●	●	●	●	●	●
0	1	0	0	0	1	1	R3	VSYNC, HSYNC Widths	#Scan Lines and #Char. Times		√					H_3	H_2	H_1	H_0
0	1	0	0	1	0	0	R4	Vert. Total	#Char. Rows -1		√		●	●	●	●	●	●	●
0	1	0	0	1	0	1	R5	Vert, Total Adjust	#Scan Lines		√				●	●	●	●	●
0	1	0	0	1	1	0	R6	Vert, Displayed	#Char. Rows		√		●	●	●	●	●	●	●
0	1	0	0	1	1	1	R7	Vert. Sync Position	#Char Rows.		√		●	●	●	●	●	●	●
0	1	0	1	0	0	0	R8	Mode Control			√							I_1	I_0
0	1	0	1	0	0	1	R9	Scan Line	#Scan Lines-1		√				●	●	●	●	●
0	1	0	1	0	1	0	R10	Cursor Start	Scan Line No.		√		B_1	B_0	●	●	●	●	●
0	1	0	1	0	1	1	R11	Cursor End	Scan Line No.		√				●	●	●	●	●
0	1	0	1	1	0	0	R12	Display Start Addr (H)			√			●	●	●	●	●	●
0	1	0	1	1	0	1	R13	Display Start Addr (L)			√	●	●	●	●	●	●	●	●
0	1	0	1	1	1	0	R14	Cursor Position (H)		√	√			●	●	●	●	●	●
0	1	0	1	1	1	1	R15	Cursor Position (L)		√	√	●	●	●	●	●	●	●	●
0	1	1	0	0	0	0	R16	Light Pen Reg (H)		√				●	●	●	●	●	●
0	1	1	0	0	0	1	R17	Light Pen Reg (L)		√		●	●	●	●	●	●	●	●

Notes: ● Designates binary bit

▨ Designates unused bit. These bits are always "0", except for $\overline{CS}$ = 1, which does not drive the data bus at all.

Figure 3. Internal Register Summary

TOTAL = 90

DISPLAY = 80

TOTAL = 34

DISPLAY = 24

0	1	2	---	---	77	78	79	80	81	---	89
80	81	82	---	---	157	158	159	160	161	---	169
160	161	162	---	---	237	238	239	240	241	---	249
⋮							⋮				⋮
⋮							⋮				⋮
⋮							⋮				⋮
1760	1761	1762	---	---	1837	1838	1839	1840	1841	---	1849
1840	1841	1842	---	---	1917	1918	1919	1920	1921	---	1929
1920	1921	1922	---	---	1997	1998	1999	2000	2001	---	2009
2000	2001	2002	---	---	2077	2078	2079	2080	2081	---	2089
⋮							⋮				⋮
2640	2641	2642	---	---	2717	2718	2719	2720	2721	---	2729

STRAIGHT BINARY ADDRESSING SEQUENCE

Figure 4. Display Address Sequences (with Starting Address = 0) for 80 x 24 Example

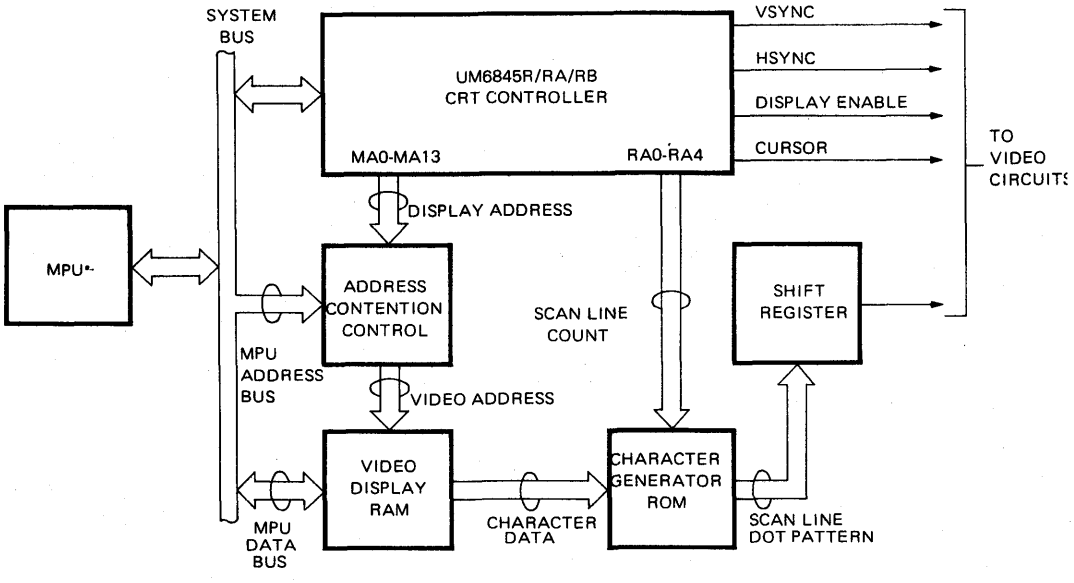


Figure 5. Shared Memory System Configuration

Memory Contention Schemes for Shared Memory Addressing

From Figure 5, it is clear that both the UM6845R/RA/RB and the system MPU must be capable of addressing the video display memory. The UM6845R/RA/RB repetitively fetches character information to generate the video signals in order to keep the screen display active. The MPU occasionally accesses the memory to change the displayed information or to read out current data characters. There are three ways of resolving this dual contention:

MPU PRIORITY

With this method, the address lines to the video display memory are normally driven by the UM6845R/RA/RB unless the MPU needs access, in which case the MPU addresses immediately override those from the UM6845R/RA/RB and the MPU has immediate access.

$\phi 1/\phi 2$ MEMORY INTERLEAVING

This method permits both the UM6845R/RA/RB and the MPU access to the video display memory by time-sharing via the system $\phi 1$ and $\phi 2$ clocks. During the $\phi 1$ portion of each cycle (the time when E is low), the UM6845R/RA/RB address outputs are gated to the video display memory. In the $\phi 2$ time, the MPU address lines are switched in. In this way, both the UM6845R/RA/RB and the MPU have periods of unimpeded access to the memory. Figure 6 illustrates the timings.

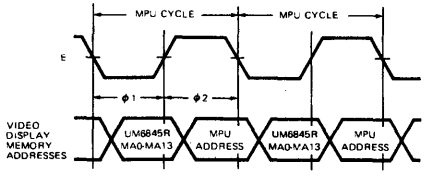


Figure 6. $\phi 1/\phi 2$ Interleaving

INTERLACED MODES

There are three raster-scan display modes (see Figure 7).

a) Non-Interlaced Mode. In this mode each scan line is refreshed at the vertical field rate (50 or 60Hz).

In the interlaced scan modes, even and odd fields alternate to generate frames. The horizontal and vertical timing relationship causes the scan lines in the odd fields to be displaced from those in the even fields. The two additional raster-scan display modes pertain to interlaced scans.

b) Interlaced Sync Mode. This mode is used when the same information is to be displayed in both odd and even fields. Enhanced readability results because the spaces between adjacent rows are filled and a higher quality character is displayed. This is achieved with only a slight alteration in the device operation: in alternate fields, the position of the VSYNC signal is delayed by ½ of a scan line time. This is illustrated in Figure 8 and is the only difference in the UM6845R/RA/RB operation in this mode.

c) Interlaced Sync and Video Mode. This mode is used to double the character density on the screen by displaying the even lines in even fields and the odd lines in odd fields. As in the Interlaced Sync mode, the VSYNC position is delayed in alternate display fields. In addition, the address generation is altered.

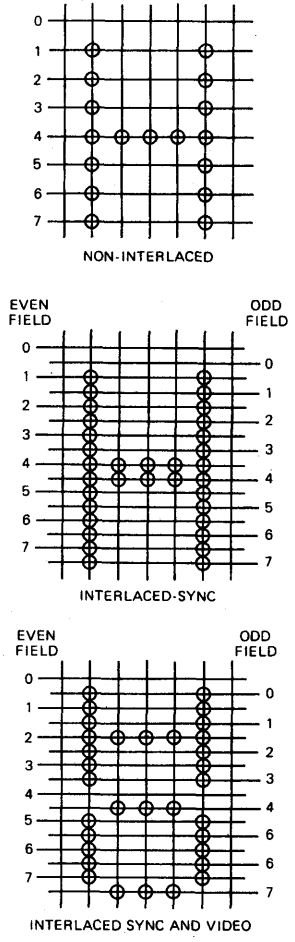


Figure 7. Comparison of Display Modes

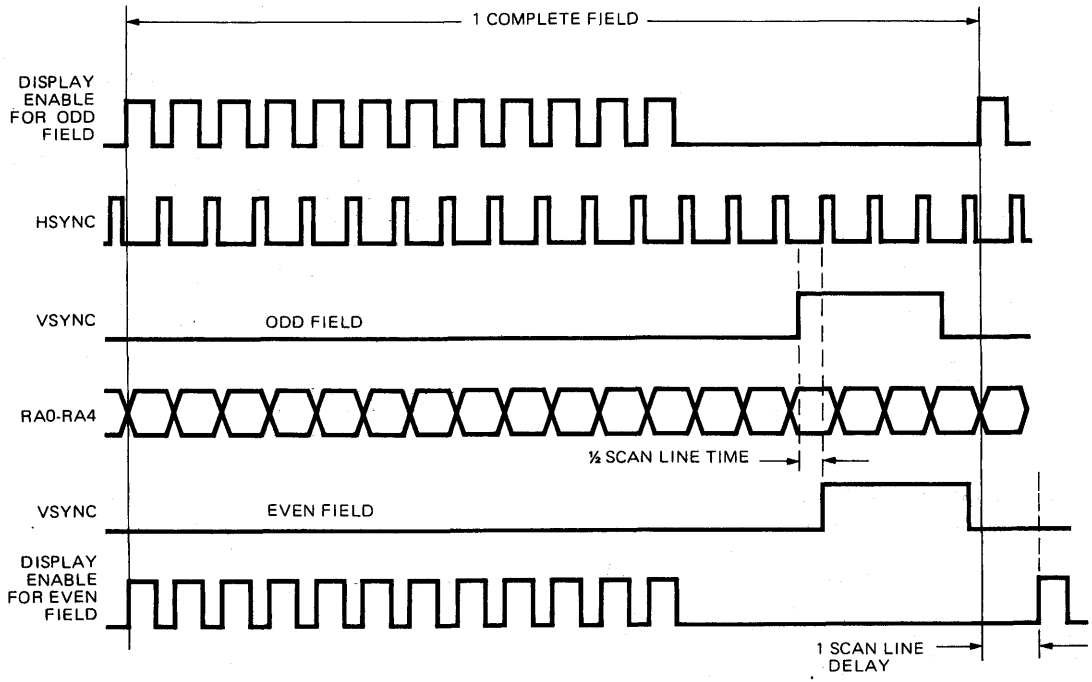


Figure 8. Interlaced Sync Mode and Interlaced Sync & Video Mode Timing

CRTC Register Comparison Table

NON-INTERLACED

Register	UM6845R/RA/RB MC6845 MC6845*1	MC6845R HD6845R	UM6845/A/B HD6845S	UM6845E/EA/EB
R0 Htotal	Total-1	Total-1	Total-1	Total-1
R1 Hdisp	Actual	Actual	Actual	Actual
R2 Hsync	Actual	Actual	Actual	Actual
R3 Sync Width	Horizontal (& Vertical *1)	Horizontal	Horizontal & Vertical	Horizontal & Vertical
R4 Vtotal	Total-1	Total-1	Total-1	Total-1
R5 Vtotal Adjustment	Any Value	Any Value	Any Value	Any Value
R6 Vdisp	Any Value <R4	Any Value <R4	Any Value <R4	Any Value <R4
R7 Vsync	Actual-1	Actual-1	Actual-1	Actual-1
R8 B0-1	Interlace	Interlace	Interlace	Interlace
Mode Select B2	–	–	–	Row/Column or Binary Addr.
B3	–	–	–	Shared or Transparent Addr.
B4	(Display Enable Skew *1)	–	Display Enable Skew	Display Enable Skew
B5	(Display Enable Skew *1)	–	Display Enable Skew	Cursor Skew
B6	(Cursor Skew *1)	–	Cursor Skew	RA4/
B7	(Cursor Skew *1)	–	Cursor Skew	Transparent
R9 Scan Lines	Total-1	Total-1	Total-1	Total-1
R10 Cursor Start	Actual	Actual	Actual	Actual
R11 Cursor End	Actual	Actual	Actual	Actual
R12/R13 Display Addr.	Write-only Read/Write (MC6845 & *1)	Read/Write	Read/Write	Write-only
R14/R15 Cursor Position	Read/Write	Read/Write	Read/Write	Read/Write
R16/R17 Position	Read-only	Read-only	Read-only	Read-only
R18/R19 Update Addr. Register	N/A	N/A	N/A	Transparent Mode Only
R31 Dummy Register	N/A	N/A	N/A	Transparent Mode Only
Status Register	Yes (UM6845R)	No	No	Yes

CRTC Register Comparison Table (Continued)

INTERLACED SYNC

Register	UM6845R/RA/RB MC6845 MC6845*1	MC6845R HD6845R	UM6845/A/B HD6845S	UM6845E/EA/EB
R0 Htotal	Total-1 = Odd or Even	Total-1 = Odd	Total-1 = Odd	Total-1 = Odd or Even

INTERLACED SYNC AND VIDEO

R4 Vtotal	Total-1	Total-1	Total-1	Total-1
R6 Vdisp	Total	Total/2	Total	Total
R7 Vsync	Actual-1	Actual-1	Actual-1	Actual-1
R9 Scan Lines	Total-1 Odd/Even	Total-1 Only Even	Total-1 Odd/Even	Total-1 Odd/Even
R10 Cursor Start	Odd/Even	Both Odd	Odd/Even	Odd/Even
R11 Cursor End	Odd/Even	Both Even	Odd/Even	Odd/Even
I_{CCLK}	2.5 MHz	2.5 MHz	3.7 MHz	3.7 MHz

Ordering Information

Part Number	CPU Clock Rate	Package
UM6845R	1 MHz	40L DIP
UM6845RA	2 MHz	40L DIP
UM6845RB	3 MHz	40L DIP

UMC

UM6845E/EA/EB

CRT Controller

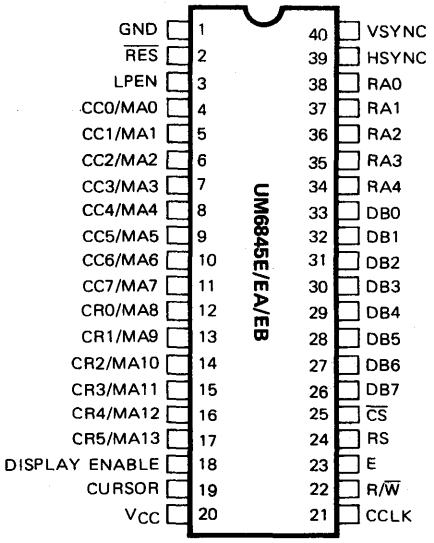
Features

- Single + 5 volt (± 5%) power supply
- Alphanumeric and limited graphics capabilities
- Fully programmable display (rows, columns, blanking, etc.).
- Interlaced or non-interlaced scan
- 50/60 Hz operation
- Fully programmable cursor
- External light pen capability
- Addressing capability up to 16K-character Video Display RAM
- No DMA required
- Pin-compatible with MC6845R
- Row/column or straight-binary addressing for Video Display RAM
- Video Display RAM configurable as part of microprocessor memory field or as independent slave to UM6845
- Internal status register
- 3.7 MHz character clock
- Transparent address mode

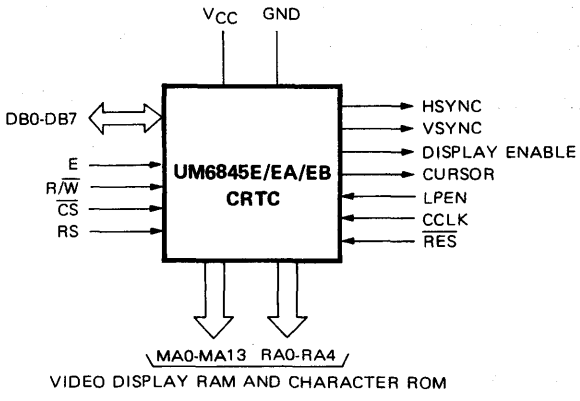
General Description

The UM6845E/EA/EB is a CRT Controller intended to provide capability for interfacing 8 or 16-bit microprocessors to CRT or TV-type raster scan displays. It's unique feature is the inclusion of several modes of operation, so that the system designer can configure the system with a wide assortment of features.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Supply Voltage, V_{CC} . . . . . −0.3V to +7.0V
Input/Output Voltage, V_{IN} . . . . . −0.3V to +7.0V
Operating Temperature, T_{OP} . . . . . 0°C to 70°C
Storage Temperature, T_{STG} . . . . . −55°C to 150°C

All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

*Comments

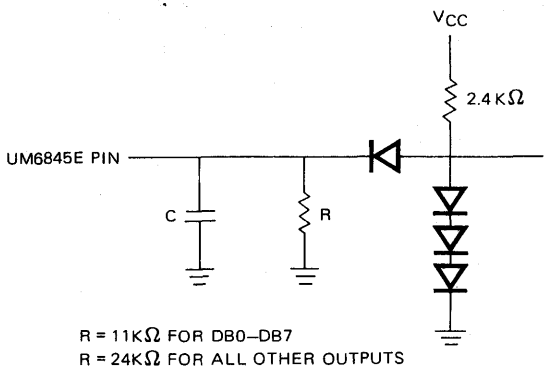
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(V_{CC} = 5.0V ± 5%, T_A = 0 − 70°C, unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage	2.0		V_{CC}	V
V_{IL}	Input Low Voltage	−0.3		0.8	V
I_{IN}	Input Leakage (ϕ2, R/W, RES, CS, RS, LPEN, CCLK)	−		2.5	μA
I_{TSI}	Three-State Input Leakage (DB0-DB7) V_{IN} = 0.4 to 2.4V	−10.0		+10.0	μA
V_{OH}	Output High Voltage I_{LOAD} = −205μA (DB0-DB7) I_{LOAD} = −100μA (all others)	2.4		−	V
V_{OL}	Output Low Voltage I_{LOAD} = 1.6mA	−		0.4	V
P_D	Power Dissipation	−	325	650	mW
C_{IN}	Input Capacitance ϕ2, R/W, RES, CS, RS, LPEN, CCLK DB0-DB7	 − −		 10.0 12.5	 pF pF
C_{OUT}	Output Capacitance	−		10.0	pF

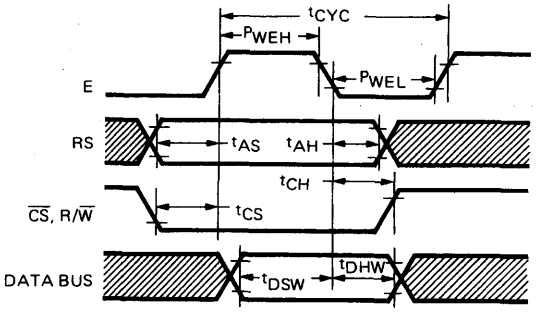
Test Load



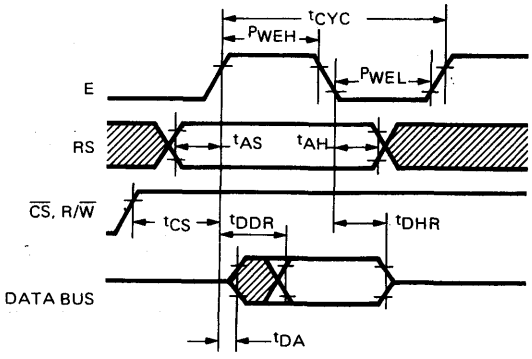
R = 11KΩ FOR DB0–DB7
R = 24KΩ FOR ALL OTHER OUTPUTS
C = 130pF TOTAL FOR DB0–DB7
C = 30pF ALL OTHER OUTPUTS

MPU Bus Interface Characteristics

WRITE CYCLE



READ CYCLE



Write Timing Characteristics (V_{CC} = 5.0V ± 5%, T_A = 0 – 70°C, unless otherwise noted)

Symbol	Parameter	UM6845E		UM6845EA		UM6845EB		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	–	0.5	–	0.33	–	μs
P_{WEH}	E Pulse Width, High	440	–	200	–	150	–	ns
P_{WEL}	E Pulse Width, Low	420	–	190	–	140	–	ns
t_{AS}	Address Set-Up Time	80	–	40	–	30	–	ns
t_{AH}	Address Hold Time	0	–	0	–	0	–	ns
t_{CS}	R/W, CS Set-Up Time	80	–	40	–	30	–	ns
t_{CH}	R/W, CS Hold Time	0	–	0	–	0	–	ns
t_{DSW}	Data Bus Set-Up Time	165	–	60	–	60	–	ns
t_{DHW}	Data Bus Hold Time	10	–	10	–	10	–	ns

(t_r and t_f = 10 to 30 ns)

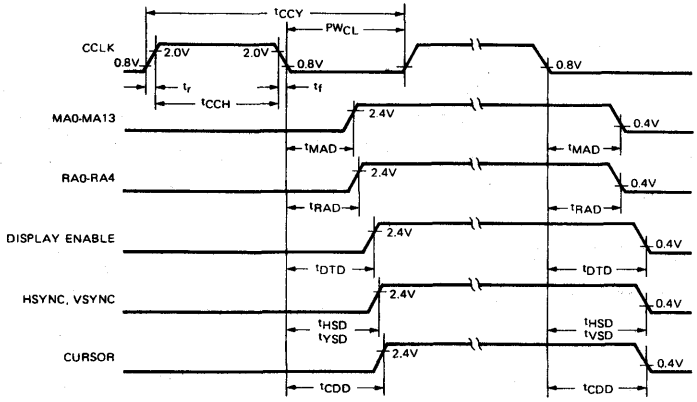
Read Timing Characteristics (V_{CC} = 5.0V ± 5%, T_A = 0 – 70°C, unless otherwise noted)

Symbol	Parameter	UM6845E		UM6845EA		UM6845EB		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	–	0.5	–	0.33	–	μs
P_{WEH}	ϕ_2 Pulse Width, High	440	–	200	–	150	–	ns
P_{WEL}	ϕ_2 Pulse Width, Low	420	–	190	–	140	–	ns
t_{AS}	Address Set-Up Time	80	–	40	–	30	–	ns
t_{AH}	Address Hold Time	0	–	0	–	0	–	ns
t_{CS}	R/W, CS Set-Up Time	80	–	40	–	30	–	ns
t_{DDR}	Read Access Time (Valid Data)	–	290	–	150	–	100	ns
t_{DHR}	Read Hold Time	10	–	10	–	10	60	ns
t_{DA}	Data Bus Active Time (Invalid Data)	20	60	20	60	20	60	ns
t_{TAD}	MA0-MA13 Switching Delay (Refer to Figure Trans. Addressing)	100 typ.	160	100 typ.	160	90 typ.	130	ns

(t_r and t_f = 10 to 30 ns)

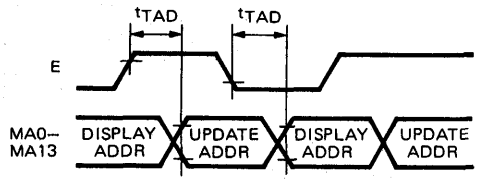
Memory and Video Interface Characteristics

(V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)

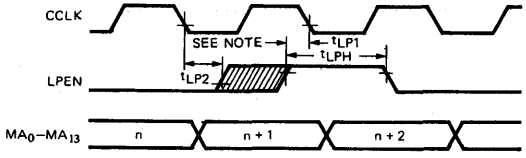


Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{CCH}	Minimum Clock Pulse Width, High	130			ns
t_{CCV}	Clock Frequency			3.7	MHz
t_r, t_f	Rise and Fall Time for Clock Input			20	ns
t_{MAD}	Memory Address Delay Time		100	160	ns
t_{RAD}	Raster Address Delay Time		100	160	ns
t_{DTD}	Display Timing Delay Time		160	250	ns
t_{HSD}	Horizontal Sync Delay Time		160	250	ns
t_{VSD}	Vertical Sync Delay Time		160	250	ns
t_{CDD}	Cursor Display Timing Delay Time		160	250	ns

Transparent Addressing (ϕ1/ϕ2 Interleaving)



Light Pen Strobe Timing



Note: "Safe" time position for LPEN positive edge to cause address n + 2 to load into Light Pen Register. t_{LP2} and t_{LP1} are time positions causing uncertain results.

Symbol	Parameter	UM6845E		UM6845EA		UM6845EB		Unit
		Min.	max.	Min.	Max.	Min.	Max.	
t_{LPH}	LPEN Strobe Width	100	–	100	–	100	–	ns
t_{LP1}	LPEN to CCLK Delay	–	120	–	120	–	120	ns
t_{LP2}	CCLK to LPEN Delay	–	0	–	0	–	0	ns

t_r and t_f = 20 ns (max.)

MPU Interface Signal Description

E (Enable)

The enable signal is the system input and is used to trigger all data transfers between the system microprocessor and the UM6845E/EA/EB. Since there is no maximum limit to the allowable E cycle time, it is not necessary for it to be a continuous clock. This capability permits the UM6845E/EA/EB to be easily interfaced to non-6500-compatible microprocessors.

R/$\overline{W}$ (Read/Write)

The R/$\overline{W}$ signal is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the UM6845E/EA/EB; a low on the R/$\overline{W}$ pin allows a write to the UM6845E/EA/EB.

$\overline{CS}$ (Chip Select)

The Chip Select input is normally connected to the processor address bus either directly or through a decoder. The UM6845E/EA/EB is selected when $\overline{CS}$ is low.

RS (Register Select)

The Register Select input is used to access internal registers. A low on this pin permits writing into the Address Register and reads from the Status Register. The Address Register contains the identity of the register accessed when RS is high.

DB0-DB7 (Data Bus)

The DB0-DB7 pins are the eight data lines used for transfer of data between the processor and the UM6845E/EA/EB. These lines are bi-directional and are normally high-impedance except during read/write cycles when the chip is selected.

Video Interface Signal Description

HSYNC (Horizontal Sync)

The HSYNC signal is an active-high output used to determine the horizontal position of displayed text. It may drive a CRT monitor directly or may be used for composite video generation. HSYNC time position and width are fully programmable.

VSYNC (Vertical Sync)

The VSYNC signal is an active-high output used to determine the vertical position of displayed text. Like HSYNC, VSYNC may be used to drive a CRT monitor or composite video generation circuits. VSYNC position and width are both fully programmable.

DISPLAY ENABLE

The DISPLAY ENABLE signal is an active-high output and is used to indicate when the UM6845E/EA/EB is generating active display information. The number of horizontally displayed characters and the number of vertically displayed characters are both fully programmable and together are used to generate the DISPLAY ENABLE signal. DISPLAY ENABLE may be delayed by one character time by setting bit 4 of R8 to a "1".

CURSOR

The CURSOR signal is an active-high output and is used to indicate when the scan coincides with the programmed cursor position. The cursor position may be programmed to be any character in the address field. Furthermore, within the character, the cursor may be programmed to be any block of scan lines, since the start scan line and the end scan line are both programmable. The CURSOR position may be delayed by one character time by setting bit 5 of R8 to a "1".

LPEN

The LPEN signal is an edge-sensitive input and is used to load the internal Light Pen Register with the contents of the Refresh Scan Counter at the time the active edge occurs. The active edge of LPEN is the low-to-high transition.

CCLK

The CCLK signal is the character timing clock input and is used as the time base for all internal count/control functions.

$\overline{RES}$

The $\overline{RES}$ signal is an active-low input used to initialize all internal scan counter circuits. When $\overline{RES}$ is low, all internal counters are stopped and cleared, all scan and video outputs are low, and control registers are unaffected. $\overline{RES}$ must stay low for at least one CCLK period. All scan timing is initiated when $\overline{RES}$ goes high. In this way, $\overline{RES}$ can be used to synchronize display frame timing with line frequency.

Memory Address Signal Description

MA0-MA13 (Video Display RAM Address Lines)

These signals are active-high outputs and are used to address the Video Display RAM for character storage and display operations. The starting scan address is fully programmable and the ending scan address is determined by the total number of characters displayed, which is also programmable, in terms of characters/line and lines/frame.

There are two selectable address modes for MA0-13:

- Binary
  Characters are stored in successive memory locations. Thus, the software must be developed so that row and column co-ordinates are translated to sequentially numbered addresses for video display memory operations.
- Row/Column
  In this mode, MA0-7 functions as the column addresses CC0-7, and MA8-13, as row addresses CR0-CR5. In this case, the software may handle addresses in terms of row and column locations, but additional address compression circuits are needed to convert CC0-7 and CR0-5 into a memory-efficient binary scheme.

RA0-RA4 (Raster Address Lines)

These signals are active-high outputs and are used to select each raster scan within an individual character row. The number of raster scan lines is programmable and determines the character height, including spaces between character rows.

The high-order line, RA4, is unique in that it can also function as a strobe output pin when the UM6845E/EA/EB is programmed to operate in the "Transparent Address Mode". In this case the strobe is an active-high output and is true at the time the Video Display RAM update address is gated on to the address lines, MA0-MA13. In this way, updates and readouts of the Video Display RAM can be made under control of the UM6845E/EA/EB with only a small amount of external circuitry.

Description of Internal Registers

Figure 1 illustrates the format of a typical video display and shows the functions of the various UM6845E/EA/EB internal registers. Figure 2 illustrates vertical and horizontal timing. Figure 3 summarizes the internal registers and indicates their address selection and read/write capabilities.

Address Register

This is a 5-bit register which is used as a "pointer" to direct UM6845E/EA/EB data transfers to and from the system MPU. Its contains the number of the desired register (0-31). When RS is low, then this register may be loaded; when RS is high, then the register selected is the one whose identity is stored in this register.

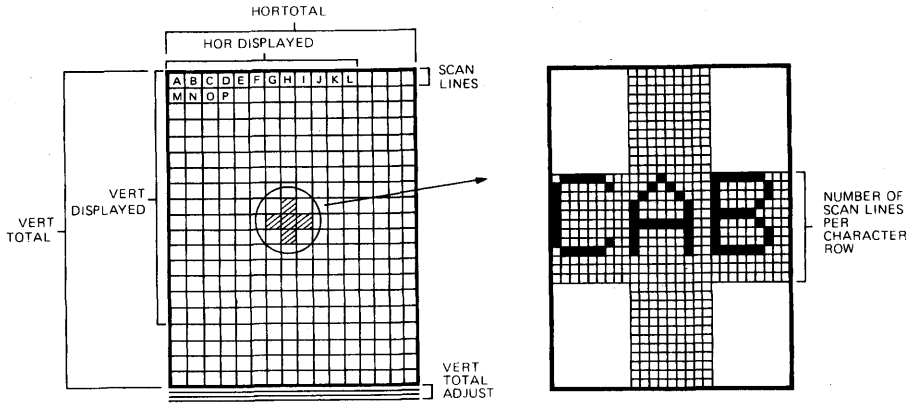
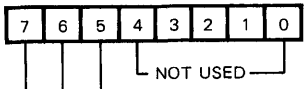


Figure 1. Video Display Format

Status Register

This 3-bit register is used to monitor the status of the CRTC, as follows:



NOT USED

VERTICAL BLANKING
"0": Scan is not currently in vertical blanking portion of its timing
"1": Scan currently is in its vertical blanking time.

LPEN REGISTER FULL
"9": This bit goes to "0" whenever either register R16 or R17 is read by the MPU.
"1": This bit goes to "1" whenever a LPEN strobe occurs.

UPDATE READY
"0": This bit goes to "0" when register R31 has been either read or written by the MPU.
"1": This bit goes to "1" when an Update Strobe occurs.

Horizontal Total (R0)

This 8-bit register contains the total of displayed and non-displayed characters, minus one, per horizontal line. The frequency of HSYNC is thus determined by this register.

Horizontal Display (R1)

This 8-bit register contains the number of displayed characters per horizontal line.

Horizontal Sync Position (R2)

This 8-bit register contains the position of the HSYNC on the horizontal line, in terms of the character location number on the line. The position of the HSYNC determines the left-to-right location of the displayed text on the video screen. In this way, the side margins are adjusted.

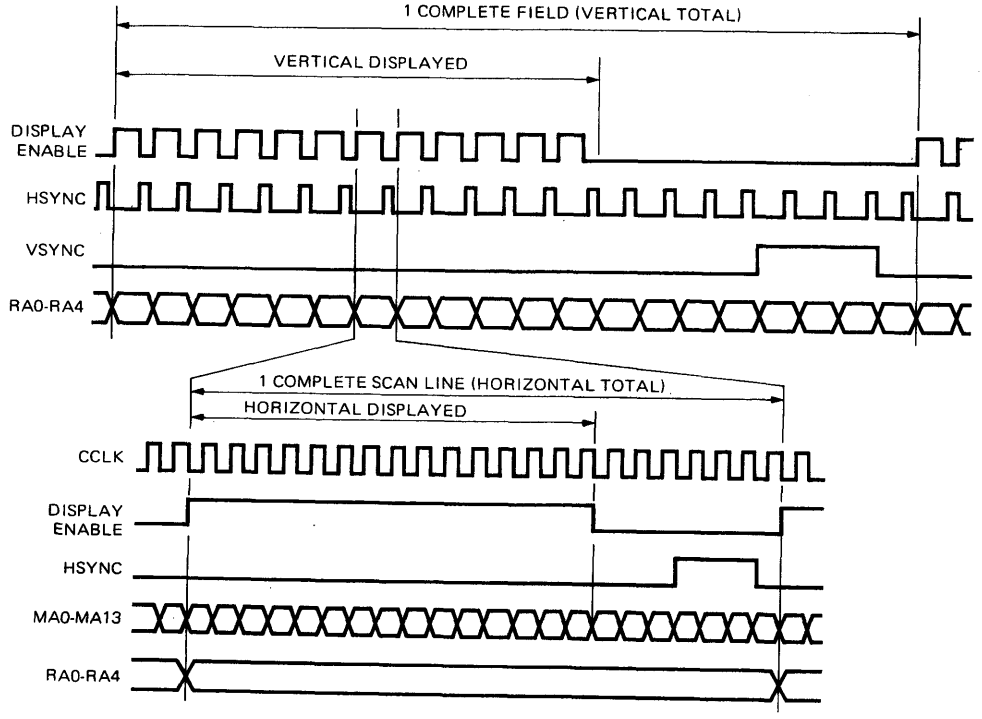
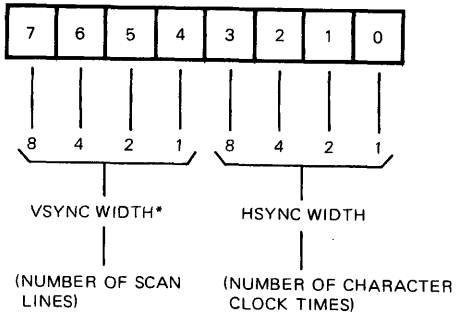


Figure 2. Vertical and Horizontal Timing

Horizontal and Vertical SYNC Widths (R3)

This 8-bit register contains the widths of both HSYNC and VSYNC, as follows:



*IF BITS 4-7 ARE ALL "0", THEN VSYNC WILL BE 16 SCAN LINES WIDE.

Control of these parameters allows the UM6845E/EA/EB to be interfaced to a variety of CRT monitors, since the HSYNC and VSYNC timing signals may be accommodated without the use of external one-shot timing.

Vertical Total (R4)

The Vertical Total Register is a 7-bit register containing the total number of character rows in a frame, minus one. This register, along with R5, determines the overall frame rate, which should be close to the line frequency to ensure flicker-free appearance. If the frame time is adjusted to be longer than the period of the line frequency, then $\overline{RES}$ may be used to provide absolute synchronization.

Vertical Total Adjust (R5)

The Vertical Total Adjust Register is a 5-bit write-only register containing the number of additional scan lines needed to complete an entire frame scan and is intended as a fine adjustment for the video frame time.

Vertical Displayed (R6)

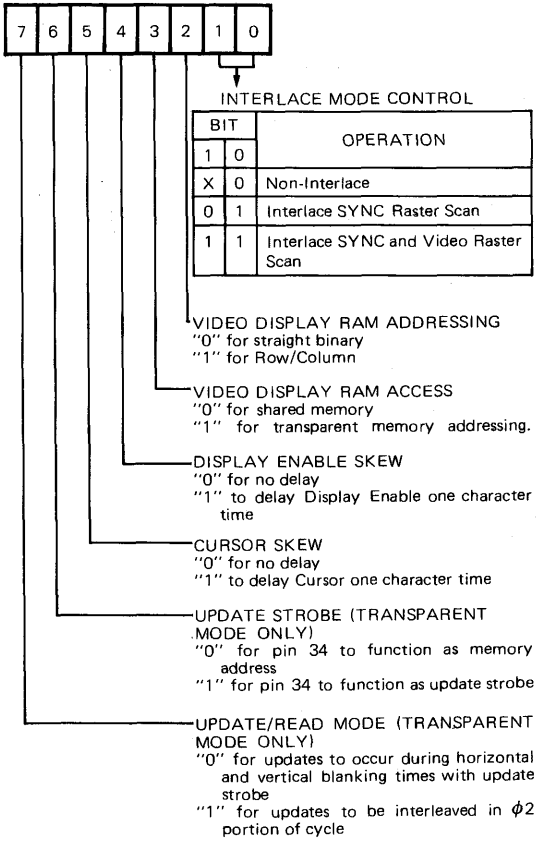
This 7-bit register contains the number of displayed character rows in each frame. In this way, the vertical size of the displayed text is determined.

Vertical Sync Position (R7)

This 7-bit register is used to select the character row time for the VSYNC pulse and thus is used to position the displayed text in the vertical direction

Mode Control (R8)

This register is used to select the operating modes of the UM6845E/EA/EB and is outlined as follows:



Scan Line (R9)

This 5-bit register contains the number of scan lines per character row, including spacing, minus one.

Cursor Start (R10) and Cursor End (R11)

These 5-bit registers select the starting and ending scan lines for the cursor. In addition, bits 5 and 6 of R 10 are used to select the cursor mode, as follows:

BIT 6	BIT 5	Cursor Mode
0	0	No Blinking
0	1	No Cursor
1	0	Blink at 16 x field period
1	1	Blink at 32 x field period

Note that the ability to program both the start and end scan line for the cursor enables either block cursor or underlined. Registers R14 and R15 are used to control the character position of the cursor over the entire 16K address field.

Display Start Address High (R12) and Low (R13)

These registers together comprise a 14-bit register containing the memory address of the first character of the displayed scan (the character on the top left of the video display, as in Figure 1). Subsequent memory addresses are generated by the UM6845E/EA/EB as a result of CCLK input pulses. Scrolling of the display is accomplished by changing R12 and R13 to the memory address associated with the first character of the desired line of text to be displayed first. Entire pages of text may be scrolled or changed as well via R12 and R13.

Cursor Position High (R14) and Low (R15)

These registers together comprise a 14-bit register containing the memory address of the current cursor position. When the video display scan counter (MA lines) matches the contents of this register, and when the scan line counter (RA lines) falls within the bounds set by R10 and R11, then the CURSOR output becomes active. Bit 5 of the Mode Control Register (R8) may be used to delay the CURSOR output by a full CCLK time to accommodate slow access memories.

LPEN High (R16) and Low (R17)

These registers together comprise a 14-bit register containing the light pen strobe position, in terms of the video display address at which the strobe occurred. When the LPEN input changes from low to high, on the next negative-going edge of CCLK the contents of the internal scan counter are stored in registers R16 and R17.

Update Address High (R18) and Low (R19)

These registers together comprise a 14-bit register containing the memory address at which the next read or update will occur (for transparent address mode only). Whenever a read/update occurs, the update location automatically increments to allow for fast updates or readouts of consecutive character locations. This is described elsewhere in this document.

Dummy Location (R31)

This register does not store any data, but is required to detect when transparent addressing updates occur. This is necessary to increment the Update Address Register and to set the Update Ready bit in the status register.

Description of Operation

Register Formats

Register pairs R12/R13, R14/R15, R16/R17, and R18/R19 are formatted in one of two ways:

1. Straight binary if register R8, bit 2 is a "0".
2. Row/Column if register R8, bit 2 is a "1". In this

case the low byte is the Character Column and the high byte is the Character Row.

Figure 4 illustrates the address sequence for the video display control for each mode.

Note from Figure 4 that the straight-binary mode has the advantage that all display memory addresses are stored in a continuous memory block, starting with address 0 and ending at 1919. The disadvantage of this method is that, if it is desired to change a displayed character location, the row and column identity of the location must be converted to a binary address before the memory may be written. The row/column mode, on the other hand, does not need to undergo this conversion. However, memory is not used as efficiently, since the memory addresses are not continuous, but gaps exist. This requires that the system be equipped with more memory than is actually used and this extra memory is wasted. Alternatively, address compression logic may be employed to translate the row/column format into a continuous address block. In this way, the user may select whichever mode is best for the given application. The trade-offs between the modes are in software and hardware needs. Straight-binary mode minimizes hardware requirements and row/column requires minimum software.

Video Display RAM Addressing

There are two modes of addressing for the video display memory:

1. Shared Memory

   In this mode the memory is shared between the MPU address bus and the UM6845E/EA/EB address bus. In this case, memory contention must be resolved by means of external timing and control circuits. Both the MPU and the UM6845E/EA/EB must have access to the video display RAM and the contention circuits must resolve this multiple access requirement. Figure 5 illustrates the system configuration.

$\overline{CS}$	RS	Address Reg. 4	3	2	1		Reg. No.	Register Name	Stored Info.	RD	WR	Register Bit 7	6	5	4	3	2	1	0
1		–	–	–	–	–	–												
0	0	–	–	–	–	–	–	Address Reg	Reg. No.		√				A_4	A_3	A_2	A_1	A_0
0	0	–	–	–	–	–	–	Status Reg		√		U	L	V					
0	1	0	0	0	0	0	R0	Horiz, Total	#Charac, – 1		√	•	•	•	•	•	•	•	•
0	1	0	0	0	0	1	R1	Horiz, Displayed	#Charac.		√	•	•	•	•	•	•	•	•
0	1	0	0	0	1	0	R2	Horiz, Sync Position	#Charac.		√	•	•	•	•	•	•	•	•
0	1	0	0	0	1	1	R3	VSYNC, HSYNC Widths	#Scan Lines and #Char, Times		√	V_3	V_2	V_1	V_0	H_3	H_2	H_1	H_0
0	1	0	0	1	0	0	R4	Vert, Total	#Charac, Row – 1		√		•	•	•	•	•	•	•
0	1	0	0	1	0	1	R5	Vert, Total Adjust	#Scan Lines		√				•	•	•	•	•
0	1	0	0	1	1	0	R6	Vert, Displayed	#Charac, Rows		√		•	•	•	•	•	•	•
0	1	0	0	1	1	1	R7	Vert, Sync Position	#Charac, Rows		√		•	•	•	•	•	•	•
0	1	0	1	0	0	0	R8	Mode Control			√	U_1	U_0	C	D	T	RC	I_1	I_0
0	1	0	1	0	0	1	R9	Scan Line	#Scan Lines–1		√				•	•	•	•	•
0	1	0	1	0	1	0	R10	Cursor Start	Scan Line No.		√		B_1	B_0	•	•	•	•	•
0	1	0	1	0	1	1	R11	Cursor End	Scan Line No.		√				•	•	•	•	•
0	1	0	1	1	0	0	R12	Display Start Addr (H)	Row		√			•	•	•	•	•	•
0	1	0	1	1	0	1	R13	Display Start Addr (L)	Col		√	•	•	•	•	•	•	•	•
0	1	0	1	1	1	0	R14	Cursor Position (H)	Row	√	√			•	•	•	•	•	•
0	1	0	1	1	1	1	E15	Cursor Position (L)	Col	√		•	•	•	•	•	•	•	•
0	1	1	0	0	0	0	R16	Light Pen Reg (H)		√				•	•	•	•	•	•
0	1	1	0	0	0	1	R17	Light Pen Reg (L)		√		•	•	•	•	•	•	•	•
0	1	1	0	0	1	0	R18	Update Location (H)			√			•	•	•	•	•	•
0	1	1	0	0	1	1	R19	Update Location (L)			√	•	•	•	•	•	•	•	•
0	1	1	1	1	1	1	R31	Dummy Location											

Notes: [•] Designates binary bit

[▨] Designates unused bit, Reading this bit is always "0", except for R31, which does not drive the data bus at all, and for CS = "1" which operates likewise.

Figure 3. Internal Register Summary

Straight Binary Addressing Sequence

TOTAL = 90

DISPLAY = 80

TOTAL = 34

DISPLAY = 24

0	1	2	---	---	77	78	79	80	81	---	89
80	81	82	---	---	157	158	159	160	161	---	169
160	161	162	---	---	237	238	239	240	241	---	249
⋮							⋮				⋮
1760	1761	1762	---	---	1837	1838	1839	1840	1841	---	1849
1840	1841	1842	---	---	1917	1918	1919	1920	1921	---	1929
1920	1921	1922	---	---	1997	1998	1999	2000	2001	---	2009
2000	2001	2002	---	---	2077	2078	2079	2080	2081	---	2089
⋮							⋮				⋮
2640	2641	2642	---	---	2217	2718	2719	2720	2721	---	2729

Row/Column Addressing Sequence

TOTAL = 90

DISPLAY = 80

COLUMN ADDRESS (MA0-MA7)

TOTAL = 34

DISPLAY = 24

ROW ADDRESS (MA8-MA13)

	0	1	2			77	78	79	80	81		89
0	0	1	2	---	---	77	78	79	80	81	---	89
1	256	257	258	---	---	333	334	335	336	337	---	345
2	512	513	514	---	---	589	590	591	592	593	---	601
	⋮							⋮				⋮
21	⋮							⋮				⋮
22	5632	5633	5634	---	---	5709	5710	5711	5712	5713	---	5721
23	5888	5889	5890	---	---	5965	5966	5697	5968	5969	---	5977
24	6144	6145	6146	---	---	6221	6222	6223	6224	6225	---	6233
25	6400	6401	6402	---	---	6477	6478	6479	6480	6481	---	6489
	⋮							⋮				⋮
33	8448	8449	8450	---	---	8525	8526	8527	8528	8529	---	8537

Figure 4. Display Address Sequences (with Start Address = 0) for 80 x 24 Example

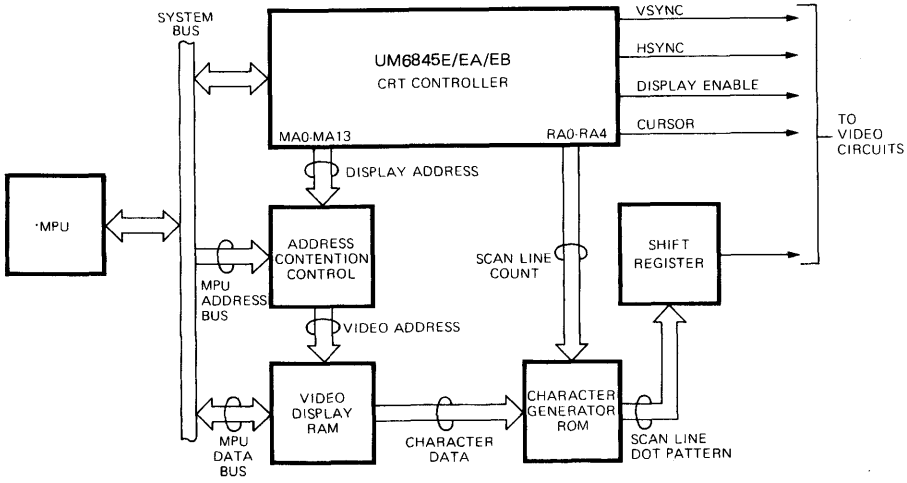


Figure 5. Shared Memory System Configuration

2. Transparent Memory Addressing.

For this mode, the display RAM is not directly accessible by the MPU, but is controlled entirely by the UM6845E/EA/EB. All MPU accesses are made via the UM6845E/EA/EB and a small amount of external circuits. Figure 6 shows the system configuration for this approach.

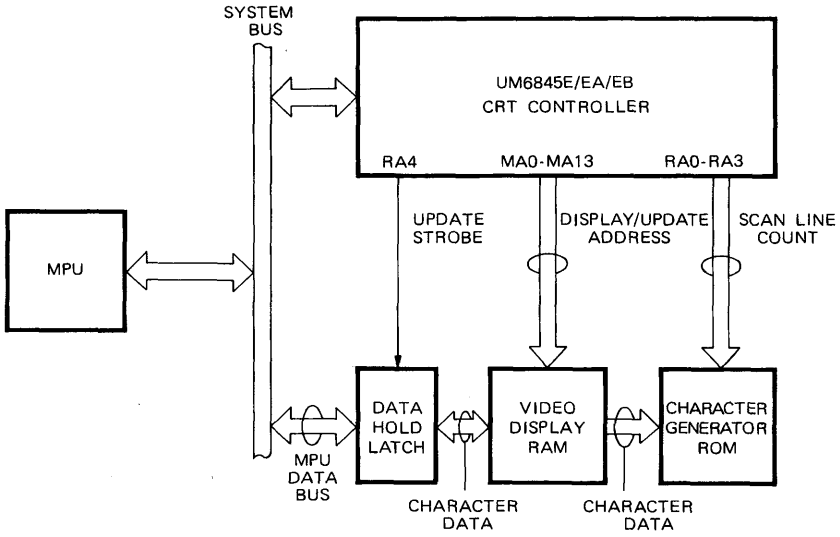


Figure 6. Transparent Memory Addressing System Configuration (Data Hold Latch needed for Horizontal/Vertical Blanking updates only).

Memory Contention Schemes for Shared Memory Addressing

From Figure 5 it is clear that both the UM6845E/EA/EB and the system MPU must be capable of addressing the video display memory. The UM6845E/EA/EB repetitively fetches character information to generate the video signals in order to keep the screen display active. The MPU occasionally accesses the memory to change the displayed information or to read out current data characters. Three ways of resolving this dual contention requirement are apparent:

- **MPU Priority**

  In this technique, the address lines to the video display memory are normally driven by the UM6845E/EA/EB unless the MPU needs access, in which case the MPU addresses immediately over-ride those from the UM6845E/EA/EB and the MPU has immediate access.

- **$\phi 1/\phi 2$ Memory Interleaving**

  This method gives both the UM6845E/EA/EB and the MPU access to the video display memory by time-sharing via the system $\phi 1$ and $\phi 2$ clocks. During the $\phi 1$ portion of each cycle (the time when E is low), the UM6845E/EA/EB address outputs are gated to the video display memory. In the $\phi 2$ time, the MPU address lines are switched in. In this way, both the UM6845E/EA/EB and the MPU have unimpeded access to the memory. Figure 7 illustrates the timings.

- **Vertical Blanking**

  With this approach, the address circuitry is identical to the case for MPU Priority updates. The only difference is that the Vertical Retrace status bit (bit 5 of the Status Register) is used by the MPU so that access to the video display memory is only made during vertical blanking time (when bit 5 is a "1"). In this way, no visible screen perturbations result.

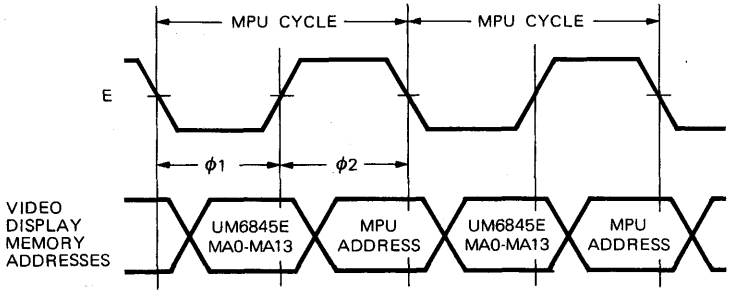


Figure 7. φ1/φ2 Interleaving

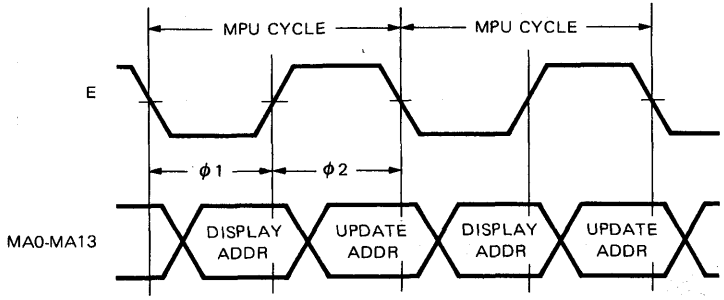


Figure 8. φ1/φ2 Transparent Interleaving

Transparent Memory Addressing

In this mode of operation, the video display memory address lines are not switched by contention circuits, but are generated by the UM6845E/EA/EB. In effect, the contention is handled by the UM6845E/EA/EB. As a result, the schemes for accessing MPU memory are different:

- **φ1/φ2 Interleaving**

  This mode is similar to the Interleave mode used with shared memory. In this case, however, the φ2 address is generated from the Update Address Register (Registers R18 and R19) in the UM6845E/EA/EB. Thus, the MPU must first load the address to be accessed into R18/R19. This address is then always gated onto the MA lines during φ2. Figure 8 shows the timing.

- **Horizontal/Vertical Blanking**

  In this mode, the Update Address is loaded by the MPU, but is only gated onto the MA lines during horizontal or vertical blank times, so memory accesses do not interfere with the display appearance. To signal when the update address is on the MA lines, an update strobe (STR) is provided as an alternate function of pin 34. Data hold latches are necessary to temporarily retain the character to be stored until the retrace time occurs. In this way, the system MPU is not halted waiting for the blanking time to arrive. Figure 9 illustrates the address and strobe timing for this mode.

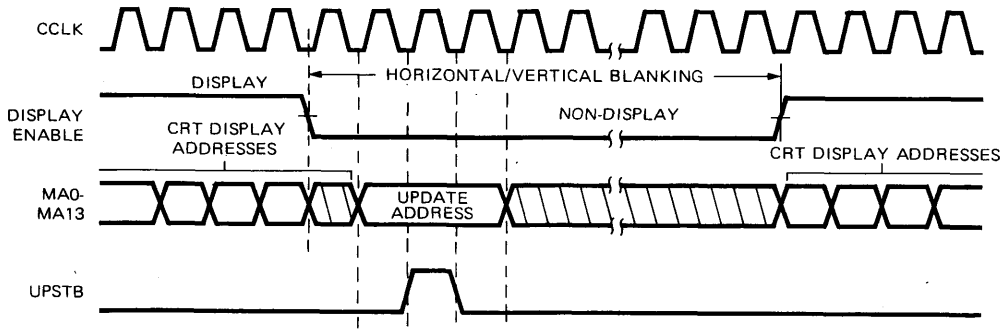


Figure 9. Retrace Update Timings

Interlaced Modes

There are three raster-scan display modes (see Figure 10).

a) Non-Interlaced Mode

In this mode each scan line is refreshed at the vertical field rate (50 or 60 Hz).

In the interlaced scan modes, even and odd fields alternate to generate frames. The horizontal and vertical timing relationship causes the scan lines in the odd fields to be displaced from those in the even fields. The two additional raster-scan display modes pertain to interlaced scans.

b) Interlaced Sync Mode

This mode is used when the same information is to be displayed in both odd and even fields. Enhanced readability results because the spaces between adjacent rows are filled and a higher quality character is displayed. This is achieved with only a slight alteration in device operation: in alternate fields, the position of the VSYNC signal is delayed by ½ of a scan line time. This is illustrated in Figure 11, and is the only deviance of UM6845E/EA/EB operation in this mode.

c) Interlaced Sync and Video Mode

This mode is used to double the character density on the screen by displaying the even lines in even fields and the odd lines in odd fields. As in the Interlaced-Sync mode, the VSYNC position is delayed in alternate display fields. In addition, the address generation is altered.

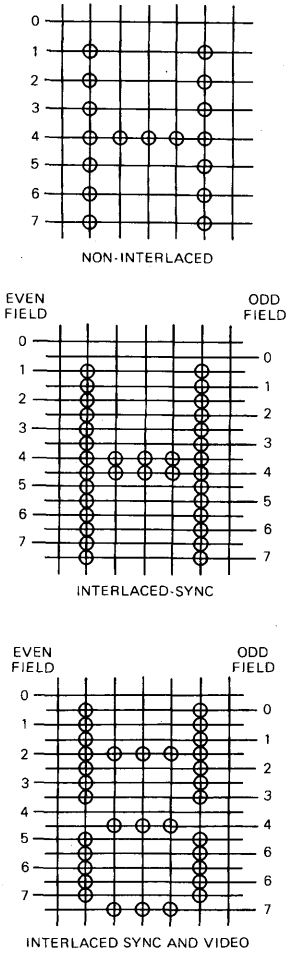


Figure 10. Comparison of Display Modes

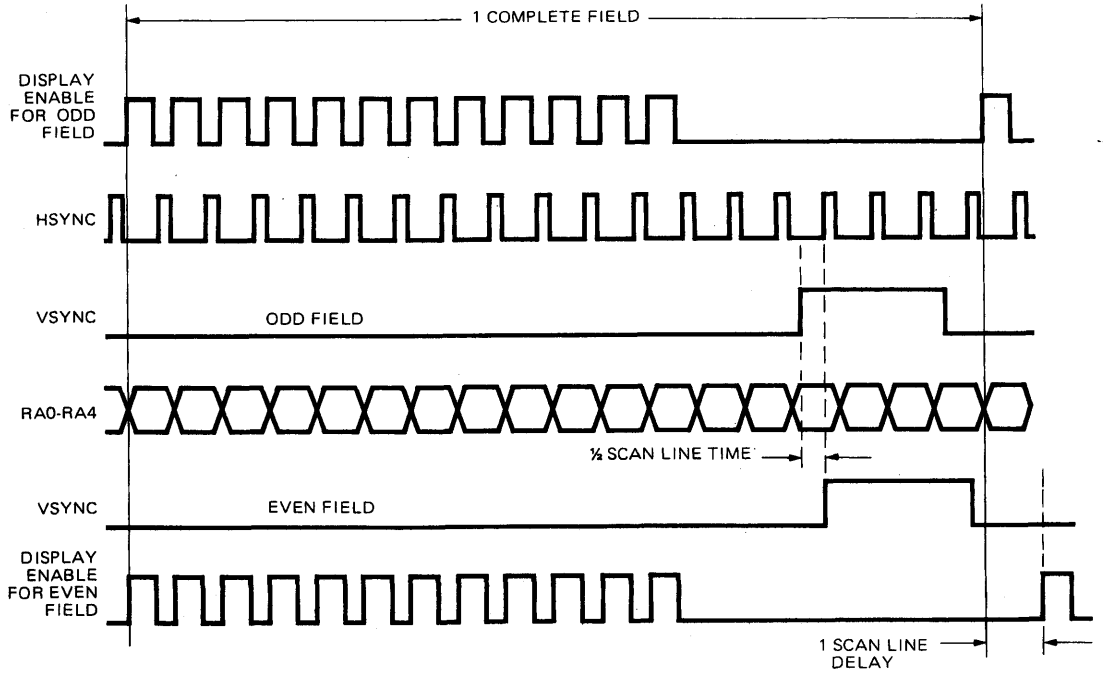


Figure 11. Interlaced Sync Mode and Interlaced Sync & Video Mode Timing

Cursor and Display Enable Skew Control

Bits 4 and 5 of the Mode Control register (R8) are used to delay the Display Enable and Cursor outputs, respectively. Figure 12 illustrates the effects of the delays.

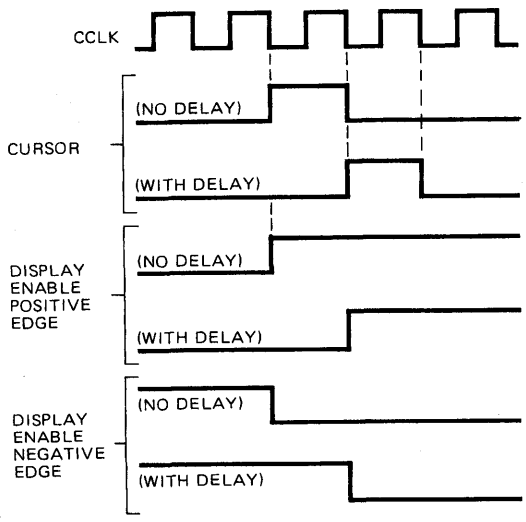


Figure 12. Cursor and Display Enable Skew

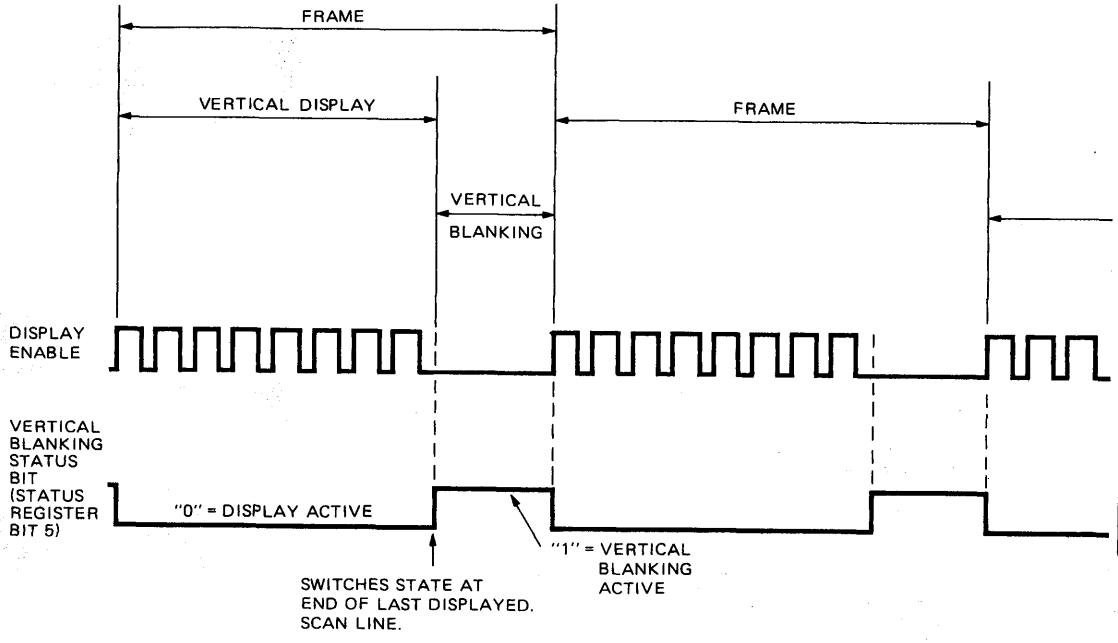


Figure 13. Operation of Vertical Blanking Status Bit

CRTC Register Comparison Table

NON-INTERLACED

Register	UM6845R/RA/RB MC6845 MC6845*1	MC6845R/RA/RB HD6845R	UM6845/A/B HD6845S	UM6845E/EA/EB
R0 Htotal	Total-1	Total-1	Total-1	Total-1
R1 Hdisp	Actual	Actual	Actual	Actual
R2 Hsync	Actual	Actual	Actual	Actual
R3 Sync Width	Horizontal (& Vertical *1)	Horizontal	Horizontal & Vertical	Horizontal & Vertical
R4 Vtotal	Total-1	Total-1	Total-1	Total-1
R5 Vtotal Adjustment	Any Value	Any Value	Any Value	Any Value
R6 Vdisp	Any Value <R4	Any Value <R4	Any Value <R4	Any Value <R4
R7 Vsync	Actual-1	Actual-1	Actual-1	Actual-1
R8 B0-1	Interlace	Interlace	Interlace	Interlace
Mode Select B2	–	–	–	Row/Column or Binary Addr.
B3	–	–	–	Shared or Transparent Addr.
B4	(Display Enable Skew *1)	–	Display Enable Skew	Display Enable Skew
B5	(Display Enable Skew *1)	–	Display Enable Skew	Cursor Skew
B6	(Cursor Skew *1)	–	Cursor Skew	RA4/
B7	(Cursor Skew *1)	–	Cursor Skew	Transparent
R9 Scan Lines	Total-1	Total-1	Total-1	Total-1
R10 Cursor Start	Actual	Actual	Actual	Actual
R11 Cursor End	Actual	Actual	Actual	Actual
R12/R13 Display Addr.	Write Only Read/Write (MC6845 & *1)	Read/Write	Read/Write	Write Only
R14/R15 Cursor Position	Read/Write	Read/Write	Read/Write	Read/Write
R16/R17 Position	Read Only	Read Only	Read Only	Read Only
R18/R19 Update Addr. Register	N/A	N/A	N/A	Transparent Mode Only
R31 Dummy Register	N/A	N/A	N/A	Transparent Mode Only
Status Register	Yes (UM6845R)	No	No	Yes

CRTC Register Comparison Table (Continued)

INTERLACED SYNC

Register	UM6845R/RA/RB MC6845 MC6845*1	MC6845R/RA/RB HD6845R	UM6845/A/B HD6845S	UM6845E/EA/EB
R0 Htotal	Total-1 = Odd or Even	Total-1 = Odd	Total-1 = Odd	Total-1 = Odd or Even

INTERLACED SYNC AND VIDEO

R4 Vtotal	Total-1	Total-1	Total-1	Total-1
R6 Vdisp	Total	Total/2	Total	Total
R7 Vsync	Actual-1	Actual-1	Actual-1	Actual-1
R9 Scan Lines	Total-1 Odd/Even	Total-1 Only Even	Total-1 Odd/Even	Total-1 Odd/Even
R10 Cursor Start	Odd/Even	Both Odd	Odd/Even	Odd/Even
R11 Cursor End	Odd/Even	Both Even	Odd/Even	Odd/Even
I_{CCLK}	2.5 MHz	2.5 MHz	3.7 MHz	3.7 MHz

Ordering Information

Part Number	CPU Clock Rate	Package
UM6845E	1 MHz	40L DIP
UM6845EA	2 MHz	40L DIP
UM6845EB	3 MHz	40L DIP

UM70C171/-50/-65

Color Palette With Triple 6-Bit DAC

Features

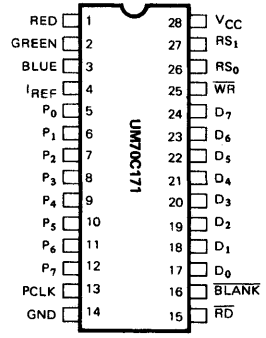
- Pixel Rates of 35 MHz, 50 Mhz & 65 MHz.
- 256 x 18 Bit Color Palette
- 256K possible Colors
- Color Palette Read-back
- Three Internal 6-Bit DACs
- Direct Drive (75Ω) Video Cable
- RGB Analog Output
- Composite Blank
- Single +5V Power Supply
- Low Power, High Performance CMOS Process
- TTL Compatible Inputs
- Full Asynchronous μP Interface
- Available in 28 pin DIP and 44 PLCC packages

Description

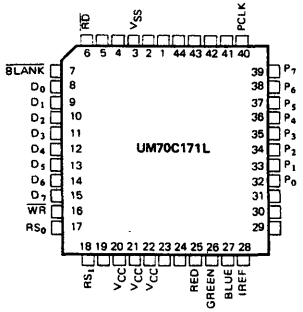
The UM70C171 is a monolithic triple 6-bit video digital-to-analog converter with on-chip 256 x 18 Bit color palette intended for graphics applications. The color palette makes possible the display of 256 colors selected from a total of 256K possible colors through the internal 6-bit RGB video DACs. The DACs are capable of driving single or double terminated 75Ω loads to normal video levels at pixel rates of 35 MHz, 50 MHz, & 65 MHz. The UM70C171 provides a bidirectional microprocessor interface with TTL compatible inputs. The UM70C171 is pin compatible with the Inmos IMS G171/176.

Pin Configurations

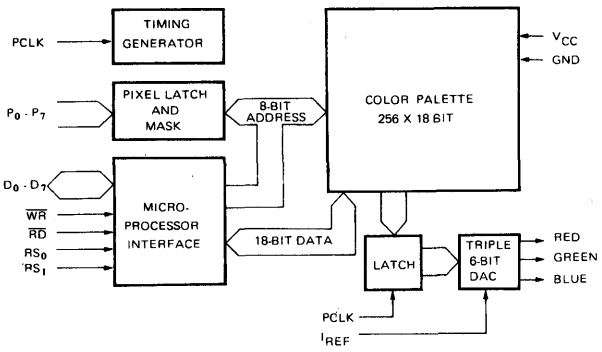
28-Pin DIP



44-Pin PLCC



Block Diagram



PIN NAMES	
$P_0 - P_7$	Pixel address inputs
$D_0 - D_7$	Program data I/O's
$RS_0 - RS_1$	Register select
RED, GREEN, BLUE	Analog video outputs
PCLK	Pixel clock
$\overline{WR}$	Write enable
$\overline{RD}$	Read enable
$\overline{BLANK}$	Video blanking input
IREF	Reference current
V_{CC}	+5 volt supply input
GND	Ground

Pin Description

Pin No.	Symbol	I/O	Description
1 2 3	RED GREEN BLUE	O O O	These signals are the analog outputs of the 6-bit DACs. These are the currents used for each of the guns in an RGB (Red, Green, Blue) video display. Each DAC is composed of 63 current sources. The output of each of these current sources is summed together according to the applied 6-bit binary value.
4	IREF	I	This is the Reference Current Input. The current forced out of this pin to ground determines the current sourced by each of the 63 current sources in each of the three 6-bit DACs. Each current source produces 1/30 of IREF when activated by the 6-bit digital input code.
5-12	P_0-P_7	I	These are the Pixel Address lines. This byte-wide information is latched and masked by the Pixel Mask Register. The resulting value is used as an address of a location in the Color Palette RAM.
13	PCLK	I	The Pixel Clock signal is applied to this pin. The rising edge controls the latching of the Pixel Address and Blanking Inputs. It also controls the progress of these values through the three stage pipeline of the Color Palette and through the DACs to the outputs.
14	GND	I	This is the power supply connection, and is connected to ground.
15	$\overline{RD}$	I	This is the active Low READ bus control signal. When active, any information present on the internal data bus is available on the Data I/O lines (D_0-D_7).
16	$\overline{BLANK}$	I	This is an active Low signal that forces the DAC's outputs to zero. When $\overline{BLANK}$ is asserted, a video monitor's screen becomes black and the DACs ignore any output values from the Color Palette. However, the Color Palette can still be updated through D_0-D_7.
17-24	D_0-D_7	I/O	These are the bidirectional Data I/O lines used by the host microprocessor to WRITE information (using the active Low $\overline{WR}$) into and READ information (using the active Low $\overline{RD}$) from the UM70C171 internal registers (Pixel Address register, Color Value register, and Pixel Mask register). During the WRITE cycle, the rising edge of $\overline{WR}$ latches the data into the selected register. The rising edge of $\overline{RD}$ determines the end of the READ cycle. With $\overline{RD}$ and $\overline{WR}$ equal to a logic HIGH, the Data I/O lines will no longer contain information from the selected register and will go into a tristate mode.
25	$\overline{WR}$	I	This is the active Low WRITE signal, and controls the timing of the WRITE operations on the microprocessor interface inputs, D_0-D_7.
26, 27	RS_0, RS_1	I	These are the Register Select lines which control the selection of one of the three internal registers. These lines are sampled during the falling edges of the enable signals ($\overline{RD}$ or $\overline{WR}$). (See Functional Description for more information regarding the internal registers.)
28	V_{CC}		This is the positive power supply pin. It is normally connected to +5V DC and bypassed with a 10μF tantalum capacitor.

Functional Description

The UM70C171 forms the output stage for high resolution raster scan RGB video systems. It contains a Color Palette with 256 memory locations that are 18 bits wide. The color palette's output is connected to three high speed current output 6-bit video DACs. The devices use on-board registers to easily interface with microprocessors.

Microprocessor Interface

The UM70C171 Microprocessor interface consists of three internal registers; Pixel Address Register, Color Value Register and Pixel Mask Register. These are individually accessed by register select signals, RS_0 and RS_1. The following table defines which register is selected by the logic states of RS_0 and RS_1.

RS_0	RS_1	Register
0	0	Pixel Address (Write Mode)
1	1	Pixel Address (Read Mode)
1	0	Color Value
0	1	Pixel Mask

The contents of the color palette can be accessed through the Color Value and Pixel Address registers.

All of the operations on the microprocessor interface can take place asynchronously to the pixel information currently being processed by the Color Palette.

The Pixel Address register is a byte-wide latch that receives and latches address information applied to pins P_0-P_7. It can be used in both Read and Write mode depending on the logic state of RS_0 and RS_1, With RS_0 = RS_1 = 0 (register select = 0, 0), the Pixel Address register is in the write mode. Two events normally precede WRITING one or more new color definitions to the color palette. The first is the specification of a color palette address. Second, the Color Value register must be loaded with a color definition. The sequence of data transfer is (1) the desired color palette address - this address is stored in the Pixel Address register and (2) the color definitions: RED, GREEN and lastly, BLUE. Refer to Figures 10 and 11.

When RS_0 = RS_1 = 1 (register select = 1, 1), the Pixel Address register is in the Read mode. Once again, two events take place and normally precede READING one or more color definitions in the color palette. The first action is to specify an address within the color palette. The second is to load the Color Value register with the contents of the location addressed in the color palette. The color definition data transfer sequence is RED, GREEN and lastly, BLUE. Refer to Figures 9, 12, and 13.

The Color Value register is an internal 18-bit wide register used as a buffer between the microprocessor interface and the color palette. It is accessed by setting RS_0 = 1 and RS_1 = 0. A color definition can be read from or written to this register by a sequence of three byte-wide transfers to this register address. When a byte is written to this register, only the least significant six bits (D_0-D_5) contain color information. When a byte is read from this register address, only the six least significant bits contain information - the most significant two bits are set to zero. Refer to Figures 9-13.

After the write sequence is completed, the Color Value register's contents are written to the specified color palette address stored in the Pixel Address register. Finally, the Pixel Address register is automatically incremented.

The color definitions can be read from the UM70C171 color palette. After setting RS_0 and RS_1 equal to 1, the desired color palette address is stored in the Pixel Address register. The color definition (18-bits) in the desired color palette location is then transferred to the Color Value register and the Pixel Address is auto-incremented. With successive read cycle, the color definitions pointed to by the incremented address is transferred to the Color Value register. Refer to Figure 12.

Attempting to update the color palette when $\overline{\text{BLANK}}$ is not asserted results in the data from the Color Value register taking precedence over the UM70C171 bit mapping operation. The output of the three 6-bit DACs will be based on the color definition from the memory location specified by the Pixel Address register and not the address found on P_0-P_7. This conflict results in the DACs generating unexpected output levels. This can last as long as two PCLK periods.

The Pixel Mask register is a byte-wide latch. By setting RS_0 = 0 and RS_1 = 1, the Pixel Mask register can be accessed by the microprocessor interface, D_0-D_7. This register is used to mask selected bits of the Pixel Address values applied to the Pixel Address inputs (P_0-P_7). A "1" in any location in the Pixel Mask register leaves the corresponding bit to zero. The operation of the Pixel Mask register does not affect the address of the color definition when the microprocessor accesses the color palette. The masking operation makes it possible to alter the displayed colors without altering the contents of external video memory or the UM70C171 color palette.

Writing to the color palette

A new color definition can be stored in the color palette by first specifying the initial address under write mode. This address is stored in the Pixel Address register (RS_0 = RS_1 = 0). The initial address is followed by RED, GREEN and BLUE color definition data (RS0 = 1, RS1 = 0). These six-bit inputs are collected together in the Color

Value register for a total of 18 bits. This new color definition is then transferred to the location pointed to by the information stored in the Pixel Address register. As soon as this transfer is completed, the Pixel Address register is auto-incremented. This allows consecutive color palette locations to be updated without the microprocessor specifying each address. All that is necessary is to continue supplying the RED, GREEN and BLUE data for each consecutive address. Refer to Figures 10 and 11.

Reading from the color palette

To read a location in the color palette, an address is sent on the Data I/O lines (D_0-D_7) under Read mode and stored in the Pixel Address register (RS_0 = RS_1 = 1). The color definition contained in the specified location is then transferred to the Color Value register. Once again, the Pixel Address register is auto-incremented. The color definition can now be retrieved with three sequential read operations (RS_0 = 1, RS_1 = 0). The first byte placed on the Data I/O lines contains the RED value. The next is GREEN and the final is BLUE. The two most significant bits are set to zero in each case. In a manner similar to the write mode, consecutive color palette locations can be ready by simply specifying the beginning address and reading color palette one or more times. Refer to Figures 9, 12 and 13.

If the Pixel address register is ever updated during a read or write operation, the current data sequence is terminated and a new read or write operation is initialized.

Real-Time Transfer

In typical applications, the microprocessor should access the color palette only during the retrace intervals to avoid "sparkle" on the screen. The UM70C171, while accessing the color palette during active display time, lets any disturbed pixels same as previous pixels. This greatly reduced viewer distress which sparkle otherwise creates. Because of this, the limitation of 256 colors out of 256K on the same screen can be removed. This effectively provides all 256K colors for users.

Video path

The Video path consists of the Pixel Latch and Mask (inputs P_0-P_7), color palette (256 18-bit wide RAM), 18-bit wide bus, and an 18-bit wide latch on the inputs of the three 6-bit high-speed video DACs. The video path uses a three clock cycle (PCLK) pipeline for the Pixel Address and $\overline{BLANK}$ inputs. These signals are latched on the rising edge of PCLK.

Analog outputs

The analog outputs are designed to drive single-terminated 75Ω loads to a peak-white amplitude of 0.7V.

The reference current (IREF) for this output is set to 4.44 mA. The analog outputs can also drive double-terminated 75Ω loads with IREF set to 8.88 mA.

The analog outputs can be set to zero by using $\overline{BLANK}$ input. This is an active Low signal that forces the analog outputs to ground by placing all zeros on the DACs' inputs. The color definition selected by the Pixel Address is ignored. Each of the 63 current sources used in each of the 6-bit DACs produces 1/30 IREF. Therefore, the magnitude of peak white voltage is a function of the output loading and is determined by:

$$V_{PEAK\ WHITE} = 2.1\ (I_{REF})R_L$$

$$V_{BLACK\ LEVEL} = 0V.$$

AC Characteristics: (T_A = 0°C to +70°C, V_{CC} = 5V ± 10%, GND = 0V)

Symbol	Parameter	UM70C171		UM70C171 -50		UM70C171 -65		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CHCH}	PCLK Period	28		20		15.3		ns	
Δt_{CHCH}	PCLK Jitter		±2.5		±2.5		±2.5	%	Note 1
t_{CLCH}	PCLK Width Low	9		6		5		ns	
t_{CHCL}	PCLK Width High	7		6		5		ns	
t_{PVCH}	Pixel Word Setup Time	4		4		3		ns	Note 2
t_{CHPX}	Pixel Word Hold Time	4		4		3		ns	Note 2
t_{BVCH}	BLANK Setup Time	4		4		3		ns	Note 2
t_{CHBX}	BLANK Hold Time	4		4		3		ns	Note 2
t_{CHAV}	PCLK to valid DAC Output	5	30	5	30	5	30	ns	Note 3
Δt_{CHAV}	Differential Output Delay		1		1		1	ns	Note 4
t_{WLWH}	WR Pulse Width Low	50		50		50		ns	
t_{RLRH}	RD Pulse Width Low	50		50		50		ns	
t_{SVWL}	Register Select Setup Time (Write Cycle)	15		10		10		ns	
t_{SVRL}	Register Select Setup (Read Cycle)	15		10		10		ns	

AC Characteristics (Continued)

Symbol	Parameter	UM70C171		UM70C171 -50		UM70C171 -65		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{WLSX}	Register Select Hold Time (Write Cycle)	15		10		10		ns	
t_{RLSX}	Register Select Hold Time (Read Cycle)	15		10		10		ns	
t_{DVWH}	WR Data Setup Time	15		10		10		ns	
t_{WHDX}	WR Data Hold Time	15		10		10		ns	
t_{RLQX}	Output Turn-on Delay	5		5		5		ns	
t_{RLQV}	RD Enable Access Time		40		40		40	ns	
t_{RHQX}	Output Hold Time	5		5		5		ns	
t_{RHQZ}	Output Turn-off Delay		20		20		20	ns	Note 5
t_{WHWL1}	Successive Write Interval	3		3		3		t_{CHCH}	
t_{WHRL1}	WR followed by READ Interval	3		3		3		t_{CHCH}	
t_{RHRL1}	Successive READ Interval	3		3		3		t_{CHCH}	
t_{RHWLI1}	RD followed by WRITE Interval	3		3		3		t_{CHCH}	
t_{WHWL2}	WR after Color Write	3		3		3		t_{CHCH}	Note 6
t_{WHRL2}	RD after Color Write	3		3		3		t_{CHCH}	Note 6
t_{RHRL2}	RD after Color Read	6		6		6		t_{CHCH}	Note 6
t_{RHWL2}	WR after Color Read	6		6		6		t_{CHCH}	Note 6
t_{WHRL3}	RD after Read Address Write	6		6		6		t_{CHCH}	Note 6
	Read/Write Enable Transition Time		50		50		50	ns	

Note 1: This parameter is the allowed variation in the pixel clock frequency. It does not permit the pixel clock period to vary below the minimum value for pixel clock (tCHCH) period specified.

Note 2: It is necessary that the color palette's pixel address be a valid logic level with the appropriate setup and hold times at each rising edge of PCLK (this requirement includes blanking period).

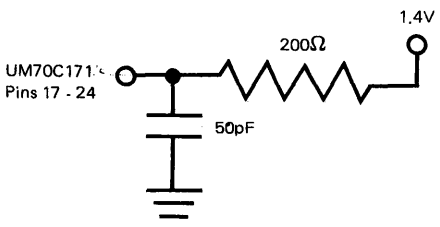
Note 3: A valid analog output is defined as the 50% point between successive values. This parameter is stable with time but can vary between different devices and may vary with different DC operating conditions.

Note 4: This applies to different analog outputs on the same device. This is a design parameter, not 100% tested.

Note 5: Measured at ±200 mV from initial steady state output voltage.

Note 6: This parameter allows synchronization between operations on the microprocessor interface and the pixel stream being processed by the color palette.

AC Test Conditions



Input Pulse Levels	GND to 3V
Input Rise and Fall Times (10% to 90%)	2.5 ns
Digital Input Timing Reference Level	1.5V
Digital Output Timing Reference Level	0.8V and 2.4V

Timing Waveforms

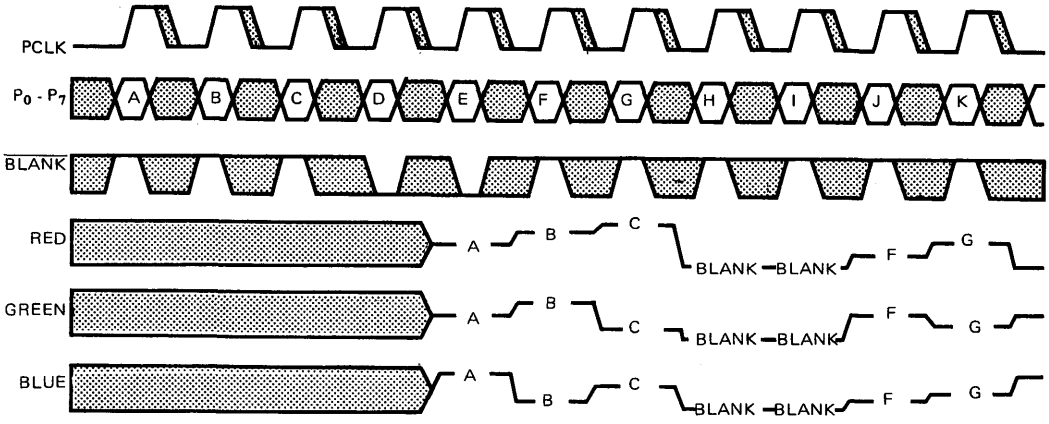


Figure 1. System Timing Diagram.

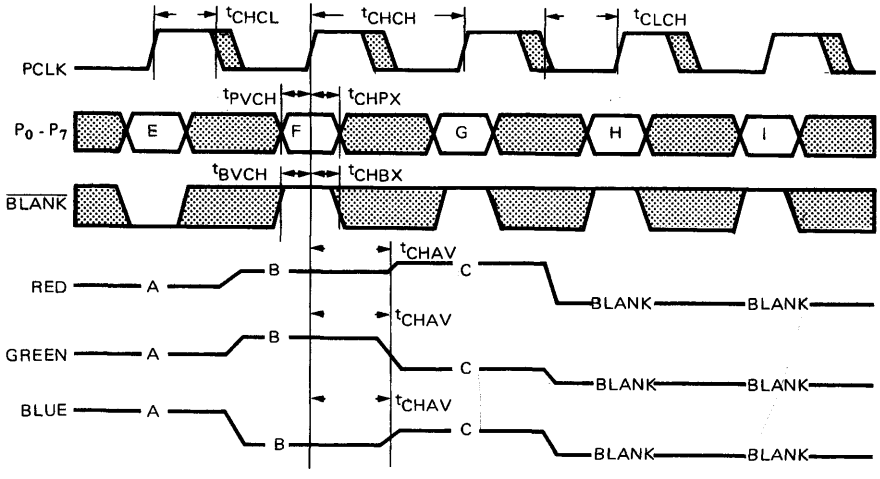


Figure 2. Detailing Timing Specifications.

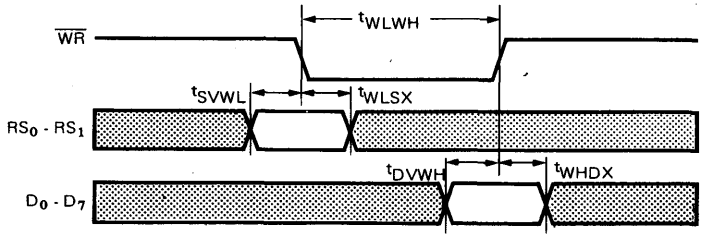


Figure 3. Basic Write Cycle Timing Diagram.

Timing Waveforms (Continued)

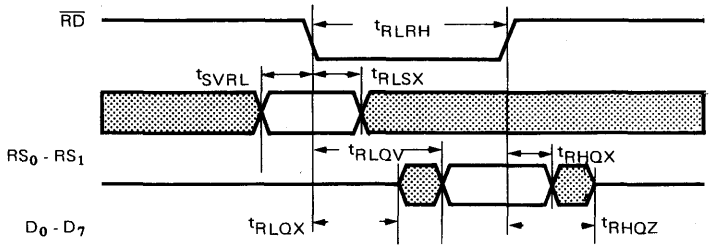


Figure 4. Basic Read Cycle Timing Diagram.

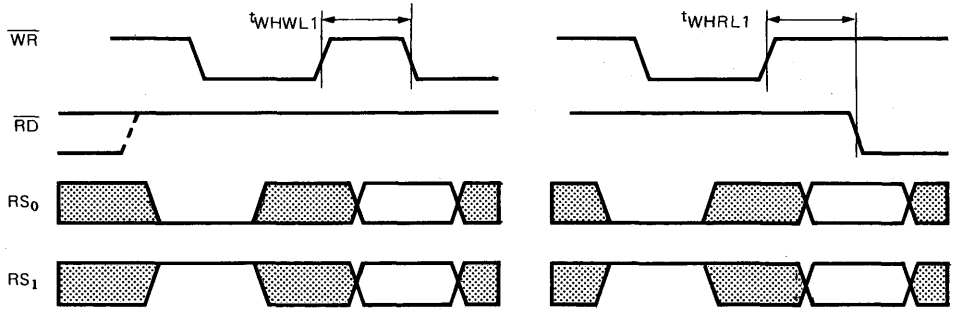


Figure 5. Write to Pixel Mask Register Followed by (a) Write and (b) Read.

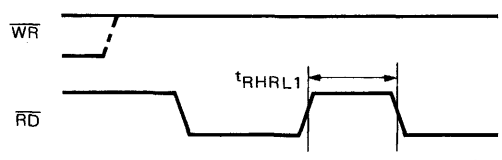


Figure 6a. Read from Pixel Mask or Pixel Address Register (Read or Write Mode) Followed by Read.

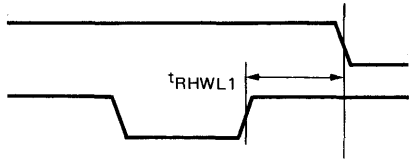


Figure 6b. Read from Pixel Mask or Pixel Address Register (Read or Write Mode) Followed by Write.

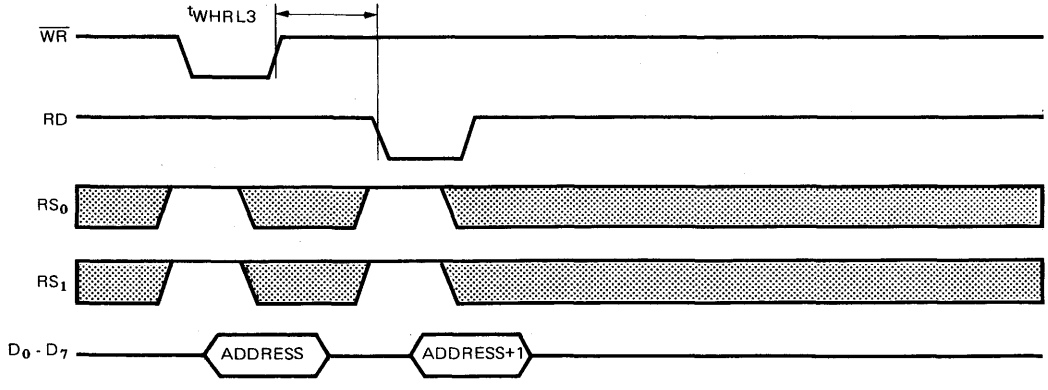


Figure 7. Write and Read Back Pixel Address Register (Read Mode).

Timing Waveforms (Continued)

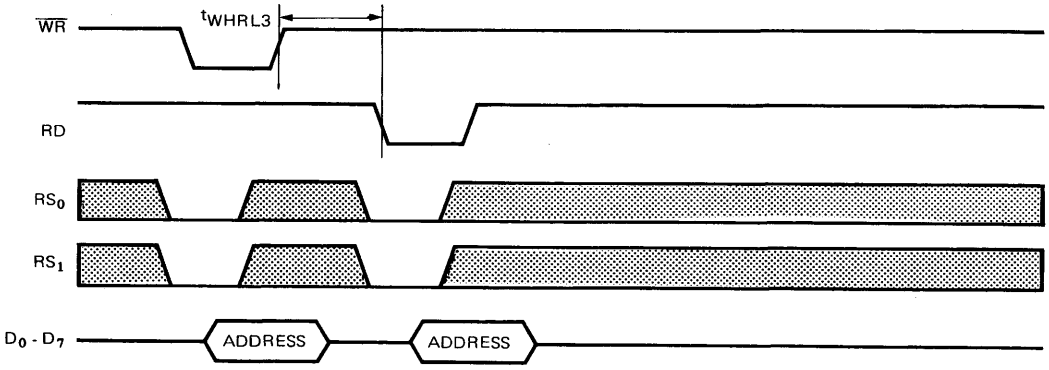


Figure 8. Write and Read Back Pixel Address Register (Write Mode).

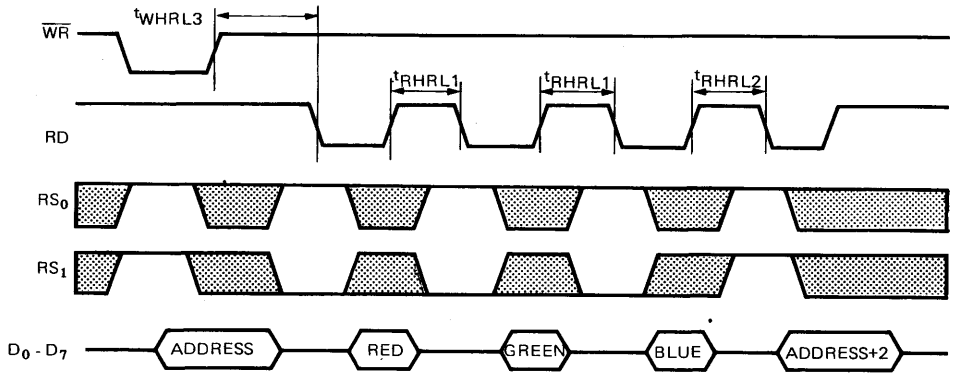


Figure 9. Read Color Value then Read Pixel Address Register (Read Mode).

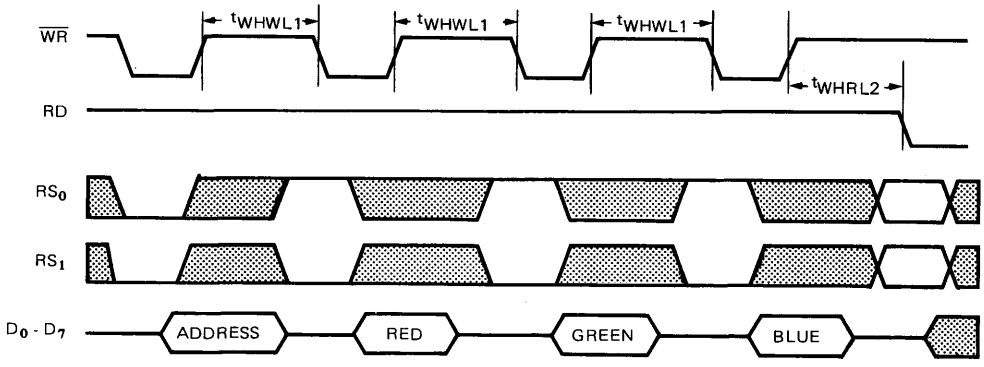


Figure 10. Color Value Write Followed by any Read.

Timing Waveforms (Continued)

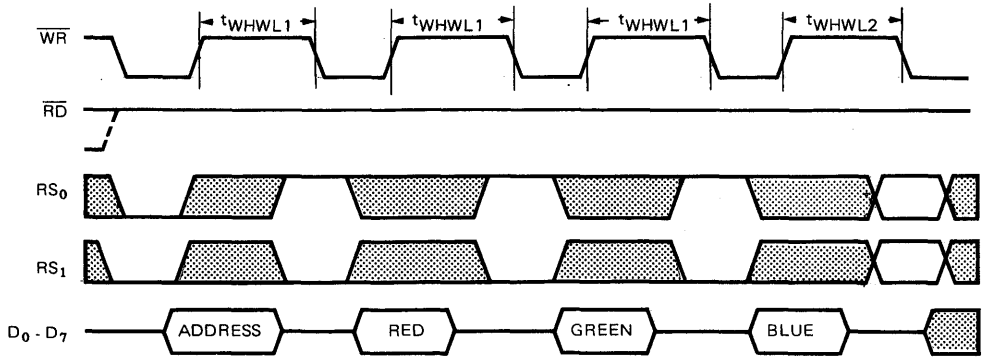


Figure 11. Color Value Write Followed by any Write.

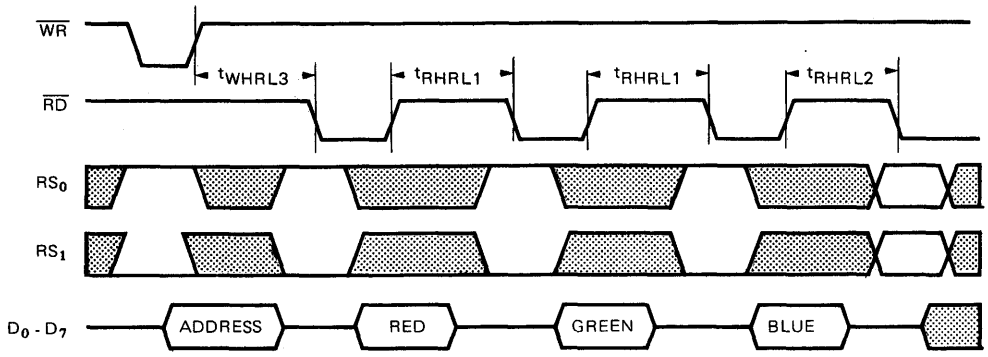


Figure 12. Color Value Read Followed by any Read.

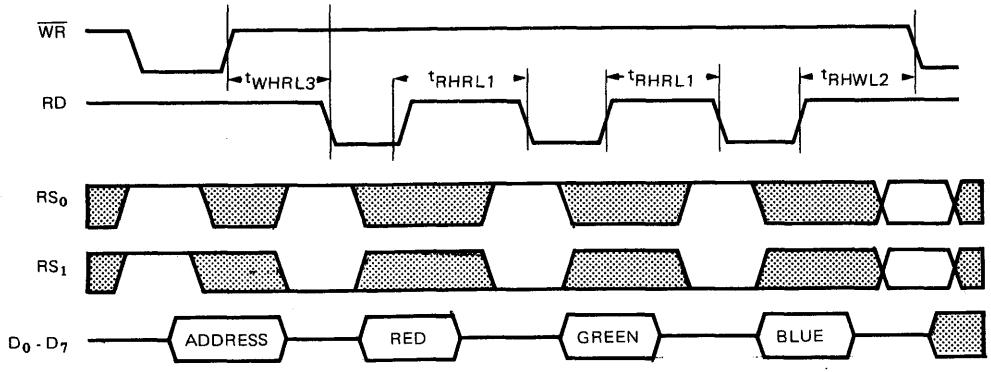


Figure 13. Color Value Read Followed by any Write.

Absolute Maximum Ratings *

Ambient Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +150°C
Supply Voltage to Ground Potential . . . . −0.5V to +7.0V
Applied Input Voltage . . . . . −0.5V to +7.0V

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics: T_A = 0°C to 70°C, V_{CC} 5V ± 10%, GND = 0V

Symbol	Parameter	Min.	Max.	Unit	Conditions
VOH	Output High Voltage	2.4		V	IOH = 400μA
VOL	Output Low Voltage		0.4	V	
VIH	Input High Voltage	2.0	V_{CC}+0.5	V	TTL
VIL	Input Low Voltage	−0.5	0.8	V	TTL
CO	Output Capacitance		7	pF	
CI	Input Capacitance		7	pF	
CIO	Input/Output Capacitance		16	pF	
ILI	Input Leakage Current	−10	10	μA	
OLI	Output Leakage Current	−10	10	μA	
IREF	Reference Current	−3	−10	mA	
ICC	Operating Supply Current (UM70C171)		150 160	mA mA	PCLK = 35 MHz PCLK = 50 MHz IOUT=Max. Digital Outputs Unloaded
VREF	Reference Voltage at IREF Pin	V_{CC}−3		V	V_{CC} = 4.5V, IREF = 10 mA
	DAC Resolution		6	BITS	
VOUT	Output Voltage Compliance (Pins 1-3)	1.5		V	IOUT ⩽ 10 mA
IOUT	Output Current Compliance (Pins 1-3)	21		mA	VOUT ⩽ 1V IREF ⩽ 10 mA
	Full Scale Error Note 7		±5	%	ZL = 75Ω + 30 pF IREF = 4.44 mA ZL = 37.5Ω+30 pF IREF = 8.88 mA
	DAC-to DAC Mismatch Note 8		±1	%	ZL = 75Ω + 30 pF IREF = 4.44 mA
	Internal Linearity Note 9		±0.5	LSB	ZL = 75Ω + 30 pF IREF = 4.44 mA
tON	Rise Time Note 10		8	ns	ZL = 75Ω + 30 pF IREF = 4.44 mA

Display

DC Electrical Characteristics (Continued)

Symbol	Parameter	Min.	Max.	Unit	Conditions
	Full-Scale Setting Time (UM70C171) Note 11		28	ns	ZL = 75Ω + 30 pF IREF = 4.44 mA
	Glitch Energy Note 12		±200	pV-sec	ZL = 75Ω + 30 pF IREF = 4.44 mA
COUTA	Analog Capacitance (Pins 1-3)		10	pF	$\overline{\text{BLANK}}$=Logic Low
VOUT-BLANK	Blanking Output Voltage		±0.5	LSB	$\overline{\text{BLANK}}$=Logic Low ZL = 75Ω + 30 pF IREF = 4.44 mA
	Unadjusted Output Offset Error		±0.5	LSB	$\overline{\text{BLANK}}$=Logic High ZL = 75Ω + 30 pF IREF = 4.44 mA
	Clock Feedthrough (UM70C171) Note 13		–35	dB	PCLK = 35 MHz PCLK = 50 MHz ZL = 75Ω + 30 pF IREF = 4.44 mA

Note 7: Full-scale error is defined as ([F. S. IOUT) RL – 2.1 (IREF) RL] / [2.1 (IREF) RL])100%. VBLACK LEVEL = 0V.

Note 8: The listed value is relative to the midpoint of the full-scale distribution of the internal three DACs.

Note 9: Zero and full-scale adjusted linearity error = [VOUT–VOFFSET–(D x VLSB)) / VLSB, VLSB = (VFULLSCALE –VOFFSET)/63].

Note 10: The rise time is measured for 10% to 90% of the full scale transition.

Note 11: The output signal's setting time is measured from a 2% change at the transition's initial value until it has settled to within 2% of the final value.

Note 12: This value is determined using triangle approximation: glitch energy = (area of positive transient) – (area of negative transient).

Note 13: These values are referenced to full-scale output.

Application Hints

Power Supply

The UM70C171 may draw large transient currents from the power supply. To ensure proper operation, it is necessary to utilize standard high frequency board layout techniques and power supply distribution.

The transient currents required by the UM70C171 dictate that the AC impedance of the ground path must be kept to a minimum. This is accomplished by using the recommended decoupling capacitors, C1 and C2, as shown in Figure 14. These capacitors must have leads that are as short as possible. High frequency decoupling is accomplished with a 0.1μF chip capacitor, C1. A bead tantalum, between 10μF to 47μF, should be used for C2.

Differential ground noise can be created when voltage difference appears between pin 14 and the ground of the digital devices driving the UM70C171. This difference is caused by series impedance in the ground path and the current transients drawn by the UM70C171. The differential ground noise can be minimized by using large, low inductance ground paths between the digital devices that drive the UM70C171 and pin 14. Therefore, a ground plane layout is recommended.

Analog Output-Line Driving

The connection between the UM70C171 outputs and the RGB inputs of the video monitor it is driving should be viewed as a transmission line. Impedance changes along this line will result in the reflection of part of the video signal back to the DACs' outputs. These reflections may result in a degradation in the picture quality displayed on the monitor. To ensure good signal fidelity RF techniques should be observed. Any traces connecting the UM70C171 to an onboard connector should form a transmission line of 75Ω impedance. However, the need to ensure

that the connecting traces form a transmission line can be eliminated by placing the DACs' output termination resistor at the output connector instead of the DACs' output pin. The coaxial cable that connects the UM70C171 outputs to a video monitor should have a characteristic impedance of 75Ω. Connectors on the coaxial line can cause impedance change. Any connectors used with the coaxial cable must match its characteristic impedance.

The UM70C171 DACs use switched current sources that are summed together, thus generating the output current. Each 6-bit DAC consists of 63 current sources, each of which has a magnitude of 1/30 (IREF). The digital input code determines the number of current sources that are active and contributing to the total output current. This output current, in conjunction with a termination resistance connected between each DAC output and ground, sets the full-scale magnitude of the output voltage. There are four different methods of terminating the UM70C171 DAC outputs:

(1) Single Termination at the DAC (75Ω)
(2) Single Termination at the Destination (75Ω)
(3) Double Termination (37.5Ω)
(4) Buffered Signal

(1) Single termination at the source involves placing a single termination resistor at each DAC output of the UM70C171. No other terminating load is present. Therefore, a high-input impedance monitor should be used. The AC load driven by the DACs' outputs is the transmission line impedance in parallel with the load resistor. The transmission line's impedance should match the impedance of the load resistor. Thus, the DACs' output has an initial signal amplitude that is half the DC value expected. This half-amplitude signal is 100% reflected by the open circuit presented by the monitor input. This restores the signal amplitude to the expected value. The reflections from the monitor propagate back towards the DAC outputs. The load resistor at each DAC output presents a correctly terminated transmission line so no further reflections occur. This arrangement is relatively tolerant to mismatches in the transmission line between the DAC and the monitor because no reflections occur at the DAC end of the transmission line. However, multiple monitors should not be connected in parallel despite each monitor's high input impedance.

(2) Single-termination at the destination has the termination impedance at the input of the monitor acting as both the load resistor for the DAC and the termination impedance of the cable (transmission line). If the connection between the UM70C171 is correctly terminated there will be no reflections. However, if there are any line impedance variations along the cable, reflections will occur and create "ghost images" on the display. This occurs because there is a reflection from the point where the mismatch occurs back to the DACs' output. The signal then reflects off the DAC's output back toward the monitor. It arrives with a significant time delay following the original signal and "ghosting" results.

(3) Double-termination of the DAC outputs allows each end of the transmission line to be correctly matched. This results in the least amount of reflection and the highest signal and display fidelity. This termination method also allows for the fastest rise time. The DAC termination's RC time constant sets the outputs' rise time. The greater the time constant, the slower the rise time. Therefore, the rise time will be minimized since the impedance using this termination technique is less than that achieved with single termination. With double-termination, it is necessary to increase IREF to 8.8 mA to ensure a full-scale output voltage of 700 mV.

(4) By placing a buffer at the DAC's output the UM70C171 will be able to drive large capacitance loads such as long lossy cables. The buffer requires a high input impedance, a condition that is satisfied by the LM1201 and LM1203. A 75Ω load is placed at the buffer's input.

The buffer's low output impedance should be matched to the interconnecting cable with a series resistor. The cable should then be terminated with the same resistance at the monitor.

Analog Output-Protection

Each of the UM70C171 pins has on-chip electrostatic discharge damage (ESD) protection. However, proper precautions for handling these parts are recommended during manufacturing to reduce the possibility of ESD.

Generating IREF

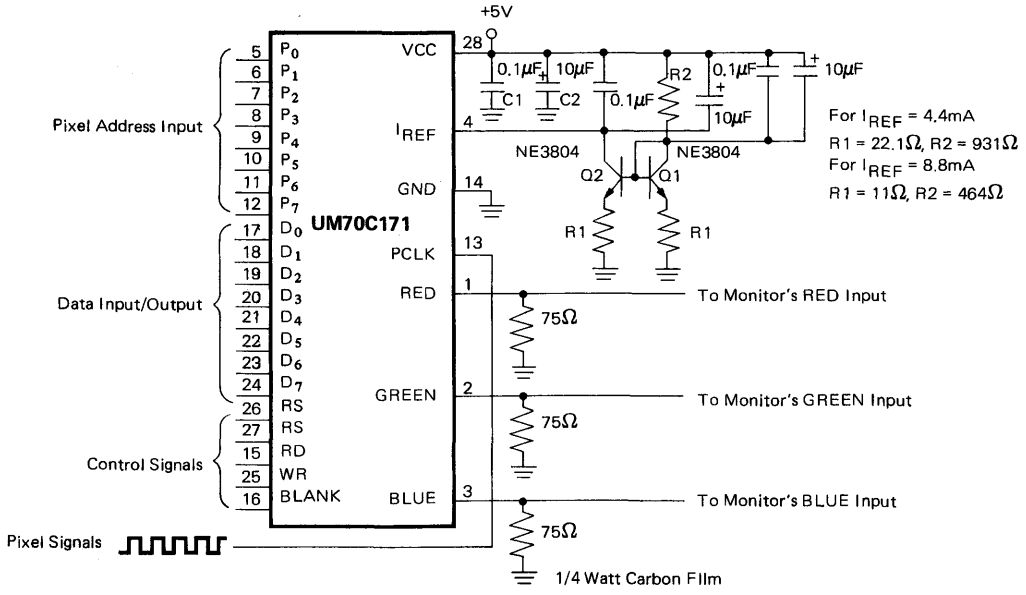
An active current source for IREF is recommended to ensure that the UM70C171 has predictable and stable output currents. There are numerous methods available to generate the reference current. One of the simplest circuits is shown with the UM70C171 in Figure 14. As shown, this IREF generator will sink −4.44 mA (single termination) with R1 = 22.1Ω and R2 = 931Ω.

For applications that use double termination, R1 = 11Ω and R2 = 464Ω. The diode connected transistor, Q1, across Q2's base-emitter junction performs a first-order compensation for thermal variations.

Figure 15 shows an alternative method of generating IREF. The LM334 precision current source is used in a temperature compensated configuration. The reference current is set by a single resistor, R1, independent of V_{CC}. The current's value is:

$$IREF = 33.85\ mV/R1$$

Application Hints (Continued)



Note: Bead-style tantalum capacitors should be used for the 10μF devices
Thermally connect the NPN transistors together with a Wakefield 25V series Equalizing Link.

Figure 14. Typical Connection Showing IREF Generator.

Figure 16 shows an LM10 and a discrete transistor generating IREF. The LM's onboard 200 mV voltage reference is used along with the reference's amplifier to set the voltage on R1 to 200 mV. Ignoring the small amount of base current, the discrete transistor's collector current (and therefore, IREF) is found to be:

IREF = 200 mV/R1

For IREF = 4.44 mA, R1 is, to the nearest 1% value 44.2Ω; IREF = 8.88 mA gives an R1 of 22.1Ω. The circuit shown in Figure 17 operates in the same fashion as the LM10 circuit in Figure 16. The LM611's on-board reference produces a nominal 1.24V. The voltage divider connected to the reference's output, pin 3, creates 200 mV that is applied to R1. The current (IREF) through the discrete transistor's collector is:

IREF = 200 mV/R1

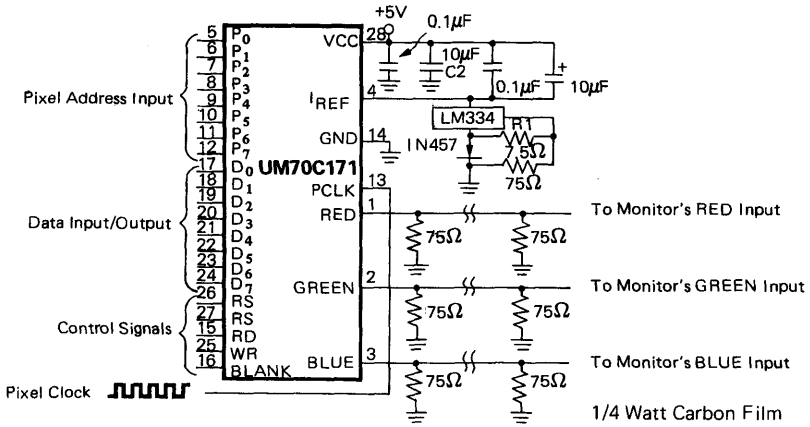
For IREF = 4.4 mA, R1 is, to the nearest 1% value 44.2Ω; IREF = 8.88 mA gives an R1 of 22.1Ω.

Decoupling IREF

The UM70C171 uses DACs composed of switched current sources. Each current source is based on a current mirror that produces (IREF)/30 when active. The total output current is determined by the number of active current sources switched to the output and the magnitude of IREF.

The magnitude of the current flowing through the internal current sources depends not only on IREF, but also on the voltage at pin 4 relative to V_{CC}. Therefore, voltage variations between V_{CC} and the IREF input can result in variations in the DAC's output current. These variations can be greatly attenuated by using a high frequency capacitor in parallel with a larger electrolytic capacitor to couple the IREF input to V_{CC}. This allows the reference current input to track both high and low frequency variations in V_{CC}.

Application Hints (Continued)



Note: Bead-style tantalum capacitors should be used for the 10μF devices.

Figure 15. Double Termination with LM334 Current Source IREF Generator.

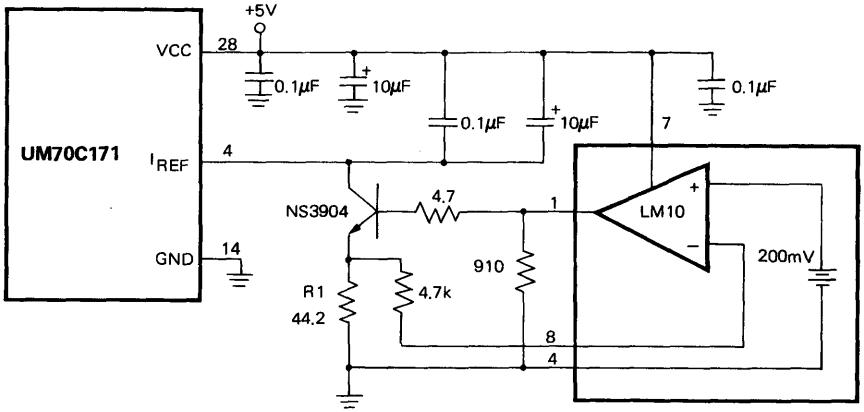


Figure 16. IREF Generator using LM10.

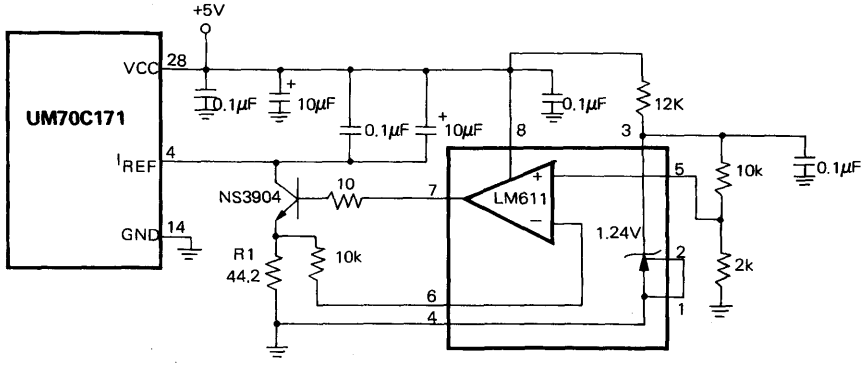


Figure 17. IREF Generator using LM611.

Ordering Information

Part No.	Frequency	Package
UM70C171	35 MHz	28L DIP
UM70C171L	35 MHz	44L PLCC
UM70C171-50	50 MHz	28L DIP
UM70C171L-50	50 MHz	44L PLCC
UM70C171-65	65 MHz	28L DIP
UM70C171L-65	65 MHz	44L PLCC

Storage

Part No.	Description	Page
UM8272A/A-4	Floppy Disk Controller	4-3
UM83C001	Hard Disk Controller	4-24
UM83C002	RAM Buffer Controller	4-44
UM83C003	Hard Disk Controller Interface	4-53
UM83C004	Hard Disk Controller Interface	4-57
UM83C021	Hard Disk Controller	4-61
UM83C022	AT HDC Interface	4-80
UM8326/B	Floppy Disk Data Separator (FDDS)	4-96
UM8388	Single-Chip Floppy Disk Controller	4-101
UM8397	Single-Chip Floppy Disk Controller	4-113
UM8398	Single-Chip Floppy Disk Controller	4-130

UMC

UM8272A/A-4

Floppy Disk Controller

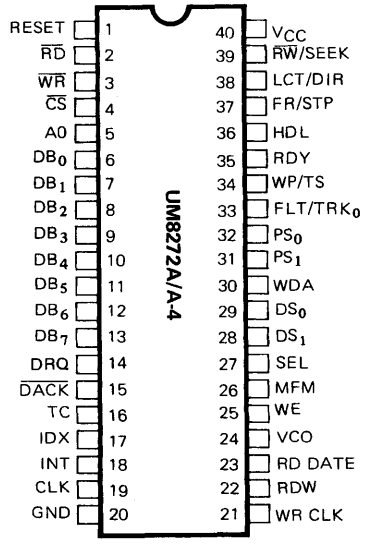
Features

- IBM compatible in both single and double density recording formats
- Programmable data record lengths: 128, 256, 512, or 1024 bytes/sector
- Multi-sector and multi-track transfer capability
- Drives up to 4 floppy or mini-floppy disks
- Data transfers in DMA or Non-DMA mode
- Parallel seek operations on up to four drives
- Compatible with all INTEL and most other microprocessors
- Single-phase 8MHz/4MHz clock for UM8272A/UM8272A-4 respectively
- Single + 5 volt power supply (± 10%)

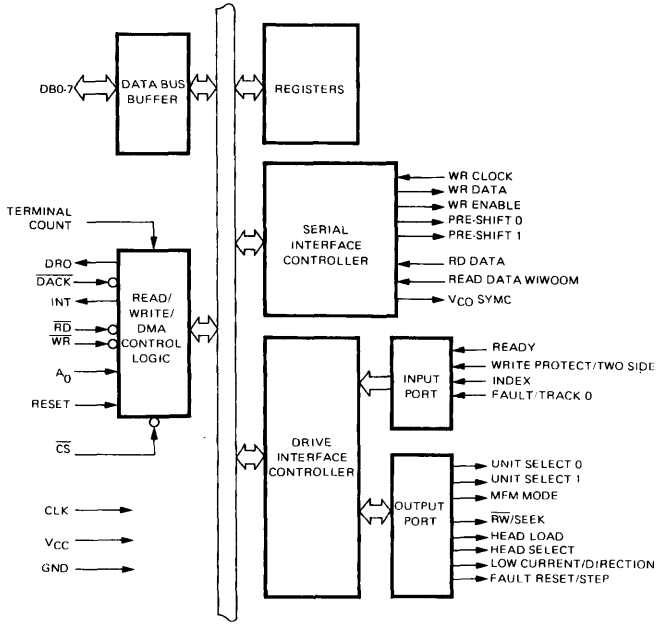
General Description

The UM8272A/A-4 is a LSI Floppy Disk Controller (FDC) Chip, which contains the circuitry and control functions for interfacing a processor to 4 floppy disk drives. It is capable of supporting either IBM 3740 single density format (FM), or IBM System 34 double density format (MFM) including double sided recording.

Pin Configuration



Block Diagram



The UM8272A/A-4 provides control signals which simplify the design of an external phase locked loop and write precompensation circuitry. The FDC simplifies and handles most of the burdens associated with implementing a floppy disk drive interface. The UM8272A/A-4 is a pin-compatible upgrade of the 8272.

Hand-shaking signals are provided in the UM8272A/A-4 which make DMA operation easy to incorporate with the aid of an external DMA controller chip. The FDC will operate in either DMA or Non-DMA mode. In the Non-DMA mode, the FDC generates interrupts to the processor every time a data byte is available. In the DMA mode, the processor need only load the command into the FDC and all data transfers occur under control of the UM8272A/A-4 and DMA controller.

There are 15 separate commands which the UM8272A/A-4 will execute. Each of these commands requires multiple 8-bit bytes to fully specify the operation which the processor wishes the FDC to perform. The following commands are available:

Read Data	Write Data
Read ID	Format a Track
Read Deleted Data	Write Deleted Data
Read a Track	Seek
Scan Equal	Recalibrate (Restore to Track 0)
Scan High or Equal	Sense interrupt Status
Scan Low or Equal	Sense Drive Status
Specify	

Address mark detection circuitry is internal to the FDC, which simplifies the phase locked loop and read electronics. The track stepping rate, head load time, and head unload time may be programmed by the user. The UM8272A/A-4 offers many additional features such as multiple sector transfers in both read and write with a single command, and full IBM compatibility in both single and double density models.

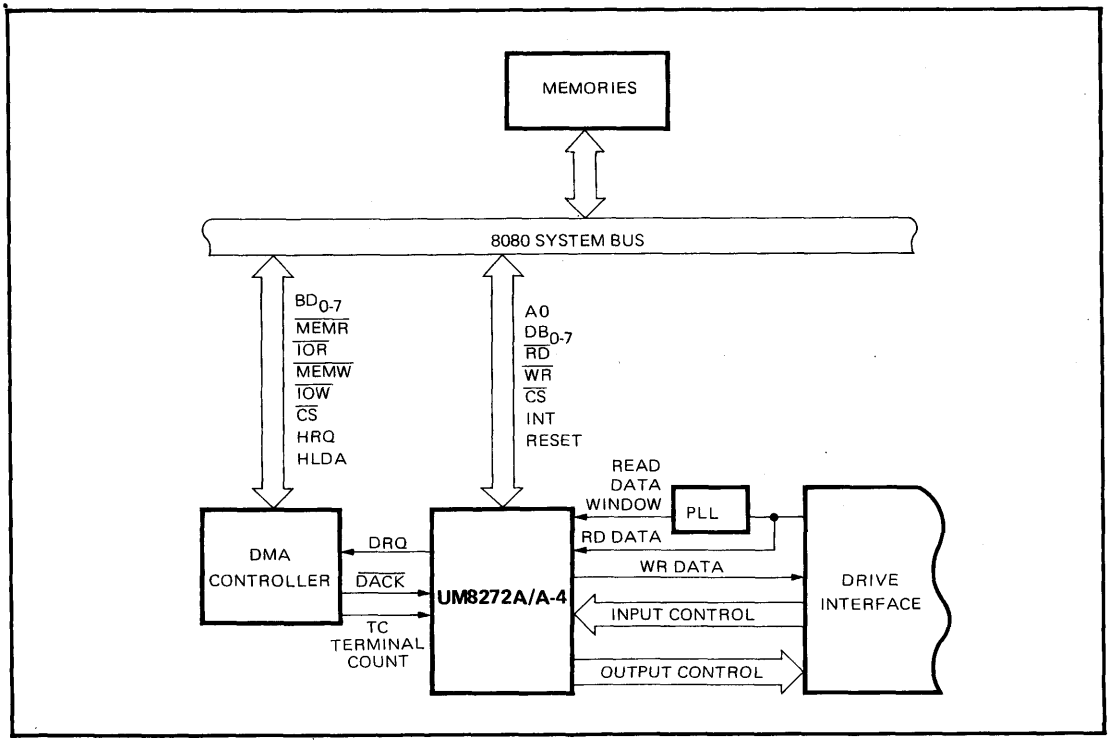


Figure 1. System Configuration

Absolute Maximum Ratings*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . −55°C to +150°C
All Output Voltages . . . . . −0.5 to +7 Volts
All Input Voltages . . . . . −0.5 to +7 Volts
Supply Voltage V_{CC} . . . . . −0.5 to +7 Volts
Power Dissipation . . . . . 1 Watt

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(T_A = 0°C to +70°C, V_{CC} = +5V ± 10%)

Symbol	Parameter	Limits		Units	Conditions
		Min.	Max.		
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	2.4	V_{CC}	V	I_{OH} = −400 μA
I_{CC}	V_{CC} Supply Current		120	mA	
I_{IL}	Input Load Current (All Input Pins)		10 −10	μA μA	V_{IN} = V_{CC} V_{IN} = 0 V
I_{LOH}	High Level Output Leakage Current		10	μA	V_{OUT} = V_{CC}
I_{OFL}	Output Float Leakage Current	−10	+10	μA	0.45 V ≤ V_{OUT} ≤ V_{CC}

Capacitance

(T_A = 25°C, f_c = 1 MHz, V_{CC} = 0V)

Symbol	Parameter	Limits		Unit	Conditions
		Min.	Max.		
$C_{IN}(\phi)$	Clock Input Capacitance		20	pF	All Pins Except Pin Under Test Tied to AC Ground
C_{IN}	Input Capacitance		10	pF	
$C_{I/O}$	Input/Output Capacitance		20	pF	

AC Characteristics

(T_A = 0°C to +70°C, V_{CC} = +5.0V ± 10%)

CLOCK TIMING

Symbol	Parameter	Min.	Max.	Unit	Notes
T_{CY}	Clock Period	120	500	ns	Note 5
t_{CH}	Clock High Period	40		ns	Note 4, 5
t_{RST}	Reset Width	14		t_{CY}	

READ CYCLE

t_{AR}	Select Setup to $\overline{RD}\downarrow$	0		ns	
t_{RA}	Select Hold from $\overline{RD}\uparrow$	0		ns	
t_{RR}	$\overline{RD}$ Pulse width	250		ns	
t_{RD}	Data Delay from $\overline{RD}\downarrow$		200	ns	
t_{DF}	Output Float Delay	20	100	ns	

Storage

AC Characteristics (Continued) (T_A = 0°C to +70°C, V_{CC} = +5.0V ± 10%)

WRITE CYCLE

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
t_{AW}	Select Setup to $\overline{WR}\downarrow$	0			ns	
t_{WA}	Select Hold from $\overline{WR}\uparrow$	0			ns	
t_{WW}	$\overline{WR}$ Pulse Width	250			ns	
t_{DW}	Data Setup to $\overline{WR}\uparrow$	150			ns	
t_{WD}	Data Hold from $\overline{WR}\uparrow$	10			ns	

INTERRUPTS

t_{RI}	INT Delay from $\overline{RD}\uparrow$			500	ns	Note 5
t_{WI}	INT Delay from $\overline{WR}\uparrow$			500	ns	Note 5

DMA

t_{ROCY}	DRQ Cycle Period	13			μs	Note 5
t_{AKRO}	$\overline{DACK}\downarrow$ to DRQ↓			200	ns	
t_{ROR}	DRQ ↑ to $\overline{RD}\downarrow$	800			ns	Note 5
t_{ROW}	DRQ ↑ to $\overline{WR}\downarrow$	250			ns	Note 5
t_{RORW}	DRQ ↑ to $\overline{RD}\uparrow$ or $\overline{WR}\uparrow$			12	μs	Note 5

FDD INTERFACE

t_{WCY}	WCK Cycle Time		2 or 4 1 or 2		μs	MFM = 0 MFM = 1 Note 2
t_{WCH}	WCK High Time	80	250	350	ns	
t_{CP}	Pre-Shift Delay from WCK↑	20		100	ns	
t_{CD}	WDA Delay from WCK ↑	20		100	ns	
t_{WDD}	Write Data Width	t_{WCH}−50			ns	
t_{WE}	WE ↑ to WCK ↑ or WE ↓ to WCK ↓ Delay	20		100	ns	
t_{WWCY}	Window Cycle Time		2 1		μs	MFM = 0 MFM = 1
t_{WRD}	Window Setup to RDD ↑	15			ns	
t_{RDW}	Window Hold from RDD ↓	15			ns	
t_{RDD}	RDD Active Time (HIGH)	40			ns	

FDD SEEK/DIRECTION/STEP

t_{US}	$US_{0,1}$ Setup to $\overline{RW}$/SEEK ↑	12			μs	Note 5
t_{SU}	$US_{0,1}$ Hold after $\overline{RW}$/SEEK ↓	15			μs	Note 5
t_{SD}	$\overline{RW}$/SEEK Setup to LCT/DIR	7			μs	Note 5
t_{DS}	$\overline{RW}$/SEEK Hold from LCT/DIR	30			μs	Note 5
t_{DST}	LCT/DIR Setup to FR/STEP↑	1			μs	Note 5
t_{STD}	LCT/DIR Hold from FR/STER ↓	24			μs	Note 5
t_{STU}	$DS_{2,1}$ Hold from FR/Step ↓	5			μs	Note 5
t_{STP}	STEP Active Time (High)		5		μs	Note 5
t_{SC}	STEP Cycle Time	33			μs	Note 3, 5
t_{FR}	FAULT RESET Active Time (High)	8		10	μs	Note 5
t_{IDX}	INDEX Pulse Width		10		t_{CY}	
t_{TC}	Terminal Count Width	1			t_{CY}	

Notes:
1. Typical values for T_A are 25°C and nominal supply voltage.
2. The former values are used for standard floppy and the latter values for mini-floppies.
3. t_{SC} = 33 μs min for different drive units. In the case of same unit, t_{SC} can range from 1 ms to 16 ms with 8 MHz clock period, and 2 ms to 32 ms with 4 MHz clock, under software control.
4. At 4 MHz, the clock duty cycle may range from 16% to 76%. Using an 8 MHz clock the duty cycle can range from 32% to 52%. Duty cycle is defined as: D.C. = 100 ($t_{CH} \rightarrow t_{CY}$) with typical rise and fall times of 5 ns.
5. The specified values listed are for an 8 MHz clock period. Multiply timings by 2 when using a 4 MHz clock period.

Pin Description

Pin			Connection to	I/O	Description
No.	Symbol	Designation			
1	RESET	Reset	Processor	I	Places FDC in idle state. Resets output lines to FDD to "0" (low). Does not affect SRT, HUT or HLT in Specify command. If RDY pin is held high during Reset, FDC will generate interrupt 1.024 ms later. To clear this interrupt use Sense Interrupt Status command.
2	$\overline{RD}$	Read	Processor	O (1)	Control signal for transfer of data from FDC to Data Bus, when "0" (low).
3	$\overline{WR}$	Write	Processor	I (1)	Control signal for transfer of data to FDC via Data Bus, when "0" (low).
4	$\overline{CS}$	Chip Select	Processor	I	IC selected when "0" (low), allowing $\overline{RD}$ and $\overline{WR}$ to be enabled.
5	AO	Data/Status Reg Select	Processor	I (1)	Selects Data Reg (A_0 = 1) or Status Reg (A_0 = 0) contents of the FDC to be sent to Data Bus.
6-13	DB_0-DB_7	Data Bus	Processor	I/O (1)	Bi-Directional 8-Bit Data Bus.
14	DRQ	Data DMA Request	DMA	O	DMA Request is being made by FDC when DRW = "1".
15	$\overline{DACK}$	DMA Acknowledge	DMA	I	DMA cycle is active when "0" (low) and Controller is performing DMA transfer.
16	TC	Terminal Count	DMA	I	Indicates the termination of a DMA transfer when "1" (high). It terminates data transfer during Read/Write/Scan command in DMA or interrupt mode.
17	IDX	Index	FDD	I	Indicates the beginning of a disk track.
18	INT	Interrupt	Processor	O	Interrupt Request generated by FDC.
19	CLK	Clock		I	Single phase 8-MHz square wave Clock.
20	GND	Ground			DC power return.
21	WRCLK	Write Clock		I	Write Data rate to FDD. FM = 500 kHz; MFM = 1 MHz, with a pulse width of 250 ns for both FM and MFM.
22	RDW	Read Data Window	Phase Lock Loop	I	Generated by PLL, and used to sample data from FDD.

Pin Description (Continued)

Pin			Connection to	I/O	Description
No.	Symbol	Designation			
23	RD DATE	Read Data	FDD	I	Reads data from FDD, containing clock and data bits.
24	VCO	VCO Sync	Phase Lock Loop	O	Inhibits VCO in PLL when "0" (low), enables VCO when "1".
25	WE	Write Enable	FDD	O	Enables write data into FDD.
26	MFM	MFM Mode	Phase Lock Loop	O	MFM mode when "1", FM mode when "0".
27	SEL	Head Select	FDD	O	Head 1 selected when "1" (high). Head 2 selected when "0" (low).
28, 29	DS_1, DS_0	Unit Select	FDD	O	FDD Unit Selected.
30	WDA	Write Data	FDD	O	Serial clock and data bits to FDD.
31, 32	PS_1, PS_0	Precompensation (pre-shift)	FDD	O	Writes Precompensation status during MFM mode. Determines early, late, and normal times.
33	FLT/TRK_0	Fault/Track 0	FDD	I	Senses FDD fault condition in Read/Write mode, and Track 0 condition in Seek mode.
34	WP/TS	Write Protect/ Two-Side	FDD	I	Senses Write Protect Status in Read/ Write mode; and Two Side Media in Seek mode.
35	RDY	Ready	FDD	I	Indicates FDD is ready to send or receive data.
36	HDL	Head Load	FDD	O	Causes read/write head in FDD to contact diskette.
37	FR/STP	Fit Reset/Stop	FDD	O	Resets fault F.F. in FDD in Read/ Write mode, contains stop pulses to move head to another cylinder in Seek mode.
38	LCT/DIR	Low Current/ Direction	FDD	O	Lowers Write current on inner tracks in Read/Write mode, determines direction head will stop in Seek mode. A fault reset pulse is issued at the beginning of each Read or Write command prior to the occurrence of the Head Load signal.
39	$\overline{RW}$/SEEK	Read Write/SEEK	FDD	O	When "1" (high) Seek mode selected, when "0" (low) Read/Write mode selected.
40	V_{CC}	+5V			DC Power.

Note: (1) Disabled when $\overline{CS}$ = 1.

UM8272A/A-4 Enhancements

On the UM8272A/A-4, after detecting the Index Pulse, the VCO Sync output stays low for a shorter period of time. See Figure 2-A.

On the 8272 there can be a problem reading data when Gap 4A is 00 and there is no 1AM. This occurs on some older floppy formats. The UM8272A/A-4 solves this problem by adjusting the VCO Sync timing so that it is not low during the data field. See Figure 2.

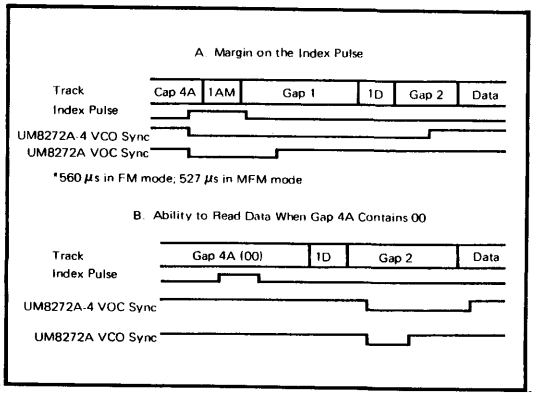


Figure 2. UM8272A/A-4 Enhancements over the 8272

UM8272A/A-4 Registers – CPU Interface

The UM8272A/A-4 contains two registers which may be accessed by the main system processor, a Status Register and a Data Register. The 8-bit Main Status Register contains the status information of the FDC, and may be accessed at any time. The 8-bit Data Register (several registers in a stack with only one register presented to the data bus at a time) stores data, commands, parameters, and FDD status information. Data bytes are read out of or written into the Data Register in order to program or obtain the results after execution of a command. The Status Register may only be read and is used to facilitate the transfer of data between the processor and UM8272A/A-4.

The relationship between the Status/Data registers and the signals $\overline{RD}$, $\overline{WR}$, and A_0 is shown in Table 1.

Table 1. A0, $\overline{RD}$, $\overline{WR}$ decoding for the selection of Status/ Data register functions.

A_0	$\overline{RD}$	$\overline{WR}$	Function
0	0	1	Read Main Status Register
0	1	0	Illegal (see note)
0	0	0	Illegal (see note)
1	0	0	Illegal (see note)
1	0	1	Read from Data Register
1	1	0	Write into Data Register

Note: Design must guarantee that the UM8272A/A-4 is not subjected to illegal inputs.

Table 2. Main Status Register Bit Description.

Bit Number	Name	Symbol	Description
DB_0	FDD 0 Busy	D_0B	FDD number 0 is in the Seek mode. If any of the bits are set FDC will not accept read or write command.
DB_1	FDD 1 Busy	D_1B	FDD number 1 is in the Seek mode. If any of the bits are set FDC will not accept read or write command.
DB_2	FDD 2 Busy	D_2B	FDD number 2 is in the Seek mode. If any of the bits are set FDC will not accept read or write command.
DB_3	FDD 3 Busy	D_3B	FDD number 3 is in the Seek mode. If any of the bits are set FDC will not accept read or write command.
DB_4	FDC Busy	CB	A read or write command is in process. FDC will not accept any other command.
DB_5	Execution Mode	EXM	This bit is set only during execution phase in non-DMA mode. When DB_5 goes low, execution phase has ended, and result phase has started. It operates only during NON-DMA modes of operation.
DB_6	Data Input/Output	DIO	Indicates direction of data transfer between FDC and Data Register. If DIO = "1" then transfer is from Data Register to the Processor. If DIO = "0", then transfer is from the Processor to Data Register.
DB_7	Request for Master	RQM	Indicates Data Register is ready to send or receive data to or from the Processor. Both bits DIO and RQM should be used to perform the hand-shaking functions of "ready" and "direction" to the processor.

The DIO and RQM bits in the Status Register indicate when Data is ready and in which direction data will be transferred on the Data Bus. The max time between the last $\overline{RD}$ or $\overline{WR}$ during command or result phase and DIO and RQM getting set or reset is 12 μs. For this reason every time Main Status Register is read the CPU should wait 12 μs. The max time from the trailing edge of the last RD in the result phase to when DB, (FDC Busy) goes low is 12 μs.

Note: There is a 12 μS or 24 μS ROM flag delay when using an 8 or 4 MHz clock respectively.

Storage

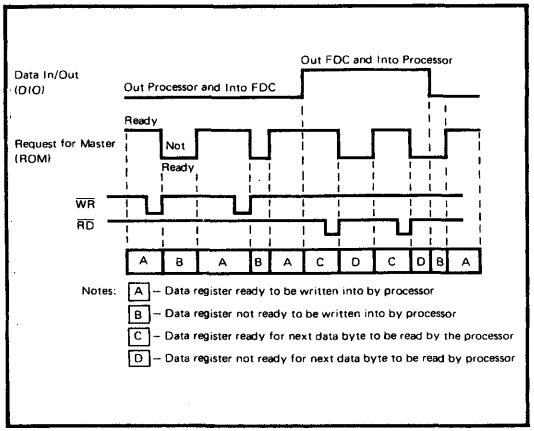


Figure 3. Status Register Timing

The UM8272A/A-4 is capable of executing 15 different commands. Each command is initiated by a multi-byte transfer from the processor, and the result after execution of the command may also be a multi-byte transfer back to the processor. Because of this multi-byte interchange of information between the UM8272A/A-4 and the processor, it is convenient to consider each command as consisting of three phases:

Command Phase:	The FDC receives all information required to perform a particular operation from the processor.
Execution Phase:	The FDC performs the operation it was instructed to do.
Result Phase:	After completion of the operation, status and other housekeeping information is made available to the processor.

During Command or Result Phases the Main Status Register (described in Table 2) must be read by the processor before each byte of information is written into or read from the Data Register. Bits D6 and D7 in the Main Status Register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the UM8272A/A-4. Many of the commands require multiple bytes, and as a result, the Main Status Register must be read prior to each byte transfer to the UM8272A/A-4. On the other hand, During the Result Phase, D6 and D7 in the Main Status Register must both be 1s (D6 = 1 and D7 = 1) before reading each byte from the Data Register. Note: this reading of the Main Status Register before each byte transfer to the UM8272A/A-4 is required in only the Command and Result Phases, and NOT during the Execution Phase.

During the Execution Phase, the Main Status Register need not be read. If the UM8272A/A-4 is in the non-DMA Mode, then the receipt of each data byte (if UM8272A/A-4 is reading data from FDD) is indicated by an interrupt signal on pin 18 (INT = 1), The generation of a Read signal (RD = 0) will reset the interrupt as well as output the Data onto the Data Bus. For example, if the processor cannot handle Interrupts fast enough (every 13 μs for MFM mode) it may poll the Main Status Registers and bit D7 (RQM) will function just like the Interrupt signal. If a Write Command is in process, the WR signal performs the reset to the Interrupt signal.

The UM8272A/A-4 always operates in a multi-sector transfer mode. It continues to transfer data until the TC input is active. In Non-DMA Mode, the system must supply the TC input.

If the UM8272A/A-4 is in the DMA Mode, no Interrupts are generated during the Execution Phase. The UM8272A/A-4 generates DRQs (DMA Requests) when each byte of data is available. The DMA Controller responds to this request with both a $\overline{DACK}$ = 0 (DMA Acknowledge) and a RD = 0 (Read signal). When the DMA Acknowledge signal goes low ($\overline{DACK}$ = 0) then the DMA Request is reset (DRQ = 0). If a Write Command has been programmed then a $\overline{WR}$ signal will appear instead of $\overline{RD}$. After the Execution Phase has been completed (Terminal Count has occurred) then an Interrupt will occur (INT = 1). This signifies the beginning of the Result Phase. When the first byte of data is read during the Result Phase, the Interrupt is automaticaily reset (INT = 0).

It is important to note that during the Result Phase all bytes shown in the Command Table must be read. The Read Data Command, for example, has seven bytes of data in the Result Phase. All seven bytes must be read in order to successfully complete the Read Data Command. The UM8272A/A-4 will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the Result Phase.

The UM8272A/A-4 contains five Status Registers. The Main Status Register mentioned above may be read by the processor at any time. The other four Status Registers (ST0, ST1, ST2, and ST3) are only available during the Result Phase, and may be read only after successfully completing a command. The particular command which has been executed determines how many of the Status Registers will be read.

The bytes of data which are sent ot the UM8272A/A-4 to form the Command Phase, and are read out of the UM8272A/A-4 in the Result Phase, must occur in the order shown in Table 3. The Command Code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result Phases are allowed. After the last byte of data in the Command Phase is sent to the UM8272A/A-4, the Execution Phase automatically starts. In a similar fashion, when the last byte of data is read out in the Result Phase, the command is automatically ended and the UM8272A/A-4 is ready for a new command. A command may be aborted by simply sending a Terminal Count signal to pin 16 (TC=1). This is a convenient means of ensuring that the processor can always get the UM8272A/A-4's attention even if the disk system hangs up in an abnormal manner.

Command Symbol Description

Symbol	Name	Description
A0	Address Line 0	A0 controls selection of Main Status Register (A0 = 0) or Data Register (A0 = 1).
C	Cylinder Number	C stands for the current selected Cylinder (track) number 0 through 76 of the medium.
D	Data	D stands for the data pattern which is going to be written into a sector.
D_7-D_0	Data Bus	8-bit Data Bus, where D_7 stands for the most significant bit, and D_0 stands for the least significant bit.
DTL	Data Length	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the Sector.
EOT	End of Track	EOT stands for the final sector number on a Cylinder. During Read or Write operation FDC will stop data transfer after a sector number equal to EOT.
GPL	Gap Length	GPL stands for the length of Gap 3. During Read/Write commands this value determines the number of bytes that VCOs will stay low after two CRC bytes. During Format command it determines the size of Gap 3.
H	Head Address	H stands for head number 0 or 1, as specified in ID field.
HD	Head	HD stands for a selected head number 0 or 1 and controls the polarity of pin 27. (H = HD in all command words.)
HLT	Head Load Time	HLT stands for the head load time in the FDD (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time	HUT stands for the head unload time after a read or write operation has occurred (16 to 240 ms in 16 ms increments).
MF	FM or MFM Mode	If MF is low, FM mode is selected, and if it is high, MFM mode is selected.
MT	Multi-Track	If MT is high, a multi-track operation is to be performed. If MT = 1 after finishing Read/Write operation on side 0, FDC will automatically start searching for sector 1 on side 1.
N	Number	N stands for the number of data bytes written in Sector.
NCN	New Cylinder Number	NCN stands for a new Cylinder number which is going to be reached as a result of the Seek operation. Desired position of Head.
ND	Non-DMA Mode	ND stands for operation in the Non-DMA Mode.
PCN	Present Cylinder Number	PCN stands for the Cylinder number at the completion of SENSE INTERRUPT STATUS Command. Position of Head at present time.
R	Record	R stands for the Sector number which will be read or written.
R/W	Read/Write	R/W stands for either Read (R) or Write (W) signal.
SC	Sector	SC indicates the number of Sectors per Cylinder.
SK	Skip	SK stands for Skip Deleted Data address mark.
SRT	Step Rate Time	SRT stands for the Stepping Rate for the FDD. (1 to 16 ms in 1 ms increments.) Stepping Rate applies to all drives, (F = 1 ms, E = 2 ms, etc.)
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	ST 0-3 stands for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by A_0 = 0); ST 0-3 may be read only after a command has been executed and contain information relevant to that particular command.
STP		During a Scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); and if STP = 2, then alternate sectors are read and compared.
US0, US1	Unit Select	US stands for a selected drive number 0 or 1.

Table 3. UM8272A/A-4 Command Set

PHASE	R/W	DATABUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
READ A TRACK										
Command	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
READ DELETED DATA										
Command	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information Prior to Command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	OTL								
Execution										Data-transfer between the FDD and main system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
WRITE DATA										
Command	W	MT	MF	0	0	0	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information Prior to Command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the main system and FDD.
Result	R	ST 0								Status information after Command execution.
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								
WRITE DELETED DATA										
Command	W	MT	MF	0	0	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information Prior to Command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main system.
Result	R	ST 0								Status information after Command execution.
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

PHASE	R/W	DATABUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
READ A TRACK										
Command	W	0	MF	SK	0	0	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main system. FDC reads all data fields from index hole to EOT.
Result	R	ST 0								Status information after Command execution.
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								
READ ID										
Command	W	0	MF	0	0	1	0	1	0	Commands
	W	X	X	X	X	X	HD	US1	US0	
Execution										The first correct ID information on the Cylinder is stored in Data Register.
Result	R	ST 0								Status information after Command execution.
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information read during Execution Phase from Floppy Disk.
	R	H								
	R	R								
	R	N								
FORMAT A TRACK										
Command	W	0	MF	0	0	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	N								Bytes/Sector
	W	SC								Sectors/Track
	W	GPL								Gap 3
	W	D								Filler Byte
Execution										FDC formats an entire track.
Result	R	ST 0								Status information after Command execution. In this case, the ID information has no meaning.
	R	ST 1								
	R	ST 2								
	R	C								
	R	H								
	R	R								
	R	N								
SCAN EQUAL										
Command	W	MT	MF	SK	0	0	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information Prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data compared between the FDD and main system.
Result	R	ST 0								Status information after Command execution.
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

Note: 1 A0 should equal binary 1 for all operations.
2 X = Immaterial; usually made to equal binary 0.

Table 3. UM8272A/A-4 Command Set (Continued)

PHASE	R/W	DATABUS D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	REMARKS
SCAN LOW OR EQUAL			
Command	W	MT MF SK 1 1 0 0 1	Command Codes
	W	X X X X X HD US1 US0	
	W	C	Sector ID information prior Command execution.
	W	H	
	W	R	
	W	N	
	W	EOT	
	W	GPL	
	W	STP	
Execution			Data compared between the FDD and main system
Result	R	ST 0	Status information after Command execution. Sector ID information after Command execution.
	R	ST 1	
	R	ST 2	
	R	C	
	R	H	
	R	R	
	R	N	
SCAN HIGH OR EQUAL			
Command	W	MT MF SK 1 1 1 0 1	Command Codes
	W	X X X X X HD US1 US0	
	W	C	Sector ID information prior Command execution.
	W	H	
	W	R	
	W	N	
	W	EOT	
	W	GPL	
	W	STP	
Execution			Data compared between the FDD and main system.
Result	R	ST 0	Status information after Command execution. Sector ID information after Command execution.
	R	ST 1	
	R	ST 2	
	R	C	
	R	H	
	R	R	
	R	N	

PHASE	R/W	DATABUS D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	REMARKS
RECALIBRATE			
Command	W	0 0 0 0 0 1 1 1	Command Codes
	W	X X X X X 0 US1 US0	
Execution			Head retracted to Track 0
SENSE INTERRUPT STATUS			
Command	W	0 0 0 0 1 0 0 0	Command Codes
Result	R	ST 0	Status information at the end of seek-operation about the FDC
	R	PCN	
SPECIFY			
Command	W	0 0 0 0 0 0 1 1	Command Codes
	W	SRT → HUT	
	W	HLT → ND	
SENSE DRIVE STATUS			
Command	W	0 0 0 0 0 1 0 0	Command Codes
	W	X X X X X HD US1 US0	
Result	R	ST 3	Status information about FDD
SEEK			
Command	W	0 0 0 0 1 1 1 1	Command Codes
	W	X X X X X HD US1 US0	
	W	NCN	
Execution			Head is positioned over proper Cylinder on Diskette
INVALID			
Command	W	Invalid Codes	Invalid Command Codes (NoOp – FDC goes into Standby State)
Result	R	ST 0	ST 0 = 80 (16)

Polling Feature of the UM8272A/A-4

After power-up RESET, the Drive Select Lines DS0 and DS1 will automatically go into a polling mode. In between commands (and between step pulses in the SEEK command) the UM8272A/A-4 polls all four FDDs looking for a change in the Ready line from any of the drives. If the Ready line changes state (usually due to a door opening or closing) then the UM8272A/A-4 will generate an interrupt. When Status Register 0 (ST0) is read (after Sense Interrupt Status is issued), Not Ready (NR) will be indicated. The polling of the Ready line by the UM8272A/A-4 occurs continuously between instructions, thus notifying the processor which drives are on or off line. Approximate scan timing is shown in Table 4.

Table 4. Scan Timing

DS_1	DS_0	APPROXIMATE SCAN TIMING
0	0	220μS
0	1	220μS
1	0	220μS
1	1	440μS

Command Descriptions

During the Command Phase, the Main Status Register must be polled by the CPU before each byte is written into the Data Register. The DIO (DB_6) and RQM (DB_7) bits in the Main Status Register must be in the "0" and "1" states respectively, before each byte of the command may be written into the UM8272A/A-4. The beginning of the execution phase for any of these commands will cause DIO and RQM to switch to "1" and "0" respectively.

READ DATA

A set of nine (9) byte words is required to place the FDC into the Read Data Mode. After the Read Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head setting time (defined in the Specify Command), and begins reading ID address Marks and ID fields. When the current sector number ("R") stored in the ID Register (IDR) compares with the sector number read off the diskette, the FDC outputs data (from the Data field) byte-by-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a "Multi-Sector Read Operation." The Read Data Command must

be terminated by the receipt of a Terminal Count signal. Upon receipt of this signal, the FDC stops outputing data to the processor, but will continue to read data from the current sector, checking CRC (Cyclic Redundancy Count) bytes, and then at the end of the sector terminating the Read Data Command.

The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track), MFM (MFM/FM), and N (Number of Bytes/Sector). Table 5 shows the Transfer Capacity. The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be

Table 5. Transfer Capacity

Multi-Track MT	MFM/FM MF	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskette
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	or 26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	or 15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	or 8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

transferred starting at Sector 1 Side 0 and completing at Sector L Side 1 (Sector L = last sector on the side). Note: This function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a Sector, the data beyond DTL in the Sector is not sent to the Data Bus. The FDC reads (internally) the complete Sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read Operation. When N is non-zero, then DTL has no meaning and should be set to OFFH.

At the completion of the Read Data Command, the head is not unloaded until after Head Unload Time Interval (specified in the Specify Command) has elapsed. If the processor issues another command before the head unloads, then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another. If the FDC detects the Index Hole twice without finding the right sector, (indicated in "R"), then the FDC sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the DE (Data Error) flag in Status Register 1 to a 1 (high), and if a CRC error occurs in the Data Field the FDC also sets the DD (Data Error in Data Field) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

If the FDC reads a Deleted Data Address Mark off the diskette, and the SK bit (bit D5 in the first Command Word) is not set to 0, then the FDC sets the CM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command, after reading all the data in the Sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be served by the processor every 27 μs in the FM Mode, and every

13 μs in the MFM Mode, or the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command.

If the processor terminates a read (or write) operation in the FDC, then the ID Information in the Result Phase is dependent upon the state of the MT bit and EOT byte. Table 6 shows the values for C, H, R, and N, when the processor terminates the Command.

Table 6. ID Information When Processor Terminates Command

MT	EOT	Final Sector Transferred to Processor	ID Information at Result Phase			
			C	H	R	N
0	1A 0F 08	Sector 1 to 25 at Side 0 Sector 1 to 14 at Side 0 Sector 1 to 7 at Side 0	NC	NC	R + 1	NC
	1A 0F 08	Sector 26 at Side 0 Sector 15 at Side 0 Sector 8 at Side 0	C + 1	NC	R = 01	NC
	1A 0F 08	Sector 1 to 25 at Side 1 Sector 1 to 14 at Side 1 Sector 1 to 7 at Side 1	NC	NC	R + 1	NC
	1A 0F 08	Sector 26 at Side 1 Sector 15 at Side 1 Sector 8 at Side 1	C + 1	NC	R = 01	NC
1	1A 0F 08	Sector 1 to 25 at Side 0 Sector 1 to 14 at Side 0 Sector 1 to 7 at Side 0	NC	NC	R + 1	NC
	1A 0F 08	Sector 26 at Side 0 Sector 15 at Side 0 Sector 8 at Side 0	NC	LSB	R = 01	NC
	1A 0F 08	Sector 1 to 25 at Side 1 Sector 1 to 14 at Side 1 Sector 1 to 7 at Side 1	NC	NC	R + 1	NC
	1A 0F 08	Sector 26 at Side 1 Sector 15 at Side 1 Sector 8 at Side 1	C + 1	LSB	R = 01	NC

Note: 1. NC (No Change): The same value as the one at the beginning of command execution.
2. LSB (Least Significant Bit): The least significant bit of H is complemented.

WRITE DATA

A set of nine (9) bytes is required to set the FDC into the Write Data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading the ID Fields. When the current sector number ("R"), stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC takes data from the processor byte by byte via the data bus, and outputs it to the FDD. After writing data into the current sector, the Sector Number stored in "R" is incremented by one, and the next data field is written into. The FDC continues this "Multi-Sector Write Operation" until the issuance of a Terminal Count-signal. If a Terminal Count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written then the remainder of the data field is filled with 00 (zeros).

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (Incorrect CRC) in one of the ID Fields, it sets the DE (Data Error) flag of Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

The Write Command operates in much the same manner as the Read Command. The Following items are the same (refer to the Read Data Command for details):

- Transfer Capacity
- EN (End of Cylinder) Flag
- ND (No Data) Flag
- Head load Time Interval
- ID Information when the processor terminates command (see Table 6)
- Definition of DTL when N = 0 and when N ≠ 0

In the Write Data mode, data transfers between the processor and FDC must occur every 31 μs in the FM mode, and every 15 μs in the MFM mode. If the time interval between data transfers is longer than this the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Write Data Command.

For mini-floppies, multiple track writes are usually not permitted. This is because the turn-off time of the erase head coils the head switches tracks before the erase head turns off. Therefore the system should typically wait 1.3 ms before attempting to step or change sides.

WRITE DELETED DATA

This command is the same as the Write Data Command except a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark.

READ DELETED DATA

This command is the same as the Read Data Command except that when the FDC detects a Data Address Mark at the beginning of a Data Field with the SK = 0 (low), it will read all the data in the sector and set the CM flag in Status Register 2 to a 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the Data Address Mark and reads the next sector.

READ A TRACK

This command is similar to the READ DATA Command except that the entire data field is read continuously from each of the sectors of a track. Immediately after encountering the INDEX HOLE the FDC starts reading all data fields on the track as continuous blocks of data. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR, and sets the ND flag of Status Register 1 to a 1 (high) if there is no comparison. Multitrack or skip operations are not allowed with this command.

This command will terminate when EOT number of sectors has been read. If the FDC does not find an ID Address Mark on the diskette after it encounters the index hole for the second time, it sets the MA (missing address mark) flag in Status Register 1 to a 1 (high), and terminates the command. (Status Register 0 has bits 7 and 6 set to 0 and 1 respectively.)

READ ID

The READ ID Command is used to give the present position of the recording head. The FDC stores the values from the first ID Field it is able to read. If no proper ID Address Mark is found on the diskette, before the INDEX HOLE is encountered for the second time then the MA (Missing Address Mark) flag in Status Register 1 is set to a 1 (high), and if no data is found then the ND (No Data) flag is also set in Status Register 1 to a 1 (high) and the command is terminated.

FORMAT A TRACK

The Format Command allows an entire track to be formatted. After the index hole is detected, Data is written on the Diskette: Gaps, Address Marks, ID Fields and Data Fields, all per the IBM System 34 (Double Density) or System 3740 (Single Density) Formats are recorded. The particular format which will be written is controlled by the values programmed into N: (number of bytes/secter), SC (sectors/cylinder), GPL (Gap Length) and D (Data Pattern). These are supplied by the processor during the Command Phase. The Data Field is filled with the Byte of data stored in D. The ID Field for each sector is supplied by the processor: four data requests per sector are made by the FDC for C (Cylinder Number), H (Head Number), R (Sector Number) and N (Number of Bytes/Sector). This allows the diskette to be formatted with nonsequential sector numbers, if desired.

After formatting each sector, the processor must send new values for C, H, R, and N to the UM8272A/A-4 for each sector on the track. The contents of the R Register are incremented by one after each sector is formatted: the R register contains a value of R + 1 when it is read during the Result Phase. This incrementing and formatting continues for the whole track until the FDC encounters the index hole for the second time, whereupon it terminates the command.

If a FAULT signal is received from the FDD at the end of a write operation, then the FDC sets the EC flag of status Register 0 to a 1 (high), and terminates the command after setting bits 7 and 6 of Status Register 0 to 0 and 1 respectively. Also the loss of a READY signal at the beginning of a command execution phase causes command termination.

Table 7 shows the relationship between N, SC, and GPL for various sector sizes:

Table 7. Sector Size Relationships

	8" STANDARD FLOPPY					5¼" MINI FLOPPY			
Format	**Sector Size**	**N**	**SC**	**GPL[1]**	**GPL[2]**	**Remarks**	**Sector Size**	**N SC**	**GPL[1]**	**GPL[2]**
FM Mode	128 bytes/Sector	00	1A	07	1B	IBM Diskette 1D	128 bytes/Sector	00 12	07	09
	256	01	0F	0E	2A		128	00 10	10	19
	512	02	06	1B	3A	IBM Diskette 2D	256	01 06	18	30
	1024	03	04	47	8A		512	02 04	46	87
	2048	04	02	C8	FF		1024	03 02	D8	FF
	4096	05	01	C8	FF		2048	04 01	C8	FF
MFM Mode	256	01	1A	0E	36	IBM Diskette 2D	256	01 12	0A	0C
	512	02	0F	1B	54		256	01 10	20	32
	1024	03	08	35	74	IBM Diskette 2D	512	02 08	2A	50
	2048	04	04	99	FF		1024	03 04	80	F0
	4096	05	02	C8	FF		2048	04 02	CB	FF
	8192	06	01	C8	FF		4096	05 01	C8	FF

Notes: 1. Suggested values of GPL in Read or Write Commands to avoid splice point between data field and ID field of contiguous sections.
2. Suggested values of GPL in formal command.

Storage

During the Command Phase of the Seek operation the FDC is in the FDC BUSY state, but during the Execution Phase it is in the NON-BUSY state. While the FDC is in the NON-BUSY state, another Seek Command may be issued, and in this manner parallel seek operations may be done on up to 4 Drives at once.

If an FDD is in a NOT READY state at the beginning of the command execution phase or during the seek operation, the NR (NOT READY) flag is set in Status Register 0 to a 1 (high), and the command is terminated.

Note that the UM8272A/A-4 Read and Write Commands do not have implied Seeks. Any R/W command should be preceded by: 1) Seek Command, 2) sense Interrupt Status, and 3) Read ID.

RECALIBRATE

This command causes the read/write head within the FDD to retract to the Track 0 position. The FDC clears the contents of the PCN counter, and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is low, the Direction signal remains 1 (high) and Step Pulses are issued. When the Track 0 signal goes high, the SE (SEEK END) flag in Status Register 0 is set to a 1 (high) and the command is terminated. If the Track 0 signal is still low after 77 Step Pulses have been issued, the FDC sets the SE (SEEK END) and EC (EQUIPMENT CHECK) flags of Status Register 0 both to 1 (high), and terminates the command.

The ability to overlap RECALIBRATE Commands to multiple FDDs, and the loss of the READY signal, as described in the SEEK Command, also applies to the RECALIBRATE Command.

SENSE INTERRUPT STATUS

An Interrupt signal is generated by the FDC upon one of the following conditions:

1. Upon entering the Result Phase of:
   a. Read Data Command
   b. Read a Track Command
   c. Read ID Command
   d. Read Deleted Data Command
   e. Write Data Command
   f. Format a Cylinder Command
   g. Write Deleted Data Command
   h. Scan Commands
2. Ready Line of FDD changes state
3. End of Seek or Recalibrate Command
4. Execution Phase in the NON-DMA Mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. However, interrupts caused by reasons 2 and 3 may be uniquely identified with the aid of the Sense Interrupt Status Command. This command when issued resets the interrupt signal and via bits 5, 6, and 7 of Status Register 0 and identifies the cause of the interrupt.

Neither the Seek nor Recalibrate Command have a Result Phase. Therefore, it is mandatory to use the Sense interrupt Status Command after these commands to effectively terminate them and to provide verification of the head position (PCN).

Table 8. Seek, Interrupt Codes

Seek End Bit 5	Interrupt Code		CAUSE
	Bit 6	Bit 7	
0	1	1	Ready Line changed state, either polarity
1	0	0	Normal Termination of Seek or Recalibrate Command
1	1	0	Abnormal Termination of Seek or Recalibrate Command

SPECIFY

The Specify Command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution Phase of one of the Read/Write Commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (01 = 16 ms, 02 = 32 ms . . . OF = 240 ms). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and when the Read/Write operation starts. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms . . . . FE = 254 ms).

The step rate should be programmed for 1 ms longer than the minimum time required by the drive.

The time intervals mentioned above are a direct function of the clock (CLK on pin 19). Times indicated above are for an 8 MHz clock; if the clock is 4 MHz (mini-floppy application) then all time intervals are increased by a factor of 2.

The choice of DMA or NON-DMA operation is made by the ND (NON-DMA) bit. When this bit is high (ND = 1) the NON-DMA mode is selected, and when ND = 0 the DMA mode is selected.

SENSE DRIVE STATUS

This command may be used by the processor whenever it wishes to obtain the status of the FDDs. Status Register 3 contains the Drive Status information.

INVALID

If an invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command. No interrupt is generated by the UM8272A/A-4 during this condition. Bit 6 and bit 7 (DIO and RQM) in the Main Status Register are both high (1) indicating to the processor that the UM8272A/A-4 is in the Result Phase and the contents of Status Register 0 (ST0) must be read. When the processor reads Status Register 0 it will find an 80H indicating an invalid command was received.

A Sense interrupt Status Command must be sent after a Seek or Recalibrate interrupt; otherwise the FDC will consider the next command to be an invalid Command.

In some applications the user may wish to use this command as a No-Op command, to place the FDC in a standby or no operation state.

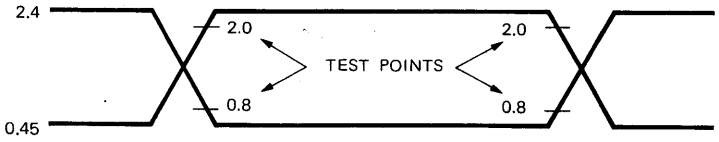
Table 9. Status Registers

Bit No.	Name	Symbol	Description
	STATUS REGISTER 0		
D_7	Interrupt Code	IC	$D_7 = 0$ and $D_6 = 0$ Normal Termination of Command, (NT). Command was completed and properly executed.
D_6			$D_7 = 0$ and $D_6 = 1$ Abnormal Termination of Command, (AT). Execution of Command was started, but was not successfully completed.
			$D_7 = 1$ and $D_6 = 0$ Invalid Command issue (IC). Command which was issued was never started.
			$D_7 = 1$ and $D_6 = 1$ Abnormal Termination because during command execution the ready signal from FDD changed state.
D_5	Seek End	SE	When the FDC completes the SEEK Command, this flag is set to 1 (high).
D_4	Equipment Check	EC	If a fault Signal is received from the FDD, or if the Track 0 Signal fails to occur after 77 Step Pulses (Recalibrate Command) then this flag is set.
D_3	Not Ready	NR	When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to Side 1 of a single sided drive, then this flag is set.
D_2	Head Address	HD	This flag is used to indicate the state of the head at Interrupt.
D_1	Unit Select 1	US 1	These flags are used to indicate a
D_0	Unit Select 0	US 0	Drive Unit Number at Interrupt
	STATUS REGISTER 1		
D_7	End of Cylinder	EN	When the FDC tries to access a Sector beyond the final Sector of a Cylinder, this flag is set.
D_6			Not used. This bit is always 0 (low).
D_5	Data Error	DE	When the FDC detects a CRC error in either the ID field or the data field, this flag is set.
D_4	Over Run	OR	If the FDC is not serviced by the main systems during data transfers, within a certain time interval, this flag is set.
D_3			Not used. This bit is always 0 (low).
D_2	No Data	ND	During execution of READ DATA, WRITE DELETED DATA or SCAN Command, if the FDC cannot find the Sector specified in the IDR Register, this flag is set.
			While executing the READ ID Command, if the FDC cannot read the ID field without an error, then this flag is set.
			During the execution of the READ A Cylinder Command, if the starting sector cannot be found, then this flag is set.

Bit No.	Name	Symbol	Description
	STATUS REGISTER 1 (CONT.)		
D_1	Not Writable	NW	During execution of WRITE DATA, WRITE DELETED DATA or Format Cylinder Command, if the FDC detects a write protect signal from the FDD, then this flag is set.
D_0	Missing Address Mark	MA	If the FDC cannot detect the ID Address Mark after encountering the Index hole twice, then this flag is set.
			If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. Also at the same time, the MD (Missing Address Mark in Data Field) of Status Register 2 is set.
	STATUS REGISTER 2		
D_7			Not used. This bit is always 0 (low.)
D_6	Control Mark	CM	While executing the READ DATA or SCAN Command, if the FDC encounters a Sector which contains a Deleted Data Address Mark, this flag is set.
D_5	Data Error in Data Field	DD	If the FDC detects a CRC error in the data field then this flag is set.
D_4	Wrong Cylinder	WC	This bit is related to the ND bit, and when the contents of C on the medium is different from that stored in the IDR, this flag is set.
D_3	Scan Equal Hit	SH	During execution of the SCAN Command, if the condition of "equal" is satisfied, this flag is set.
D_2	Scan Not Satisfied	SN	While executing the SCAN Command, if the FDC cannot find a Sector on the cylinder which meets the condition, then this flag is set.
D_1	Bad Cylinder	BC	This bit is related to the ND bit, and when the content of C on the medium is different from that stored in the IDR and the content of C is FF, then this flag is set.
D_0	Missing Address Mark in Data Field	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.
	STATUS REGISTER 3		
D_7	Fault	FT	This bit is used to indicate the status of the Fault signal from the FDD.
D_6	Write Protected	WP	This bit is used to indicate the status of the Write Protected signal from the FDD.
D_5	Ready	RDY	This bit is used to indicate the status of the Ready signal from the FDD.
D_4	Track 0	T0	This bit is used to indicate the status of the Track 0 signal from the FDD.
D_3	Two Side	TS	This bit is used to indicate the status of the Two Side signal from the FDD.
D_2	Head Address	HD	This bit is used to indicate the status of Side Select signal to the FDD.
D_1	Unit Select 1	US 1	This bit is used to indicate the status of the Unit Select 1 signal to the FDD.
D_0	Unit Select 0	US 0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD.

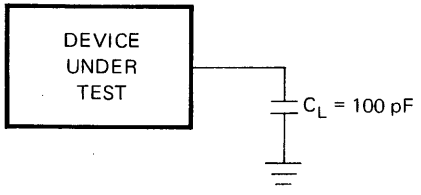
AC Testing Input, Output Waveform

INPUT/OUTPUT



A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0".

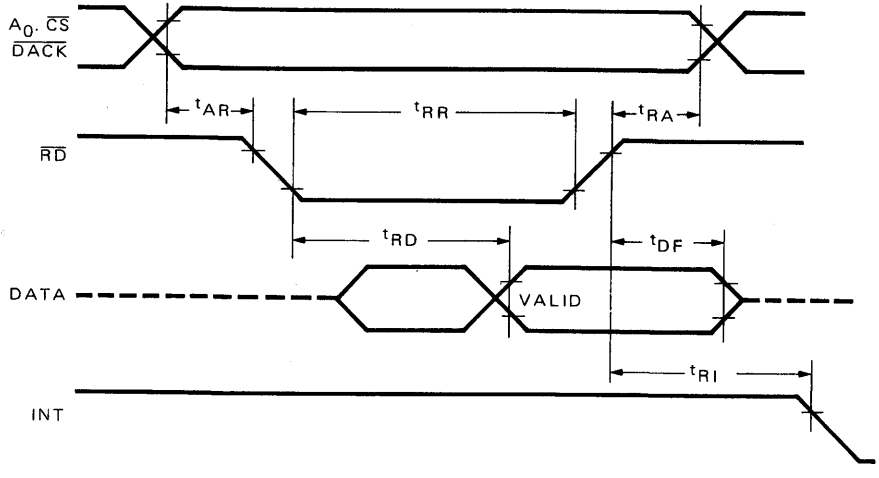
AC Testing Load Circuit



C_L INCLUDES JIG CAPACITANCE

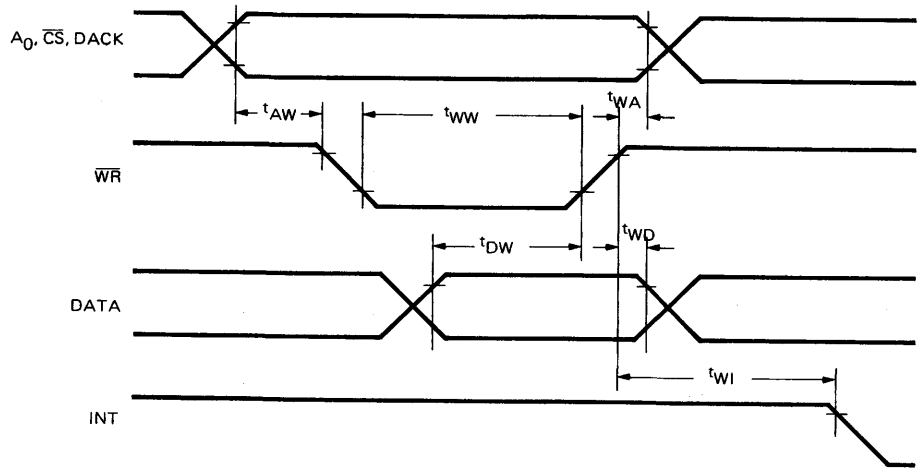
Timing Waveforms

PROCESSOR READ OPERATION

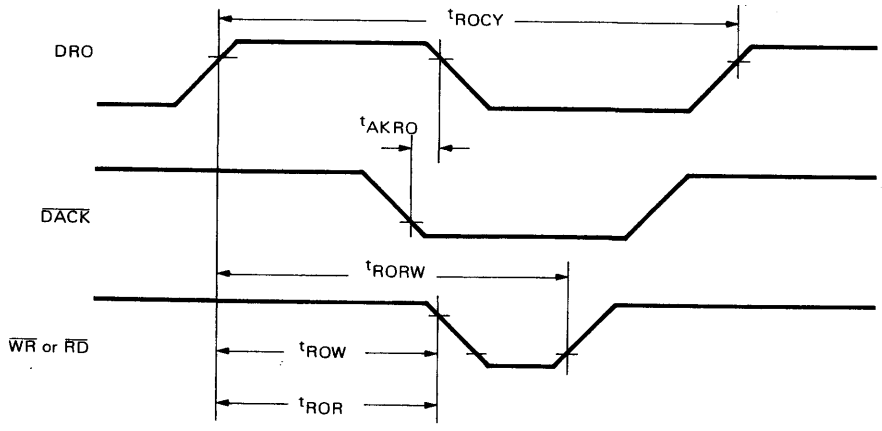


Timing Waveforms (Continued)

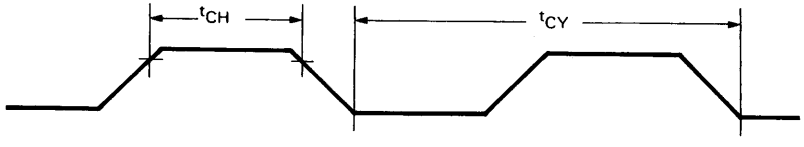
PROCESSOR WRITE OPERATION



DMA OPERATION

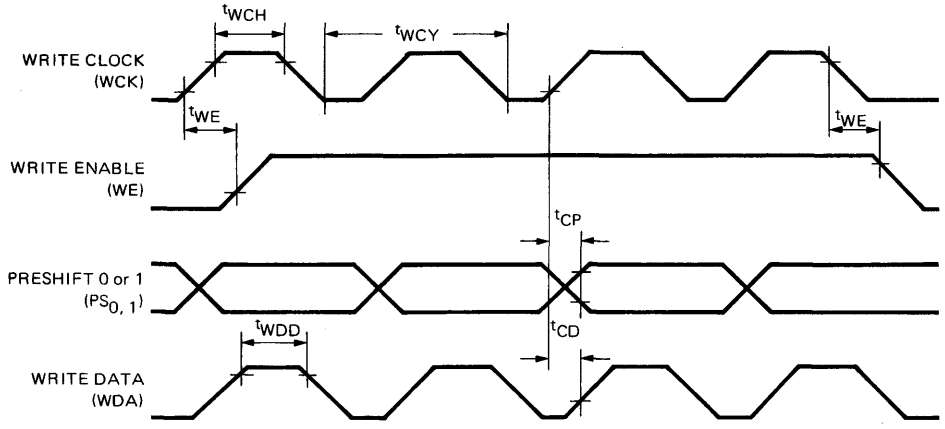


CLOCK TIMING



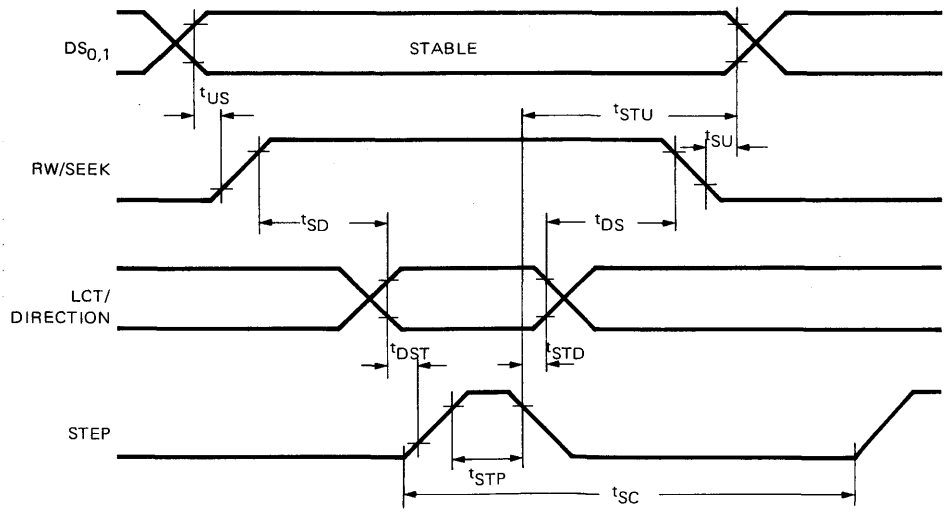
Timing Waveforms (Continued)

FDD WRITE OPERATION

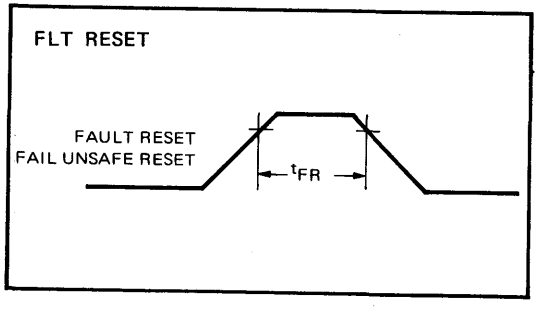


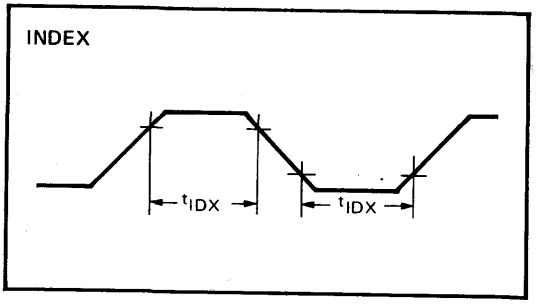
	PRESHIFT 0	PRESHIFT 1
NORMAL	0	0
LATE	0	1
EARLY	1	0
INVALID	1	1

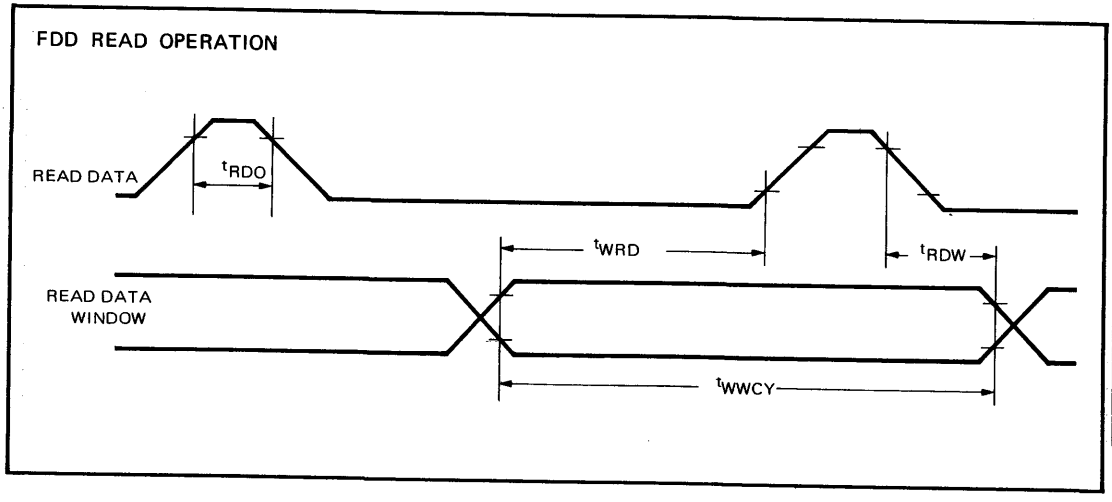
SEEK OPERATION

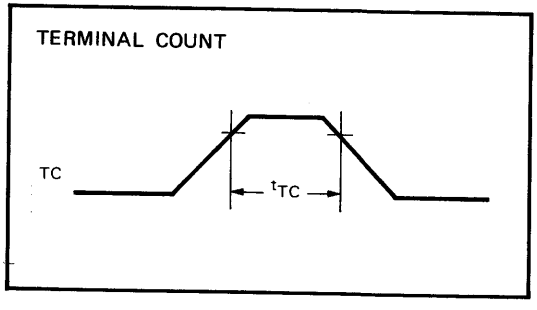


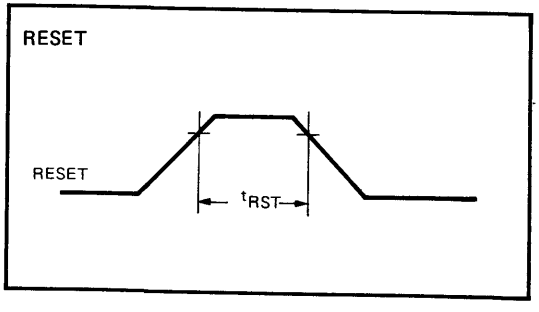
Timing Waveforms (Continued)











Ordering Information

Part Number	Operational Clock	Package
UM8272A – 4	4 MHz	40L DIP
UM8272A	8 MHz	40L DIP

UM83C001

Hard Disk Controller

Features

- Serializer-deserializer
- Programmable track format
- External drive select and head select registers for expandability
- Internal phase detector for phase lock oscillator
- Interface options: ST-506, ST-412, ST-412HP, ESDI, FLOPPY, and QIC-36 TAPE
- Sector options: SOFT, HARD, ESDI ADDRESS MARKS, ESDI BYTE and ESDI BYTE CLOCKS
- Recording options: UNENCODED, FM, MFM or RLL
- Error checking and correcting options: ECC or CRC
- Write data options: PULSE, NRZ or NRZI
- Read data options: PULSE, NRZ or NRZI
- TTL compatible inputs and outputs. Outputs drive 8 LSTTL loads

General Description

The UMC Hard Disk Controller UM83C001 is a CMOS LSI device which performs a majority of the functions for controlling floppy drives, Winchester drives and QIC-36 streaming tape drives. The following is a brief list of its capabilities:

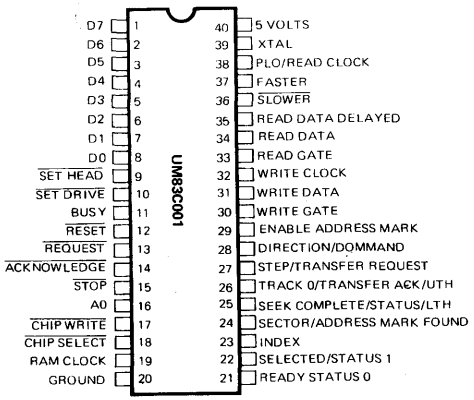
Interface Options

ST-506 (non-buffered seek Winchesters)
ST-412 (buffered seek Winchesters)
ST-412HP (10 mbos buffered seek Winchesters)
ESDI STEP/SERIAL MODES (10 mbos Winchesters)
SA-450 (5" and 3" floppies)
SA800/850 (8" floppies)
QIC-36 (streaming tape drives)

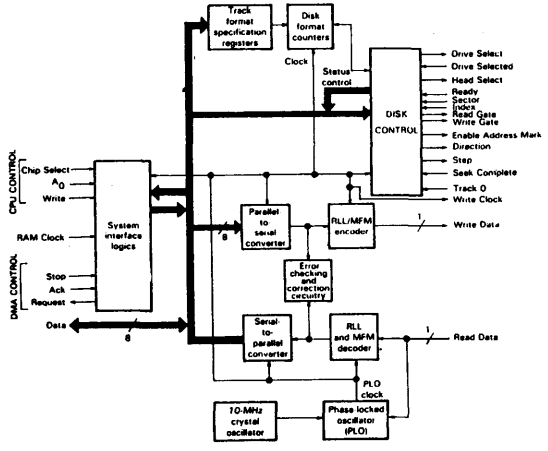
Sector Options

SOFT-SECTORING (floppy and Winchester)
HARD-SECTORING (floppy and Winchester)
ESDI ADDRESS MARKS (ESDI drives)
ESDI BYTE CLOCKS (ESDI drives)

Pin Configuration



Block Diagram



Recording Codes

UNENCODED (for ESDI drives)
FM (Frequency Modulation)
MFM (Modified Frequency Modulation)
RLL (Run Length Limited)

Error Checking

CRC (CCITT CRC-16)
ECC (4 byte, corrects 11 contiguous erroneous bits)

Data Options

NRZ (non-return to zero)
NRZI (non-return to zero inverted)
PULSE

Absolute Maximum Ratings*

Power Supply Voltage, V_{DD} . . . . . −0.5 to +7.0V
Input Voltage, V_I . . . . . −0.5V to V_{DD} +0.5V
Operating Temperature, T_{OPT} . . . . . −40 to +85°C
Storage Temperature, T_{STG} . . . . . −65 to +150°C

Track Format

Extensive control over the track format is provided by allowing the length of fields and content of ADDRESS MARKS and identifier bytes, etc. to be programmed into registers.

There are 23 registers related to TRACK FORMAT inside the UM83C001 (Refer to Figure 1). 18 of these registers contain lengths of fields within a track. Others contain "content" information. Length fields are written with length-1 giving them a range of 1 to 256 inclusive. The Data Field Length Register is 2 bytes yielding a maximum data field length of 65, 536 bytes.

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

(T_A = 0 to +70°C, V_{DD} = 5V ±5%)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Power Supply Voltage	V_{DD}	4.5	5	5.5	V	
Input Voltage	V_I	0		V_{DD}	V	
Low-level Input Voltage	V_{IL}	0		0.8	V	TTL Level*
High-level Input Voltage	V_{IH}	2.0		V_{DD}	V	TTL Level*
Input Rise Fall Times	t_R, t_F	0		10	us	

DC Electrical Characteristics

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Static Current	I_L		0.1	200	μA	$V_I = V_{DD}$ or GND
Dynamic Current	I_{DD}		4		μA	1 MHz/cell
Input Current	I_I	0.1		10	μA	$V_I = V_{DD}$ ro GND
Low-level Output Current	I_{OL}	3.2	9		mA	V_{OL} = 0.4V
High-level Output Current	I_{OH}	1	3		mA	$V_{OH} = V_{DD} - 0.4V$
Low-level Output Voltage	V_{OL}			0.1	V	I_O = 0
High-level Output Voltage	V_{OH}	$V_{DD} - 0.1$			V	I_O = 0

AC Characteristics

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Maximum Operating Frequency	f_{MAX}	DC		50	MHz	
Output Rise Time	t_R		8		ns	C_L = 15 pF
Output Fall Time	t_F		4		ns	C_L = 15 pF

Track Format

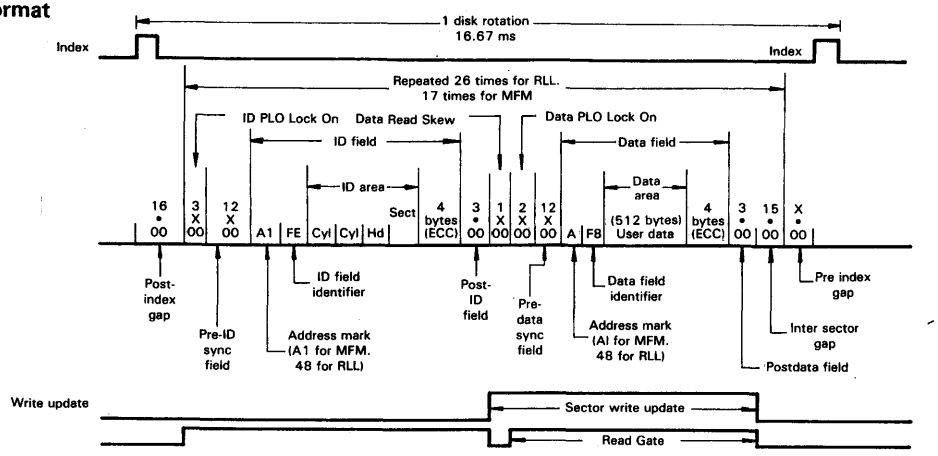


Figure 1. UM83C001 Track Format Diagram

HEX Register Address	Function	*** Range (In Bytes)
00	POST INDEX GAP	1 – 256
01	ID PLO LOCK-ON	1 – 64
02	PRE ID	1 – 64
03	ID ADDRESS MARK	1 – 4
04	FE BYTE	1 (fixed)
05	ID	1 – 16
06	ID ECC	1 – 4
07	POST ID	1 – 4
08	DATA READ SKEW	1 – 64
09	DATA PLO LOCK-ON	1 – 64
A	PRE DATA	1 – 64
B	DATA ADDRESS MARK	1 – 4
C	F8 BYTE	1 (fixed)
D	LOW BYTE	
	DATA FIELD	1 – 65, 536
0E	HIGH BYTE	
0F	DATA ECC	1 – 4
10	POST DATA	1 – 4
11	INTER-RECORD GAP	1 – 256
12	SECTORS PER TRACK	1 – 256

*** SET REGISTERS TO n–1 TO GET n BYTE LENGTH

Table 1. Programmable Format Variables

UM83C001 and UM83C002 used with an 8086/8088 System

Figure 2 illustrates the use of the UMC chip set in a typical 8088 or 8086 system. The RAM BUFFER CONTROLLER (UM83C002) directly accepts the multiplexed address and data lines from the 8086/8088. ADDRESS LATCH ENABLE (+ALE) is used to latch the address lines internally in the controller. These 16 address lines are then multiplexed down to 8 lines for use with dynamic RAMs.

When the processor does a READ or a WRITE to RAM, a PROCESSOR REQUEST is sent to the BUFFER CONTROLLER. If the RAM is currently doing a DMA read or write or a refresh, the processor will be told to wait by dropping the READY line. As soon as RAM is available, the PROCESSOR REQUEST will be acknowledged and the processor will make its memory access. Whenever the RAM is being accessed, the IO/M line will be low. If more than 64 K bytes of RAM is used, bank selects would be decoded from the high order address bits (A16 – A19).

I/O reads and writes for the DISK CONTROLLER also go through the RAM DATA BUS. Hence an I/O write to the DISK CONTROLLER occurs when the IO/M line is high, the DT/R line is high and CHIP SELECT is low.

Multi-Sector Reads and Writes

The UMC DISK CONTROLLER (UM83C001) has the capability of doing multiple sector reads and writes. The use of this capability greatly improves system performance.

On a multi-sector read, data is transferred from disk to memory beginning at the first addressed sector. Only data bytes are transferred. Identifier bytes and ECC are checked but not transferred. At the end of the first sector, the sector number is incremented by one; the sector transfer count is decremented by one; and the next sector is read and transferred to memory. This process continues until the sector count goes to zero; the end of the track is reached; or an error occurs.

When doing single sector reads and writes, the host computer system cannot respond quickly enough to read physically sequential sectors on the disk. Consequently, most hard disks will be formatted with an interleave factor of anywhere from 4 to 12. What this means is that sector 0 will be recorded right after the index pulse and that sector 1 will be recorded anywhere from 4 to 12 sectors "downstream". This interleave gives the host computer time to handle sector 0 and issue a new read in time to catch sector 1 without losing revolutions of the disk. Without the interleave, each single sector read or write would take one full revolution of the disk to accomplish.

On the UMC hard disk chips running RLL code, there are 26 sectors per track of 512 bytes each. Without interleave, it would take 26 revolutions of 16.67 ms each to transfer an entire track using single sector reads or writes. With 9 way interleave, it would take 9 revolutions of 16.67 ms each to transfer this same track using single sector reads and writes. Using multi-sector reads and writes with no interleave, this same track full of data can be transferred in a single revolution of 16.67 ms. The following table compares the times for transfer with and without interleave, and with and without multisector reads and writes.

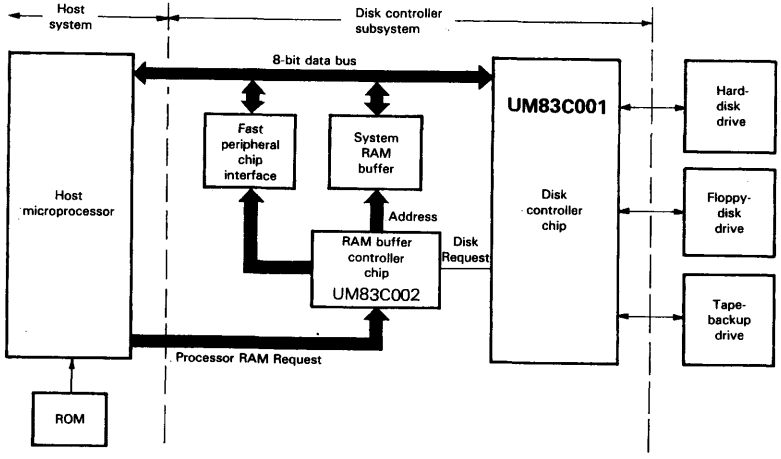


Figure 2. 8086/8088 System with UM83C001 and UM83C002

Track Transfer Times (13,312 Bytes)		Milliseconds	Bytes/Second
SINGLE SECTOR R/W	NO INTERLEAVE	433	30,744
	9-WAY INTERLEAVE	150	88,747
MULTI-SECTOR R/W	NO INTERLEAVE	16.67	798,560
	9-WAY INTERLEAVE	150	88,747

In order to see this improved performance at the system level, the computer operating system must make BASIC INPUT/OUTPUT SYSTEM (BIOS) calls for multi-sector reads and writes. The MSDOS operating system, which is used on the IBM PC and other 8086 and 8088 based microcomputers, does make multi-sector read and write calls for 512 byte sectors. Therefore it is fairly simple to take advantage of the performance increase made possible by multi-sector operations.

The CP/M operating system from Digital Research, that is used on most 8080 and Z80 based microcomputers, does only single sector read and write calls for 128 byte sectors. Getting the increased performance on these machines is still possible although somewhat more difficult. On these machines the BIOS disk driver program must be rewritten so that it does multi-sector reads into a buffer area and then "de-blocks" additional data from the buffer without having to go back to the disk.

The memory that is used as a buffer for de-blocking must be taken away from the memory that is available to the system. On these systems which have only a 64K byte addressing space, this can be a serious disadvantage. One solution to this dilemma is to include a separate RAM buffer within the disk controller itself.

Pin Description

Pin No.	Symbol	Description
1 – 8	DATA LINES D0 – D7 (TO/FROM HOST)	These 8 data lines are used for PROCESSOR and DMA READS and WRITES. They change synchronously with RAM CLOCK rising edge.
9	$\overline{\text{SETHEAD}}$	This signal is used to clock the HEAD ADDRESS, for the drive, into an external HEAD SELECT register. Writing to REGISTER ADDRESS 3D produces a pulse for loading the external head select onto this line.
10	$\overline{\text{SET DRIVE}}$	This signal is the load pulse for the external drive selection register. Writing to REGISTER ADDRESS 3E produces the load pulse on this pin.
11	BUSY	Pin 11 goes high to indicate that the DISK CONTROLLER is busy doing a disk READ or WRITE operation. This pin can be used, if desired, to cause an interrupt for the host processor at the end of disk READ or WRITE operation.
12	$\overline{\text{RESET}}$	The $\overline{\text{RESET}}$ line is intended to be an initial Power On reset line. In order to be efficient, it should go low or be low for a minimum of 100 nanoseconds at the beginning of Power On. This line is a hard reset line and will immediately terminate any disk READ or WRITE operation or any other function and reset the chip to an initial state. It should be used essentially as a Power On RESET and not intended for use as a termination command.

Pin Description (Continued)

Pin No.	Symbol	Description
13	$\overline{\text{REQUEST}}$	The $\overline{\text{REQUEST}}$ line, in conjunction with the $\overline{\text{ACKNOWLEDGE}}$ signal (Pin 14), are the "HANDSHAKING" lines for the DMA data transfer for the chip. The DISK CONTROLLER has a byte of information ready to transfer to RAM or needs a byte of information from RAM to write to the disk when the signal at pin 13 is pulled low. The RAM BUFFER CONTROLLER chip (UM83C002) will respond by driving the $\overline{\text{ACKNOWLEDGE}}$ signal (Pin 14) low and giving the DISK CONTROLLER access to the RAM BUFFER. The DMA transfer operations are run synchronously with the RAM CLOCK signal (Pin 19). The rising edge of the RAM CLOCK pulse defines the cycle boundaries for the RAM.
14	$\overline{\text{ACKNOWLEDGE}}$	This input is driven low to indicate that the requested DMA byte transfer is currently taking place. The $\overline{\text{ACKNOWLEDGE}}$ signal should be a full RAM CLOCK cycle in width. On a disk read operation, the $\overline{\text{ACKNOWLEDGE}}$ signal causes the UM83C001 to gate a byte of data onto the D0 – D7 data lines. On a disk write or verify operation, the $\overline{\text{ACKNOWLEDGE}}$ signal causes the UM83C001 to accept a byte of data from the D0 – D7 data lines. To assure proper "Handshaking" with the $\overline{\text{REQUEST}}$ line, this line must change state while the RAM CLOCK signal is high. If data is not transferred fast enough to keep up with the requirements of the disk or tape, then the OVERRUN/UNDERRUN bit will be set to one (register address 05 bit 1). If this happens, the current disk operation will be terminated at the end of the current sector.
15	$\overline{\text{STOP}}$	This input goes low to indicate the last cycle of a DMA transfer. It is normally driven low by the UM83C002 when the byte counter of the active DMA channel has reached zero. The UM83C001 will continue reading or writing until the end of the current sector is reached and then stop. However, it will not generate any more data requests after the $\overline{\text{STOP}}$ line has been activated. On a sector write, the remainder of the sector will be filled with the last byte that was transferred. This line is ignored unless $\overline{\text{ACKNOWLEDGE}}$ is also low.
16	A0	The UMC DISK CONTROLLER (UM83C001) occupies two I/O port locations selected by the A0 pin. A0 driven low selects the REGISTER ADDRESS POINTER or STATUS REGISTER and A0 driven high selects the READ or WRITE REGISTERS. (REFER TO TABLE 2)
17	$\overline{\text{CHIP WRITE}}$	This input is driven by the CPU to indicate whether a register read or write is to be performed. A low indicates a write; a high indicates a read. This line has meaning ONLY when $\overline{\text{CHIP SELECT}}$ is low; and it is ignored when $\overline{\text{CHIP SELECT}}$ is high.
18	$\overline{\text{CHIP SELECT}}$ ($\overline{\text{CSEL}}$)	The $\overline{\text{CHIP SELECT}}$ line ($\overline{\text{CSEL}}$) is driven low by the processor to read from or write to the registers inside the UM83C001. This signal is intended to be gated by processor's ACKNOWLEDGE signal.
19	RAM CLOCK (RAMCLK)	This clock input synchronizes all CPU and DMA operations of the UM83C001. Cycle boundaries are defined by the rising edge of this clock.

Pin Description (Continued)

Pin No.	Symbol	Description
20	GROUND	Negative Supply
21	READY or STATUS	This input status line is available to the Host Processor at READ REGISTER 04 Bit 6. This line performs no logical function within the UM83C001 and hence the DRIVE READY signal or any other desired status signal may be connected to this pin.
22	SELECTED or STATUS 1	This input status line is available to the Host Processor at READ REGISTER 04 Bit 7. This line performs no logical function within the UM83C001, hence the DRIVE SELECTED signal or any other desired status signal may be connected to this pin.
23	INDEX	The rising edge of this INDEX signal from the selected drive is used to define the beginning of the track. It occurs once per revolution.
24	SECTOR or ADDRESS MARK FOUND	SECTOR For hard sectored drives, the rising edge of this input defines the beginning of sector except sector 0. The beginning of sector 0 is defined by the rising edge of INDEX. ADDRESS MARK FOUND For soft sectored ESDI drives, the rising edge of this ADDRESS MARK FOUND defines the leading edge of every sector except sector 0. The beginning of sector 0 is defined by the rising edge of INDEX.
25	SEEK COMPLETE or STATUS or LTH	SEEK COMPLETE The SEEK COMPLETE input is available to the Host Processor as STATUS REGISTER Bit 2. STATUS For ESDI drives, the serial status line is input at this pin and is available to the Host Processor as STATUS REGISTER Bit 2. LTH (LOWER TAPE HOLE) For QIC-36 tapes the LOWER TAPE HOLE signal is input at this pin and is available to the Host Processor as STATUS REGISTER Bit 2.
26	TRACK 0 or TRANSFER ACK or UTH	TRACK 0 For ST-506 type drives, the TRACK 0 signal is input at this pin and is available to the Host Processor as STATUS REGISTER Bit 1. TRANSFER ACK (ESDI DISK) For ESDI drives, the TRANSFER ACKNOWLEDGE signal is input at this pin and is available to the Host Processor as STATUS REGISTER Bit 1. UTH (UPPER TAPE HOLE – QIC-36 TAPE) For QIC-36 tapes, the UPPER TAPE HOLE signal is input at this pin and is available to the Host Processor as STATUS REGISTER Bit 1.

Pin Description (Continued)

Pin No.	Symbol	Description
27	STEP or TRANSFER REQUEST	STEP This output is the STEP pulses for ST-506 drives. This line goes high whenever a one is written to register 1F bit 0. This line goes low whenever a zero is written to register 1F bit 0. TRANSFER REQUEST This output is used for TRANSFER REQUEST for ESDI drives.
28	DIRECTION or COMMAND	DIRECTION This output is the DIRECTION signal for ST-506 drives and goes high whenever a one is written to register 1E Bit 7. COMMAND This output is the SERIAL COMMAND line for ESDI drives.
29	ENABLE ADDRESS MARK	This signal is required for the ESDI interface. When writing, it causes the ESDI drive to write an address mark on the track. When reading, it causes the ESDI drive to search for an ADDRESS MARK. When the ESDI drive finds an ADDRESS MARK it will activate the ADDRESS MARK FOUND signal at Pin 24. For ESDI drives, WRITE REGISTER 1 should be set to zeros to produce a 3 byte wide ENABLE ADDRESS MARK signal on format writes.
30	WRITE GATE	This signal goes directly to the disk interface and must be HIGH to write data to the disk.
31	WRITE DATA	This signal is the WRITE DATA that goes to the disk drive. This WRITE DATA may be un-encoded or encoded either MFM or RLL and may be either in a pulse format, an NRZ format or NRZI format.
32	WRITE CLOCK	This signal is the code/encoded data rate and is intended for use as a WRITE CLOCK for the ESDI drive interface.
33	READ GATE	This signal indicates that the controller is in an ID for DATA area and is attempting to phase lock onto the READ DATA. This signal is used in the ESDI interface. This signal remains ACTIVE even though the DISK CONTROLLER chip is not actually performing a READ. The BUSY signal (Pin 11) can be used in conjunction with the READ GATE signal to produce a signal enabling an external phase comparator if desired.
34	READ DATA	This signal is the raw DATA pulses that are sent directly from the drive.
35	READ DATA DELAYED	This signal is the same as the READ GATE (Pin 34) with the exception that it is delayed by one half of a READ CODE CYCLE. For example: If you are running MFM data with a code rate of 10 MHz yielding a READ DATA CYCLE of 100 nanoseconds, then the data on this pin would be DELAYED by one half of the 100 nanoseconds equaling 50 nanoseconds. An external delay line is utilized to produce this READ DATA DELAYED signal.

Pin Description (Continued)

Pin No.	Symbol	Description
36 – 37	$\overline{\text{SLOWER}}$ and FASTER	These two signals are used as comparison inputs to an external VOLTAGE CONTROLLED OSCILLATOR so that it can produce the PLO signal at Pin 38.
38	PLO/READ CLOCK	The PHASE LOCK OSCILLATOR (PLO) Input is a READ CLOCK signal which is phase locked onto the READ DATA. The rising edge of the PLO clock should occur at the same time as the rising edge of the READ DATA delayed signal at Pin 35. If the DISK CONTROLLER chip is used to control an ESDI interface drive, the input to this pin would be the READ CLOCK signal coming directly from the ESDI interface.
39	XTAL (Crystal)	This is the crystal oscillator input which is the reference clock for writing to the hard disk. The XTAL frequency should be the code frequency going to the disk. For example: If running at MFM with a 5 megabit disk data rate, the MFM code going to the disk would be at a 10 MHz rate and the XTAL input would be at 10 MHz. When using RLL code with a 7 1/2 megabit disk data rate, the code rate going to the disk would be 15 MHz and the XTAL input would be 15 MHz. For ESDI drives, the +READ CLOCK would be input at this pin.
40	+5 VOLTS	Positive Supply

Register Addresses

Data Lines (D0-D7), in conjunction with the software controlled A0 signal (as an enabling signal), when decoded select either a write or read operation to be performed and the REGISTER ADDRESSES to be utilized. (Table 2 is a chart of the A0 REGISTER ADDRESSES)

		Read	Write
	BIT	STATUS	REGISTER ADDRESS
A0 = 0	7	CONTROLLER BUSY	AUTO-INCREMENT
	6	DISK OP IN PROGRESS	DISK DATA
	5	WRITE GATE	REG A5
	4	DATA REQUESTED	REG A4
	3	DATA AVAILABLE	REG A3
	2	SEEK COMPLETE	REG A2
	1	TRACK 0	REG A1
	0	ERROR	REG A0
A0 = 1	BIT	DATA	DATA
	7	D7	D7
	6	D6	D6
	5	D5	D5
	4	D4	D4
	3	D3	D3
	2	D2	D2
	1	D1	D1
	0	D0	D0

Table 2. Register Addressing

Auto-Increment

If the bit of the REGISTER ADDRESS is set, the address will automatically increment after every register read or write.

There are two exceptions to AUTO-INCREMENT: (1) There is no increment after writing the STEP REGISTER (address 9F); and (2) After reading or writing the DATA REGISTER (address C0).

Status Register

The STATUS REGISTER informs the host of certain events performed by the UM83C001 as well as reporting the status from the drive control.

Bit	Signal	Description
7	Controller Busy	If bit 7 comes up, this indicates that either a disk read/write is in progress or the controller is still working on the last byte written or that it is incrementing the register address
6	Disk Operation in Progress	If bit 6 comes up, a disk read/write operation is in progress.
5	Write Gate	This bit reflects the state of the WRITE GATE pin from the UM83C001 indicating that the controller is writing to the drive. Normally, registers should not be changed while writing to the disk.
4	Data Request	This bit indicates that the controller requires a byte to be written into the DISK DATA register. It is used for non-DMA data transfers.
3	Data Available	This bit indicates that there is byte for the host processor to read from the data disk register. It is used for non-DMA data transfers.
2	Seek Complete/ Status Data/LTH	This bit reflects the state of its pin (Pin 25) on the UM83C001 (i.e. if the signal at this pin is high, bit 1 will be high). It is used to indicate that the selected drive has completed any head positioning sequence; the state of a bit in the CONFIGURATION/ STATUS word on an ESDI drive; or that a QIC-36 tape has detected the lower tape hole.
1	Track 0/XFR ACK/UTH	This bit reflects the state of its pin (Pin 26) on the UM83C001 (i.e. if the signal at this pin is high, bit 2 will be high). It is used to indicate that the selected drive is at track 0; that an ESDI drive has acknowledged a COMMAND/STATUS transfer; or that a QIC-36 tape drive has detected the upper tape hole.
0	Error	This bit is set whenever any bit in the CONTROLLER ERROR register is set. It is the logical OR of the CONTROLLER ERROR register bits and may be used by the host to quickly check successful completion of a command. This bit is reset when a new command is written into the DISK OPERATION register.

Available Registers

There are 64 available REGISTER ADDRESSES in the UM83C001; however, only 41 are used. Table 3 is a list of available WRITE registers and Table 4 is a list of available READ registers.

Register Address Decimal	HEX	Auto Incr HEX	Register
0	00	80	POST-INDEX GAP
1	01	81	ID PLO LOCK-ON
2	02	82	PRE-ID
3	03	83	ID ADDRESS MARK
4	04	84	FE BYTE
5	05	85	ID
6	06	86	ID ECC
7	07	87	POST-ID
8	08	88	DATA READ SKEW
9	09	89	DATA PLO LOCK-ON
10	0A	8A	PRE-DATA
11	0B	8B	DATA ADDRESS MARK
12	0C	8C	F8 BYTE
13	0D	8D	DATA LOW
14	0E	8E	DATA HIGH
15	0F	8F	DATA ECC
16	10	90	POST DATA
17	11	91	INTER-RECORD GAP
18	12	92	SECTORS PER TRACK
19	13	93	ID START LOCATION
20	14	94	ADDRESS MARK FIRST HALF
21	15	95	ADDRESS MARK LAST HALF/UNENCODED ADDRESS MARK
22	16	96	RECORDING CODE
23	17	97	CLOCK DIVIDER
24	18	98	FE
25	19	99	F8
26	1A	9A	SECTOR SIZE
27	1B	9B	SECTOR OPTIONS
28	1C	9C	
29	1D	9D	
30	1E	9E	DIRECTION
31	1F	9F*	STEP
56	38	B8	CYLINDER HI
57	39	B9	CYLINDER LO
58	3A	BA	HEAD
59	3B	BB	SECTOR
60	3C	BC	TRANSFER COUNT
61	3D	BD	HEAD SELECT
62	3E	BE	DRIVE SELECT
63	3F	BF	DISK OP
64	40	C0*	DATA TO/FROM DISK READ/WRITE

*These Addresses do not Auto-Increment.

Table 3. Write Register Addresses

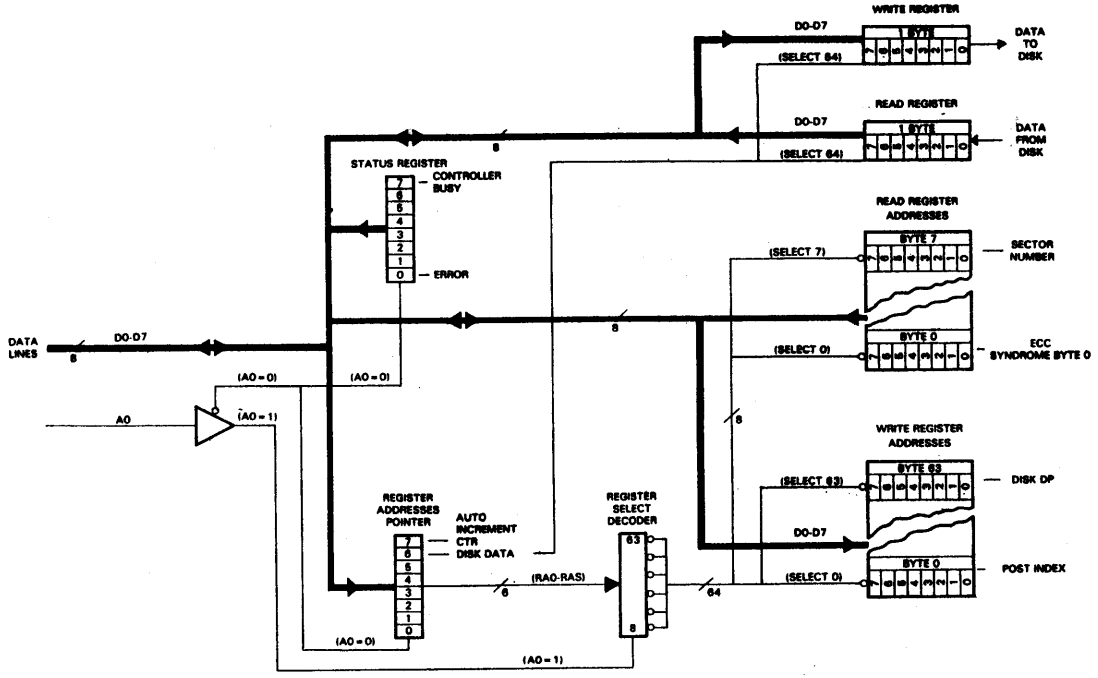


Figure 3. UM83C001 Register Addresses and Selection

Write Register Address Descriptions

The WRITE registers, Hex 0 – 17, control the length of the fields of the track format. To set the length, set the appropriate register with the desired byte count-1.

The following is a description of the available registers within the UM83C001 including the appropriate hex Register Address:

(HEX 00) POST INDEX GAP

Number of bytes after the index pulse.
FIELD LENGTH = 1 – 256 BYTES

(HEX 01) ID PLO LOCK-ON

Read gate starts at the beginning of this field. This field is to allow the PLO to lock onto the read data.
FIELD LENGTH = 1 – 64 BYTES

(HEX 02) PRE-ID

The Address Mark search begins in this field.
FIELD LENGTH = 1 – 64 BYTES

(HEX 03) ID ADDRESS MARK

This field is used on soft sectored media so that the controller can identify the start of ID and DATA fields. ADDRESS MARKS in FM or MFM are recorded with certain clock pulses missing and are unique from all other data and gap bytes recorded on the track. ADDRESS MARKS in RLL use an illegal sequence which violates the Encoding scheme of 2 to 7 zeros between flux reversals.
FIELD LENGTH = 1 – 4 BYTES

(HEX 04) FE BYTE

This field is used to identify that you are in an ID field. The value of register 18, field identifier byte, (normally an FE) is expected in this field.
FIELD LENGTH = 1 BYTE (fixed)

(HEX 05) ID

The ID information from CYL-HI, CYL-LO, HEAD and SECTION NUMBER areas are stored in this field.
FIELD LENGTH = 1 – 16 BYTES

(HEX 06) ID ECC

This field contains the CRC or ECC bytes for the ID area.
FIELD LENGTH = 1 – 8 BYTES

(HEX 07) POST-ID

This field should contain 00's. It is required to ensure proper recording and recovery of the last bits of the ID CRC/ECC field. On write data operations, the WRITE GATE goes active at the end of this field.
FIELD LENGTH = 1 – 4 BYTES

(HEX 08) DATA READ SKEW

On READ DATA operations, the READ GATE goes active at the end of this field. This field is intended to allow the PLO to skip over the write splice area before it begins trying to sync onto the read data.
FIELD LENGTH = 1 – 64 BYTES

(HEX 09) DATA PLO LOCK-ON

The READ GATE goes active at this point.
FIELD LENGTH = 1 – 4 BYTES

(HEX 0A) PRE-DATA

The search for ADDRESS MARK starts here.
FIELD LENGTH = 1 – 64 BYTES

(HEX 0B) DATA ADDRESS MARK

See ID ADDRESS MARK
FIELD LENGTH FOR HARD DISK = 1 BYTE
FIELD LENGTH FOR FLOPPY = 3 BYTES

(HEX 0C) F8 BYTE

FIELD LENGTH = 1 BYTE (fixed)

(HEX 0D) DATA LOW
(HEX 0E) DATA HIGH

These two bytes define the length of the DATA FIELD

0D = Low Byte of DATA LENGTH
0E = High Byte of DATA LENGTH

FIELD LENGTH = 1 – 65,536 BYTES

(HEX 0F) DATA ECC

See ID CRC/ECC field.
FIELD LENGTH = 1 – 8 BYTES

(HEX 10) POST DATA

Data WRITES stop at the end of this field.
FIELD LENGTH = 1 – 4 BYTES

(HEX 11) INTER-RECORD GAP

This field provides a separation between each sector to allow speed tolerances; write to read recovery time (time between deassertion of WRITE GATE and assertion of READ GATE) head switching time and controller decision making time between sectors and variations in detecting INDEX and SECTOR.
FIELD LENGTH = 1 – 256 BYTES

(HEX 12) SECTORS PER TRACK

Write N-1 to this register
FIELD LENGTH = 1 – 256 BYTES

(HEX 13) ID START LOCATION

This register is set to specify which internal register follows the FE register in the ID field. This register is set as shown below.

ID Start Value	Next Byte Following FE	
00	FE	(causes FE to be used twice)
01	CYLINDER HI	(normal setting for hard disk)
02	CYLINDER LO	(normal setting for floppy)
03	HEAD	
04	SECTOR	
05	SECTOR SIZE	

(HEX 14) ADDRESS MARK FIRST HALF
(HEX 15) ADDRESS MARK SECOND HALF

HEX 14 = The first half of the encoded ADDRESS MARK
HEX 15 = The second half of the encoded ADDRESS MARK or the whole unencoded ADDRESS MARK when running in unencoded mode.

ADDRESS MARKS are special bytes recorded at the beginning of each ID and DATA field. These bytes are unique and do not occur anywhere else on the disk. They are used to identify the exact beginning of the ID and DATA fields. These ADDRESS MARKS are made unique by violating the rules for encoding the data.

When using MFM encoding, the ADDRESS MARK is an A1 data byte with one of the clock bits dropped.

MFM CLOCK BITS 0 0 0 0 1 1 1 0
DATA BITS 1 1 1 0 0 0 0 1

MFM ADDRESS MARK
01010100 10001001 = HEX 54 and HEX 89
└ This bit has been dropped
HEX 54 = First half in location HEX 14
HEX 89 = Second half in location HEX 15

Storage

When using UM83C001 RLL encoding, the ADDRESS MARK is a 4B data byte with one of the bits dropped. This results in a unique pattern with 8 zeros in a row.

In 2,7 RLL encoding, the maximum number of zeros in a row is 7.

4B	010 010	11
RLL CODE FOR 4B	000100 000100	1000
RLL ADDRESS MARK	000100 000000	1000 = HEX 10 and HEX 08

This bit has been dropped

HEX 10 = First half in location HEX 14
HEX 08 = Second half in location HEX 15

(HEX 16) RECORDING CODE

80	00	NRZ WRITE DATA
40	01	NRZI WRITE DATA
	10	PULSE WRITE DATA
	11	
20	00	NRZ READ DATA
10	01	NRZI READ DATA
	10	PULSE READ DATA
	11	
08	000	UNENCODED
04	001	FM
02	010	MFM
	011	RLL 2,7
01	Should be 0	

(HEX 17) CLOCK DIVIDER

Through the use of a PLO divider circuit, the disk controller chip is capable of controlling several devices that do not operate at the same data rates without requiring a separate PLO circuit for each. For example, the controller can operate a hard disk, a floppy disk, and a tape drive using only a single PLO running at 10 MHz or 15 MHz. If running a 15 MHz PLO for an RLL encoded hard disk, the controller is divided by 15 to run the tape drive and divided by 30 to run the floppy disk.

The PLO divider can divide from 1 to 256. To divide by a number n, the number n-1 must be written into the Clock Divider at register address 17 hexadecimal.

In order to improve PLO lock-on performance, the Clock Divider is synchronized to the first data pulse at the beginning of every read operation.

Bytes that are written to or read from the UM83C001 at RAM CLOCK speed are internally synchronized to the WRITE CLOCK. This synchronization can take up to 5 write clock cycles. During this synchronization, the CONTROLLER BUSY bit (Status Register bit 7) will be one.

If additional bytes are written to or read from the chip during this synchronization, the results will be unpredictable.

When using a divided down clock, the length of time required for this synchronization may become significant. For example: when working with a 5-1/4 inch floppy, the disk clock would be 2 microseconds. The synchronization could take up to 5 x 2 = 10 microseconds. When designing your system, insure that reads and writes to the UM83C001 are always farther apart than 10 microseconds whenever the clock is divided down to a 2 microsecond period. This can be done by inserting extra instructions in the host program or by monitoring the CONTROLLER BUSY bit.

(HEX 18) FE

ID field identifier byte
Write FE to this register.

(HEX 19) F8

Data field identifier byte.
Write F8 to this register for hard disk or FB for floppies.

(HEX 1A) SECTOR SIZE

This byte follows the sector number in the ID field and is normally used with floppies — not hard disk.

(HEX 1B) SECTOR OPTIONS

The UM83C001 handles soft or hard sectored disks or ESDI disks using ESDI Address Marks. ESDI byte clock operation requires an external counter to create hard sector pulses.

BIT 7 to 2 = 0		
BIT 1	= 02	00 SOFT SECTORED
BIT 0	= 01	01 HARD SECTORED
		10 ESDI ADDRESS MARKS
		11 ESDI BYTE CLOCKS

(HEX 1E) DIRECTION

Bit 7 of the register is sent directly to the DIRECTION output pin. Writing a HEX 80 to this address will make the pin high; a HEX 00 will make it low. This pin is used for direction control of ST506 drives or for command data on ESDI drives.

(HEX 1F) STEP

Bit 0 of this register is sent directly to the +STEP output pin. Writing a HEX 01 to this address will make the pin high; a HEX 00 will make it low. This pin is used for STEP CONTROL of ST506 drives or for TRANSFER REQUEST on ESDI drives. Auto-increment is disabled for this address because it must be written repetitively to create multiple STEP pulses at the drive interface.

(HEX 38) CYLINDER HI

This register contains the HI 8 bits of the cylinder number. The contents of this register and the next 3 registers are used for writing or searching for ID FIELDS on the disk.

(HEX 39) CYLINDER LO

This register contains the LO 8 bits of the cylinder number.

(HEX 3A) HEAD

This register contains the HEAD number.

(HEX 3B) SECTOR

This register contains the SECTOR number. On multi-sector operations, this register is incremented after each sector is read or written and may be read at address 07.

(HEX 3C) TRANSFER COUNT

This register contains the number of sectors desired for this command –1. On multi-sector operations, this register is decremented after each sector is read or written and may be read at address 06.

(HEX 3D) HEAD SELECT

When this register is written, the external $\overline{\text{SET HEAD}}$ pin strobes low to latch the head number from the data bus.

(HEX 3E) DRIVE SELECT

When this register is written, the external $\overline{\text{SET DRIVE}}$ pin STROBES low so that the external drive register can latch the drive number from the data bus.

(HEX 3F) DISK OP

Writing to this register starts or stops DISK READ or WRITE operations. The commands are listed below and are described in more detail in the DISK COMMAND section.

00 STOP DISK OPERATION
80 NO-OP
81 WRITE DATA
82 READ DATA
83 READ ID
84 WRITE FIRST SECTOR
85 WRITE NEXT SECTOR
86 FORMAT WRITE INTERLEAVED
87 FORMAT WRITE SEQUENTIAL
88 READ DATA IMMEDIATE
89 WRITE SECTOR IMMEDIATE
8A WRITE GAP IMMEDIATE
8B VERIFY DATA
8C READ LONG
8E
8F

(HEX 40) DATA TO/FROM DISK

Data written to this register is serialized and sent as data to the disk. Writing to this register resets the DATA REQUESTED status bit (Bit 4). If data is not written fast enough to keep up with the disk, the OVERRUN/UNDERRUN status bit (register 05 Bit 1) will be set.

Read Register Address Descriptions

Register Address Decimal	Hex	Auto Inch Hex	Register	ECC 56 Bit	ECC 32 Bit	CRC 16 Bits
0	00	80	Not used			
1	01	81	Not used			
2	02	82	Not used			
3	03	83	Not used			
4	04	84	Disk status			
5	05	85	Controller status			
6	06	86	Transfer count			
7	07	87	Sector number			
8	08	88		Not used	Not used	Not used
9	09	89		0	Not used	Not used
10	0A	8A	Error	1	Not used	Not used
11	0B	8B	Syndrome	2	Not used	Not used
12	0C	8C	Bytes	3	0	Not used
13	0D	8D		4	1	Not used
14	0E	8E		5	2	0
15	0F	8F		6	3	1
64	40	C0 *	Data from disk			

* This address does not auto-increment

Table 4. Read Register Addresses

(HEX00 – HEX03) NOT USED

(HEX04) DISK STATUS

BIT 7 = DRIVE SELECTED/STATUS 1 (HEX 80)
This bit has a dual role when controlling a Winchester drive. It indicates that a drive has been successfully selected. This pin directly reads the logic level of pin 27 on the chip.

BIT 6 = READY/STATUS 0 (HEX 40)

This bit also has a dual role. When controlling floppy and Winchester drives, it indicates that a drive is up to speed and ready for read or write. And this pin directly reads the logic level of pin 21 of the chip.

BIT 5 = SECTOR ADDRESS MATCH (HEX 20)

This bit is set when a sector ID matches what was set into the Sector Address Registers during a read/write operation.

BIT 4 = LAST SECTOR ON TRACK (HEX 10)

This bit is set during the last sector of a track. (Sector # in ID field = Sector per track.) See Multi-Sector transfers.

BITS 3 THRU 0 = FIELD COUNTER

The FIELD COUNTER indicates what field is passing under the heads on a read or write.

FIELD COUNT	HEX COUNT	FIELD LOCATION ON DISK
0	00	INTER-RECORD GAP or POST-INDEX GAP
1	01	ID PLO LOCK-ON
2	02	PRE-ID
3	03	ID AM
4	04	FE
5	05	ID
6	06	ID ECC
7	07	POST-ID
8	08	DATA READ SKEW
9	09	DATA PLO LOCK-ON
10	0A	PRE-DATA
11	0B	DATA AM
12	0C	F8
13	0D	DATA
14	0E	DATA ECC
15	0F	POST-DATA

(HEX 05) CONTROLLER STATUS

BIT 7 = NO RECORD FOUND (HEX 80)

Indicates that on a read or write, the controller has received two successive index pulses without finding an ID field that matched the Sector Address registers. Sector pulses are not input on the INDEX pin).

BIT 6 = MISSING DATA AM (F8 MISCOMPARE) (HEX 40)

This bit is set if the byte after the Data Address Mark does not match the contents of register 19, the Data Field Identifier byte, indicating that a data field probably does not exist.

BIT 5 = ID ECC/CRC ERROR (HEX 20)

When set indicates that a read/write sector to the addressed sector was found, but that the CRC/ECC was in error.

BIT 4 = DATA ECC ERROR (HEX 10)

When set indicates that a read of the addressed sector was found, but that the DATA field CRC/ECC bytes was in error.

BIT 3 = DATA MISMATCH (HEX 08)

Indicates that the Verify command has stopped with a data mismatch error. See Verify command.

BIT 2 = DATA TRANSFER STOPPED (STOP RECEIVED) (HEX 04)

Indicates that during a read or write the DMA-STOP pin was activated and that the transfer has stopped.

BIT 1 = OVERRUN/UNDERRUN (HEX 02)

Indicates that data was not transferred to or from the controller quick enough for the Serializer/Deserializer section.

BIT 0 = NOT USED

(HEX 06) TRANSFER COUNT

This register contains the number of sectors remaining (including the current) for Multi-sector operations and it is decremented after each successful sector read or write.

(HEX 07) SECTOR NUMBER

This register contains the SECTOR NUMBER for the operation that the controller is currently performing. It is incremented after each multi-sector operation but is not incremented if an error occurs.

(HEX 08) NOT USED

(HEX 09) 56 BIT ECC SYNDROME BYTE 0

(HEX 0A) 56 BIT ECC SYNDROME BYTE 1

(HEX 0B) 56 BIT ECC SYNDROME BYTE 2

(HEX 0C) 56 BIT ECC SYNDROME BYTE 3

(HEX 0D) 56 BIT ECC SYNDROME BYTE 4

(HEX 0E) 56 BIT ECC SYNDROME BYTE 5

Disk Commands

Writing to the COMMAND register at location 3F causes a disk operation to begin. All registers used in the disk operation should be set up prior to writing to the COMMAND register.

(HEX 00) ABORT

This command will immediately terminate any operation in progress.

(HEX 80) NO OP

This command causes no disk operation.

(HEX 81) WRITE DATA

This command writes data from memory into the data field of the sector whose address has been written into the sector address registers in the chip. Multi-sector writes are possible up to 256 sectors.

(HEX 82) READ DATA

This command reads the data field from the sector whose ID has been set into the registers on the disk controller. The data field is transferred to memory by DMA. It may optionally be transferred under program control if the disk speed is slow enough for the computer to keep up with it. The F8 byte immediately following the data address mark is not transferred but is checked to assure that a data field is present.

At the end of every sector transfer, the Transfer Count is checked. If it is zero, the operation stops. If it is non-zero, it is decremented, the sector number is incremented, and the next sector is read. This process continues until the Transfer Count goes to zero, the end of the track is reached, or an error occurs.

The DMA data transfer may be stopped by having $\overline{STOP}$ go low during a DMA cycle ($\overline{ACK}$ low). If this happens, the disk controller will immediately cease data transfer and will halt the operation at the end of the current sector. In this case, the Transfer Count will not be decremented and the sector number will not be incremented.

The residual Transfer Count and the sector number registers can be read to determine where to continue.

(HEX 83) READ ID

This command reads the next ID field and ID ECC field that is encountered on the disk or tape. It transfers both fields to memory. The ID ECC field is checked for errors.

It can be used to establish track orientation on tape or disk. It can also be used in error recovery procedures to determine if the read-write heads are positioned over the correct track.

(HEX 84) WRITE FIRST SECTOR

This command begins writing at the Index Pulse and writes both ID fields and data fields. Information for the index field comes from the internal sector address registers. Information for the data fields is transferred from memory.

Multi-sector writes can write up to 256 sectors.

If this command is terminated by the transfer count going to zero, it stops writing at the end of the post-data field of the last sector. If this command is terminated by the sectors per track counter going to zero, it will continue writing the post-data field until the next Index Pulse is reached or until a Reset Command (00 hexadecimal) is received.

This command can be used to format and write data to a track in a single operation.

(HEX 85) WRITE NEXT SECTOR

This command begins writing at the end of the post-data field of the sector whose address has been set into the internal sector address registers. It writes ID fields as well as data fields. It stops writing at the end of the post-data field when the transfer count goes to zero.

Multi-sector writes can be done up to 256 sectors.

This command can be used to repair the ID field of a damaged sector.

(HEX 86) FORMAT INTERLEAVED

This command is similar to the Format Sequential (See HEX 87) command. However, in this command the ID fields to be written on the disk come from memory rather than from the internal registers on the ID. Numbers written are totally programmable and can be interleaved in any manner desired.

For each sector written the disk controller will fetch all bytes of the ID field plus one byte of filler (usually a hexadecimal E5) for the data field. The hexadecimal FE byte immediately following the ID Address Mark is not fetched from memory but is written from the internal register in the disk controller.

For a typical hard disk format the ID field length would be 4, and the following 5 bytes would be fetched from memory for each sector.

Cylinder High
Cylinder Low
Head
Sector
Data Filler Byte (usually E5)

If the track is being formatted with 26 sectors, then a total of 5 x 26 = 130 bytes will be fetched from memory during the Format Interleaved command execution.

(HEX 87) FORMAT SEQUENTIAL

This command is used to format a single track on a disk. It begins writing at index and continues writing to the next index. It writes all ID and data fields using the information set into the on-chip ID and DATA registers.

ID Byte	Register Address	Data Filler Byte	Register Address
CYLINDER HI	HEX 38	DATA	HEX 40
CYLINDER LO	HEX 39		
HEAD	HEX 3A		
SECTOR SIZE	HEX 1A		

After each sector is written, the sector number register is incremented by one and the track size register is decremented by one. When the track size register reaches zero, one last sector is written and the remainder of the track is written with zeros.

No data is transferred to or from memory during a format sequential command.

(HEX 88) READ DATA IMMEDIATE

It differs in that when it is issued, the track orientation counters are reset to the post-index gap and the read operation begins there. It is intended primarily for use when controlling tape drives where there is no index pulse to establish position on the track. With this command the microprocessor is resoonsible for maintaining track orientation.

Data transfer occurs the same as with the Read Data command. Up to 256 sectors can be transferred with a single command.

(HEX 89) WRITE IMMEDIATE

Write immediate is a formatting type write in that it writes the ID field of each sector as well as the data field. It is intended primarily for use when controlling tape where there is no index pulse to establish track orientation. When it is issued, the track orientation counters are set to post-index gap and + WRITE GATE goes high immediately.

ID field information is written from the internal sector address registers. Data field information is transferred from memory. The sector number is incremented after every sector is written. Up to 256 sectors can be written with a single Write Immediate command.

Writing stops at the end of the post-data field when the transfer count goes to zero.

If Write Immediate is terminated by the physical sector count going to zero, the controller will continue writing the post-data field until it is stopped by the microprocessor issuing a Reset Command (00 hexadecimal) or until an Index Pulse is received. This allows tapes to be written with a long trailer gap after the last data block.

(HEX 8A) WRITE GAP IMMEDIATE

When the Write Gap command is issued, the track orientation counters are set to post-index gap and the controller immediately begins writing zeros. Writing continues until the index is reached or until this command is terminated by the issuance of another command or a halt command.

This command is intended primarily for writing header or trailer zero fields on tape.

(HEX 8B) VERIFY DATA

This command begins reading data from the disk at the addressed sector and comparing it to the data transferred from memory. If the disk data and the data from memory do not match, this command will terminate with the Data Mismatch bit set (Read Register 0D bit 3).

(HEX 8C) READ LONG

This command is used primarily for checking the ECC and CRC circuitry. It reads and transfers to memory the data field and data ECC field of the addressed sector.

The ID ECC field and the data ECC field are checked and error latches are set if they are not correct. An error in the ID ECC field will not stop the data field from being transferred as it would with the Read Data command. However, an error in either ECC field will terminate a multi-sector Read Long at the end of the post-data field of the sector containing the error.

After using the Read Long command, the ECC Syndrome registers containing the EGG bits read from the disk instead of error bits.

This command also allows the reading of records that were written by controllers that use different ECC or CRC generators.

(HEX 8D) WRITE LONG

This command is used primarily for checking the ECC and CRC circuitry. It writes from memory the data field and the data ECC field of the addressed sector. This command permits the creation of errors to assist in testing the error detection circuits.

An error in the ID ECC field will not prevent writing to the addressed sector.

Timing Specs and Diagrams

This section is devoted to the timing of signals and their relationship to each other in order to make maximum use of the UM83C001. The following tables and diagrams are to be used as design tools when incorporating the UM83C001 into your system.

Signal	Typ.	Max.	Unit
XTAL	20	30	MHz
PLO	20	30	MHz
READ DATA	20	30	MBITS/SEC

Table 5. Signal Frequencies

Signal	LO	HI	Unit
XTAL	13	20	NANOSECONDS
PLO	13	20	
MCLK	30	30	
RESET	100		

Table 6. Signal Widths

Delays From	To	Min.	Typ.	Max.	Unit
XTAL HI	WRITE DATA		35	70	NANOSECONDS
XTAL	WRITE CLOCK		30	60	
XTAL OR PLO HI	REQUEST LO		32	63	
ACK & MCLK LO	REQUEST HI		36	72	
MCLK LO	SET HEAD LO		30	59	
MCLK HI	SET HEAD HI		21	42	
MCLK LO	SET DRIVE LO		30	59	
MCLK HI	SET DRIVE HI		21	42	
XTAL OR PLO HI	DIRECTION		43	85	
XTAL OR PLO HI	STEP		38	77	
CSEL HI OR WRT LO	D0-D7 TRI-STATE		25	50	
CSEL LO & WRT HI	D0-D7 ACTIVE		29	57	
ACK HI OR WRT LO	D0-D7 TRI-STATE		31	61	
ACK LO & WRT HI	D0-D7 ACTIVE		29	57	
XTAL HI	WRGT		32	63	
PLO HI	RDGT		36	71	
XTAL OR PLO HI	ENAM		36	71	
XTAL OR PLO HI	BUSY		31	62	
RDEL HI	FSTR HI		26	51	
PLO HI	FSTR LO		26	51	
PLO HI	SLWR LO		26	51	
RDEL HI	SLWR HI		26	51	

Table 7. Delays

From Changing Signal	Set-Up	To	Hold	Unit
ACKNOWLEDGE	4.0	RAMCLK LO		NANOSECONDS
ACKNOWLEDGE		RAMCLK HI	0	
WRITE	15	RAMCLK LO		
WRITE		RAMCLK HI	15	
CHIP SELECT	15	RAMCLK LO		
CHIP SELECT		RAMCLK HI	15	
A0	15	RAMCLK LO		
A0		RAMCLK HI	15	
NOTE THAT ALL THE ABOVE SIGNALS SHOULD CHANGE WHEN RAMCLK IS HIGH AND BE STABLE WHEN RAMCLK IS LOW				
DATA (D0 – D7)	2	RAMCLK HI	12	NANOSECONDS
STOP	6	RAMCLK HI	3	

Table 8. Set Up and Hold Time

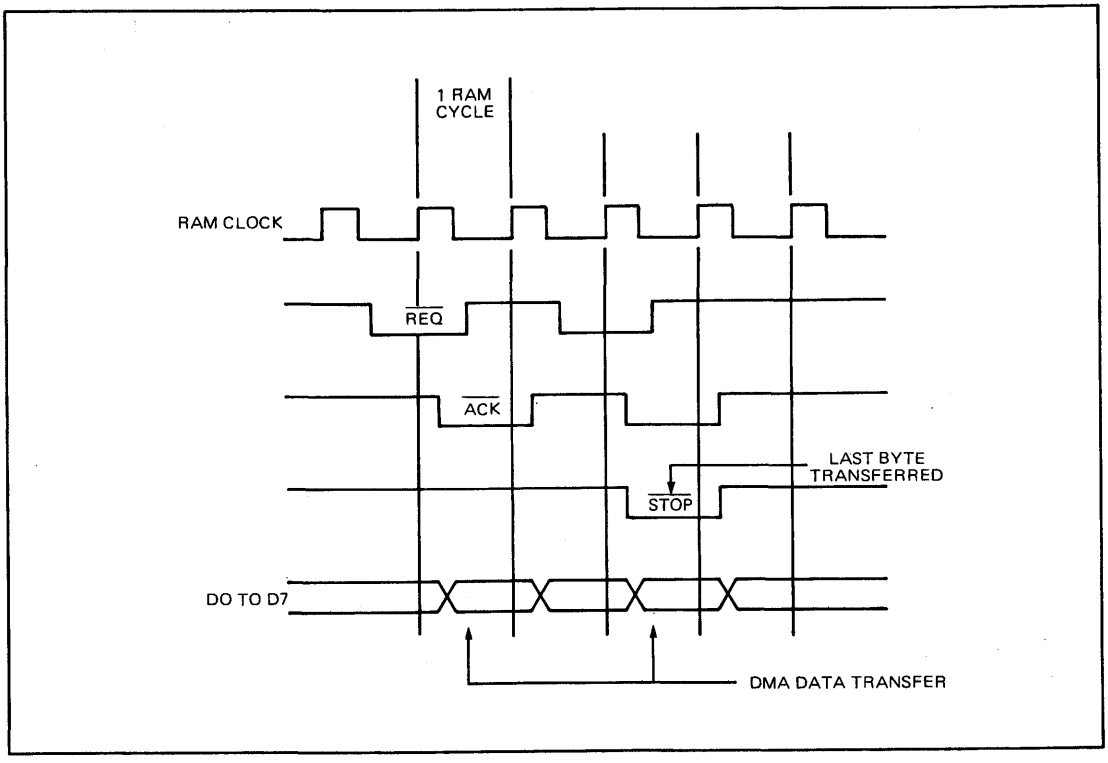


Figure 4. DMA Data Transfer Cycles

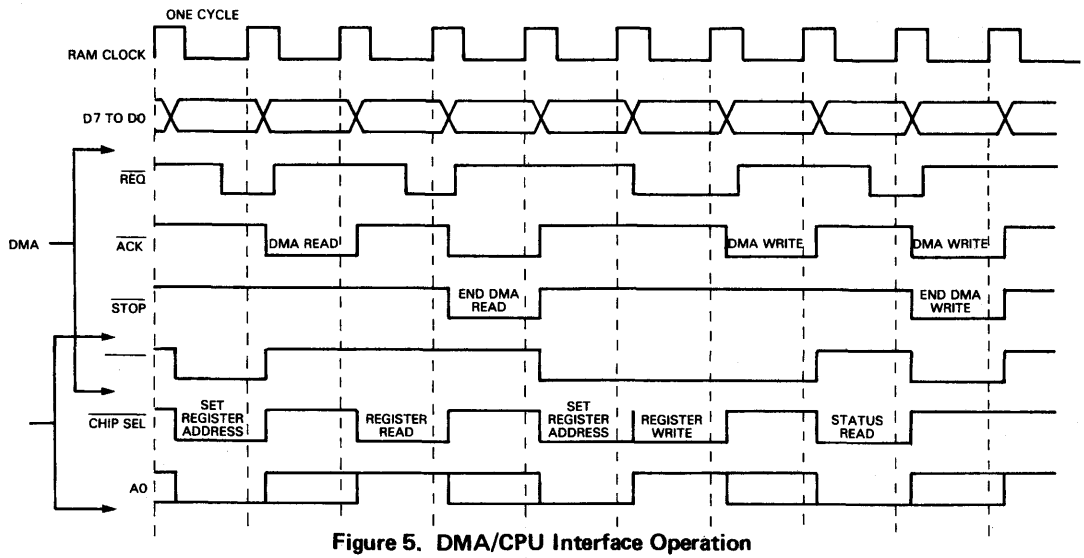


Figure 5. DMA/CPU Interface Operation

UM83C002

RAM Buffer Controller

Features

- 3 DMA channels
- Host processor port
- Refresh circuit for dynamic RAM built-in
- RAM access priority network
- Address multiplexing for dynamic RAM
- Multiplexed address and data lines from processor
- Pins arranged for easy integration into 8088/8086 systems
- No lost RAM cycles for DMA break-in
- DMA carry output permits DMA across 64K boundaries
- 24 bit timer or baud rate generator
- TTL compatible inputs and outputs. Outputs drive 8 LSTTL loads

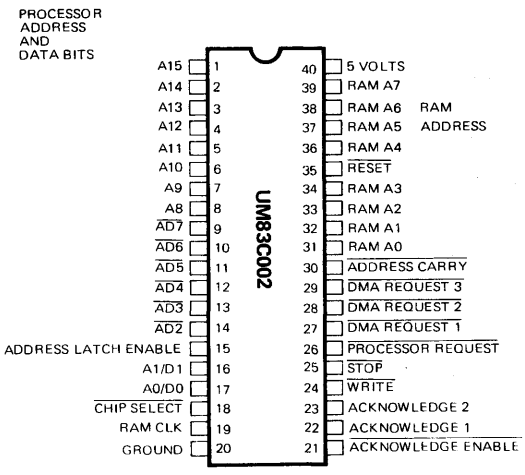
General Description

The RAM BUFFER CONTROLLER contains three high-speed DMA channels: a host computer address port, dynamic RAM refresh circuitry, and RAM access priority logic. One of the DMA address counters points inside the buffer RAM for transferring data between the RAM and the disk. A refresh address counter handles dynamic RAM refreshing. Also on chip is an address multiplexer.

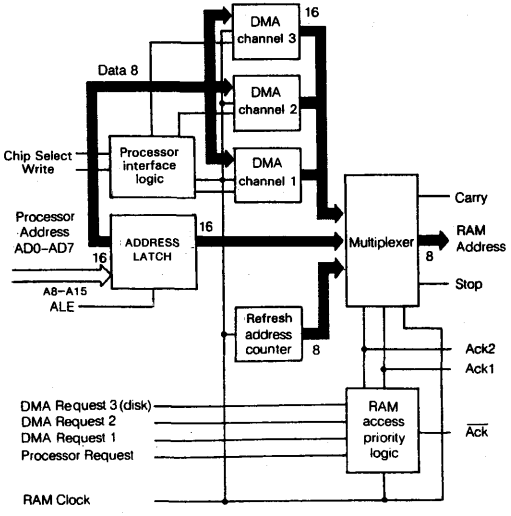
The DISK CONTROLLER UM83C001 connects to one of the RAM controller chip's DMA channels. The two other DMA channels may be used by other high-speed memory-peripheral drives or tape systems — if the chip set is being used with its own on-board processor.

When teamed with the UM83C001, the UM83C002 gives the disk direct access to a buffer RAM array. What's more, it does so at a speed high enough to accommodate 5 Mbit, 10 Mbit and 15 Mbit data transfer rates. The new ST412HP interface, for instance, which operates at 10 Mbits with MFM encoding, would have a 15 Mbit throughput if it employed RLL2, 7 encoding instead.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Power Supply Voltage, V_{DD} . . . . . −0.5 to +7.0 V
Input Voltage, V_I . . . . . −0.5 V to V_{DD} + 0.5 V
Operating Temperature, T_{OPT} . . . . . −40 to +85°C
Storage Temperature, T_{STG} . . . . . −65 to +150°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Power Supply Voltage	V_{DD}	4.5	5	5.5	V	
Input Voltage	V_I	0		V_{DD}	V	
Low-Level Input Voltage	V_{IL}	0		0.8	V	TTL Level*
High-Level Input Voltage	V_{IH}	2.0		V_{DD}	V	TTL Level*
Input Rise Fall Times	t_R, t_F			10	μS	

Note: (T_A = 0 to +70°C, V_{DD} = 5 V + 5% unless otherwise specified)

DC Electrical Characteristics

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Static Current	I_L		0.1	200	μA	$V_I = V_{DD}$ or GND
Dynamic Current	I_{DD}		4		μA	1 MHz/cell
Input Current	I_I		0.1	10	μA	$V_I = V_{DD}$ or GND
Low-Level Output Current	I_{OL}	3.2	9		mA	V_{OL} = 0.4 V
High-Level Output Current	I_{OH}	1	3		mA	$V_{OH} = (V_{DD}-0.4)$ V
Low-Level Output Voltage	V_{OL}			0.1	V	$I_O = 0$
High-Level Output Voltage	V_{OH}	$V_{DD}-0.1$			V	$I_O = 0$

AC Characteristics

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Maximum Operating Frequency	f_{MAX}	DC		50	MHz	
Output Rise Time	t_R		8		ns	C_L = 15 pF
Output Fall Time	t_F		4		ns	C_L = 15 pF

Pin Description

Pin No.	Symbol	Description
1 THRU 14, 16, AND 17	PROCESSOR ADDRESS AND DATA BITS	These 16 pins are time multiplexed to provide a 16 bit CPU Address and an 8 bit CPU data bus to the UM83C001
15	ADDRESS LATCH ENABLE (ALE)	When the ADDRESS LATCH ENABLE signal is high, the address on the AD0 to AD15 lines is enabled into the ADDRESS LATCH in the UM83C002. When the ALE signal goes low, this address is held in the latch to be used for addressing the RAM. After ALE goes low, data may be placed on the AD0 to AD7 lines.
18	$\overline{\text{CHIP SELECT}}$ ($\overline{\text{CSEL}}$)	The CHIP SELECT lines are driven low by the processor to read from or write to the registers inside the UM83C002. This signal is not intended to be gated by the processor's acknowledge signal. When the processor does a read of registers within the UM83C002, the read data will be held on the data lines until the $\overline{\text{CSEL}}$ line goes back high.
19	RAM CLOCK	This line is an input that serves two purposes. It provides the timing for multiplexing the RAS and CAS addresses to the dynamic RAM and its trailing or rising edge provides the clock to define all memory cycles. When this line is high the RAS addresses are output at RAM A0 to RAM A7. When it is low, the CAS addresses are output at RAM A0 to RAM A7. $\overline{\text{REQ1}}$, $\overline{\text{REQ2}}$, $\overline{\text{REQ3}}$ and $\overline{\text{REQH}}$ are sampled at the rising edge of this clock to determine who will be granted access to memory during the next memory cycle.
20	GROUND	Negative supply.
21	$\overline{\text{ACKNOWLEDGE ENABLE}}$	A low on this line indicates that one of the REQUEST lines has been granted access to RAM. The REQUEST lines are sampled on the rising edge of RAM CLOCK..
22	ACKNOWLEDGE 1	When the $\overline{\text{ACKNOWLEDGE}}$ line is low, these two lines are encoded to indicate which request has been granted access to RAM.
23	ACKNOWLEDGE 2	

$\overline{\text{ACK}}$	ACK2	ACK1	Request Granted
L	H	H	REQUEST 3
L	H	L	REQUEST 2
L	L	H	REQUEST 1
L	L	L	CPU REQUEST

Pin Description (Continued)

Pin No.	Symbol	Description
24	$\overline{\text{WRITE}}$ ($\overline{\text{WRT}}$)	This line indicates whether a read or a write is to be performed. A low indicates a write and a high indicates a read. During processor cycles, it is driven by the processor. During DMA cycles, it is normally driven by the UM83C002. However, the UM 83C002 may be programmed to allow the I/O device to drive this line. During unused cycles and refresh cycles, the UM83C002 drives this line high to eliminate the need for an external pull-up resistor.
25	$\overline{\text{STOP}}$	This line goes low to indicate the last cycle of a DMA transfer. It is normally driven low by the UM83C002 when the byte counter of the active DMA channel has reached zero. The DMA channel becomes disabled after this last cycle and it will ignore any further requests until it has been restarted by writing to its command register. Each channel can be programmed to allow the external I/O device to drive this line. However, internal byte counts are always active so that transfer will stop when $\overline{\text{STOP}}$ goes low or when the byte count reaches zero, whichever comes first. This line is driven by the UM83C002 during unused cycles (cycles during which $\overline{\text{ACKNOWLEDGE}}$ is high). It is normally driven low. However, a refresh cycle is indicated when $\overline{\text{STOP}}$ $\overline{\text{ACKNOWLEDGE}}$ and $\overline{\text{WRITE}}$ are high at the same time. A timer cycle is indicated by $\overline{\text{WRITE}}$ being low when $\overline{\text{ACKNOWLEDGE}}$ and $\overline{\text{STOP}}$ are high.
26	$\overline{\text{PROCESSOR REQUEST}}$	The processor requests access to RAM by placing a low on this line. This line is sampled by the rising edge of the RAM CLOCK. The processor has lowest priority. It will be granted access to RAM only if all three DMA requests are HIGH.
27	$\overline{\text{DMA REQUEST 1}}$	This is the lowest priority DMA REQUEST. It samples on the rising edge of RAM CLOCK. DMA CHANNEL 1 will be granted access to RAM, If DMA REQUEST 2 and DMA REQUEST 3 are high.
28	$\overline{\text{DMA REQUEST 2}}$	This is the middle priority DMA REQUEST. This channel will be granted access to RAM only if DMA REQUEST 3 is high.
29	$\overline{\text{DMA REQUEST 3}}$	This is the highest priority DMA REQUEST. If this line is low when the rising edge of RAM CLOCK occurs, DMA CHANNEL 3 will control the next memory cycle.
30	$\overline{\text{ADDRESS CARRY}}$	This output goes low to indicate that the memory address of the DMA channel that is acknowledged is at its maximum count of 65,535 and will roll over to 0 at the end of this memory cycle. This line also goes low on a refresh cycle when the refresh address counter is at its maximum count of 255. This line also goes low on a timer cycle when the timer is at its maximum count. When operating in the address decrement mode, that line goes low to indicate that the DMA channel address is 0000 and this it is going to roll over to FFFF at the end of the current memory cycle. This line is provided so that DMA transfers can be performed across 64K boundaries if desired. This line would be used to increment an external counter containing the higher order address bits. This line can also be used to increment additional external refresh address counter bits if more than 8 bits of refresh address are required. This line can also be used to extend the timer beyond 24 bits.

Pin Description (Continued)

Pin No.	Symbol	Description
31 ~ 34 36 ~ 39	A0 ~ A3 A4 ~ A7 RAM	These are the multiplexed address lines for use with dynamic RAMS. When RAM CLOCK is high, address bits 8 thru 15 are gated to these lines. When RAM CLOCK is low, address bits 0 thru 7 are gated to these lines. During REFRESH cycles, the refresh address is gated to these lines. During TIMER cycles, the timer count is gated to these lines.
35	$\overline{\text{RESET}}$	A low on this $\overline{\text{RESET}}$ line resets the UM83C002 to its initial state. The refresh rate is set to maximum refresh every other memory cycle and all three DMA channels are disabled.
40	+5 VOLTS	Positive supply.

RAM BUS Operation

A combination of pin signals control the BUS OPERATION to and from the UM83C002 chip. These combinations are shown in Table 1.

$\overline{\text{CARRY}}$	$\overline{\text{STOP}}$	$\overline{\text{CSEL}}$	$\overline{\text{WRITE}}$	$\overline{\text{ACK}}$	ACK2	ACK1	RAM BUS Operation
X	X	H	L	L	L	L	CPU WRITE TO MEM/IO
X	X	H	H	L	L	L	CPU READ FROM MEM/IO
X	X	L	L	L	L	L	CPU WRITE TO UM83C002
X	X	L	H	L	L	L	CPU READ FROM UM83C002
X	X	X	L	L	L	H	CH 1 WRITE TO MEMORY
X	X	X	H	L	L	H	CH 1 READ FROM MEMORY
L	X	X	X	L	L	H	CH 1 ADDRESS CARRY
X	L	X	X	L	L	H	CH 1 STOP TRANSFER
X	X	X	L	L	H	L	CH 2 WRITE TO MEMORY
X	X	X	H	L	H	L	CH 2 READ FROM MEMORY
L	X	X	X	L	H	L	CH 2 ADDRESS CARRY
X	L	X	X	L	H	L	CH 2 STOP TRANSFER
X	X	X	L	L	H	H	CH 3 WRITE TO MEMORY
X	X	X	H	L	H	H	CH 3 READ FROM MEMORY
L	X	X	X	L	H	H	CH 3 ADDRESS CARRY
X	L	X	X	L	H	H	CH 3 STOP TRANSFER
X	H	X	L	H	X	X	TIMER COUNT ON BUS
L	H	X	L	H	X	X	TIMER COUNT CARRY
X	H	X	H	H	X	X	REFRESH ADDRESS ON BUS
L	H	X	H	H	X	X	REFRESH ADDRESS CARRY
X	L	X	X	H	X	X	INACTIVE BUS CYCLE

H = HIGH L = LOW X = DON'T CARE

Table 1. Signal Combinations

Register Addressing

The UMC RAM BUFFER CONTROLLER, UM83C002, occupies 2 I/O port locations selected by the ADO pin. ADO driven low selects the REGISTER ADDRESS/ STATUS REGISTER and ADO driven high selects the DATA register.

There are 16 internal registers in the UM83C002. These registers are accessed by writing the register address into the REGISTER ADDRESS register. The selected register can then be accessed by doing a READ or WRITE with ADO high.

		Read	Write
	BIT	STATUS	REGISTER ADDRESS
AO = 0	7	CHANNEL 3 ACTIVE	0
	6	CHANNEL 2 ACTIVE	0
	5	CHANNEL 1 ACTIVE	CHANNEL NO. BIT 1
	4	TIMER ACTIVE	CHANNEL NO. BIT 0
	3	AUTO-INCREMENT	AUTO-INCREMENT
	2	REG A2	REG A2
	1	REG A1	REG A1
	0	REG A0	REG A0
	BIT	REGISTER DATA	REGISTER DATA
AO = 1	7	D7	D7
	6	D6	D6
	5	D5	D5
	4	D4	D4
	3	D3	D3
	2	D2	D2
	1	D1	D1
	0	D0	D0

Table 2. Register Addressing

The following is a list of the WRITE and READ addresses:

Register Address Decimal	HEX	Auto INCR HEX	Function	Read	Write
0	00	08	TIMER/REFRESH	TIMER COUNT	CLK DIVIDER LO
1	01	09		CH 1 STATUS	CLK DIVIDER HI
2	02	0A		CH 2 STATUS	TIMER CONTROL
3	03	0B		CH 3 STATUS	TIMER COUNT
4	04	0C*		TIMER COUNT	REFRESH RATE
16	10	18	DMA CHANNEL 1		ADDRESS LO
17	11	19			ADDRESS HI
18	12	1A			BYTE COUNT LO
19	13	1B			BYTE COUNT HI
20	14	1C*		CH 1 STATUS	CH 1 COMMAND
32	20	28	DMA CHANNEL 2		ADDRESS LO
33	21	29			ADDRESS HI
34	22	2A			BYTE COUNT LO
35	23	2B			BYTE COUNT HI
36	24	2C*		CH 2 STATUS	CH 2 COMMAND
48	30	38	DMA CHANNEL 3		ADDRESS LO
49	31	39			ADDRESS HI
50	32	3A			BYTE COUNT LO
51	33	3B			BYTE COUNT HI
52	34	3C*		CH 3 STATUS	CH 2 COMMAND

* These addresses do not auto-increment.

Table 3. Register Addresses

Write Register Addresses

(HEX 00) CLK DIVIDER LO (AUTO INCR HEX 08)

The timer consists of a 16-bit variable CLOCK DIVIDER which divides the RAM CLOCK rate. The divided down RAM CLOCK is then used to increment the 8-bit TIMER COUNT register.

(HEX 01) CLK DIVIDER HI (AUTO INCR HEX 09)

To divide by "N", the 16 bit CLOCK DIVIDER is set to N-1.

(HEX 02) TIMER CONTROL (AUTO INCR HEX OA)

Writing to this address sets one of several timer modes.

BIT 7 = ENABLE TIMER
- 1 = Timer Run
- 0 = Timer Hold

BIT 6 = OUTPUT ON INCREMENT
- 1 = Timer Byte Output to Bus When it Increments
- 0 = Timer Byte not Output on Increment

BIT 5 = OUTPUT ON CARRY
- 1 = Timer Byte Output to Bus When it Rolls over to 0
- 0 = Timer Byte Not Output on Roll Over

BIT 4 = STOP AT CARRY
- 1 = Timer Stops When it Rolls Over
- 0 = Timer Does Not Stop When it Rolls Over

BIT 3 = 0

BIT 2 = 0

BIT 1 = 0

BIT 0 = 0

(HEX 03) TIMER COUNT (AUTO INCR HEX OB)

Writing to this address sets the initial value of the TIMER COUNT. It also initializes the CLOCK DIVIDER.

(HEX 04) REFRESH RATE (AUTO INCR HEX OO)

An 8-bit register is provided for the setting of the refresh rate. Setting this register to 01 will cause refresh cycles to be inserted at the maximum rate which is one cycle. Setting this register to 00 will cause refresh to be disabled.

(HEX XX) ADDRESS LO (AUTO INCR HEX XX)

(HEX 10) = Channel 1 (AUTO INCR HEX 18)
(HEX 20) = Channel 2 (AUTO INCR HEX 28)
(HEX 30) = Channel 3 (AUTO INCR HEX 38)

Low byte of the initial value for the DMA ADDRESS

(HEX XX) ADDRESS HI (AUTO INCR HEX XX)

(HEX 11) = Channel 1 (AUTO INCR HEX 19)
(HEX 21) = Channel 2 (AUTO INCR HEX 29)
(HEX 31) = Channel 3 (AUTO INCR HEX 39)

High byte of the initial value for DMA ADDRESS

(HEX XX) BYTE COUNT LO (AUTO INCR HEX XX)

(HEX 12) = Channel 1 (AUTO INCR HEX 1A)
(HEX 22) = Channel 2 (AUTO INCR HEX 2A)
(HEX 32) = Channel 3 (AUTO INCR HEX 3A)

Low byte of the initial value for the BYTE COUNT for the transfer. Set this to N-1 to transfer N bytes.

(HEX XX) BYTE COUNT HI (AUTO INCR HEX XX)

(HEX 13) = Channel 1 (AUTO INCR HEX 1C)
(HEX 23) = Channel 2 (AUTO INCR HEX 2C)
(HEX 33) = Channel 3 (AUTO INCR HEX 3C)

High byte for the initial value for the BYTE COUNT

(HEX XX) COMMAND (AUTO INCR HEX XX)

(HEX 14) = Channel 1 (AUTO INCR HEX 1D)
(HEX 24) = Channel 2 (AUTO INCR HEX 2D)
(HEX 34) = Channel 3 (AUTO INCR HEX 3D)

Writing to these addresses STARTS, STOPS or CONTINUES the DMA operation.

BIT 7 = ENABLE CHANNEL
- 1 = Enable Channel to Respond to DMA Request
- 0 = Disable Channel so it Ignores DMA Request

BIT 6 = INITIALIZE ADDRESS
- 1 = Set Address to Initial Value
- 0 = Leave Address at Previous Value

BIT 5 = INITIALIZE COUNT
- 1 = Set Count to Initial Value
- 0 = Leave Count at Previous Value

BIT 4 = AUTO INITIALIZE
- 1 = Address and Byte Count Are Reset to Initial Values When Byte Count Reaches Zero. DMA Operation Continues
- 0 = DMA Operation Stops When Byte Count Reaches Zero.

BIT 3 = WRITE TO MEMORY
1 = DMA Write to Memory
0 = DMA Read from Memory

BIT 2 = EXTERNAL STOP
1 = Stop Line is Driven from External Source
0 = RB1002 Drives Stop Line

BIT 1 = EXTERNAL WRITE CONTROL
1 = Write Line is An Input for This Channel
0 = RB1002 Drives Write Line

BIT 0 = ADDRESS INCREMENT MODE
1 = Increment Address after Every DMA Read Or Write
0 = Decrement Address after Every DMA Read Or Write

Read Registers Addresses

(HEX 00) TIMER COUNT (AUTO INCR HEX 08)

Current value of the TIMER COUNT.

(HEX 01) CH 1 STATUS (AUTO INCR HEX 09)

SEE WRITE UP AT READ ADDRESS 14

(HEX 02) CH 2 STATUS (AUTO INCR HEX 0A)

SEE WRITE UP AT READ ADDRESS 24

(HEX 03) CH 3 STATUS (AUTO INCR HEX 0B)

SEE WRITE UP AT READ ADDRESS 34

(HEX 04) TIMER COUNT (AUTO INCR HEX 00)

Current value of the TIMER COUNT

(HEX XX) ADDRESS LO (AUTO INCR HEX XX)

(HEX 10) = Channel 1 (AUTO INCR HEX 18)
(HEX 20) = Channel 2 (AUTO INCR HEX 28)
(HEX 30) = Channel 3 (AUTO INCR HEX 38)

Current address low byte

(HEX XX) ADDRESS HI (AUTO INCR HEX XX)

(HEX 11) = Channel 1 (AUTO INCR HEX 19)
(HEX 21) = Channel 2 (AUTO INCR HEX 29)
(HEX 31) = Channel 3 (AUTO INCR HEX 39)

Current address high byte

(HEX XX) BYTE COUNT LO (AUTO INCR HEX XX)

(HEX 12) = Channel 1 (AUTO INCR HEX 1A)
(HEX 22) = Channel 2 (AUTO INCR HEX 2A)
(HEX 32) = Channel 3 (AUTO INCR HEX 3A)

Current BYTE COUNT

(HEX XX) BYTE COUNT HI (AUTO INCR HEX XX)

(HEX 13) = Channel 1 (AUTO INCR HEX 1B)
(HEX 23) = Channel 2 (AUTO INCR HEX 2B)
(HEX 33) = Channel 3 (AUTO INCR HEX 3B)

Current BYTE COUNT

(HEX XX) STATUS (AUTO INCR HEX XX)

(HEX 14) = Channel 1 (AUTO INCR HEX 1C)
(HEX 24) = Channel 2 (AUTO INCR HEX 2C)
(HEX 34) = Channel 3 (AUTO INCR HEX 3C)

The following STATUS information is also available at READ addresses 01, 02 and 03

BIT 7 = CHANNEL ENABLE
1 = Channel is Enabled
0 = Channel is Disabled

BIT 6 = ADDRESS CARRY
1 = Address is at FFFF if Counting up; Address is at OOOO if Counting down
0 = Not at Carry

BIT 5 = TERMINAL COUNT
1 = Byte Count is at Zero
0 = Byte Count is Not Zero

BIT 4 = AUTO INITIALIZE
1 = Auto Initialize Mode
0 = Stop at Terminal Count

BIT 3 = WRITE TO MEMORY
1 = DMA Write to Memory Mode
0 = DMA Read from Memory Mode

BIT 2 = EXTERNAL STOP
1 = Stop is Input
0 = Stop is Output

BIT 1 = EXTERNAL WRITE CONTROL
1 = Write is Externally Controlled
0 = Write is Internally Controlled

BIT 0 = ADDRESS INCREMENT MODE
1 = Address Counts up
0 = Address Counts down

Dynamic RAM Refresh

The UM83C002 has built-in refresh circuitry for dynamic RAMs. It provides 8 bits of refresh address so that dynamic RAMs up to 256 K bits can be accommodated.

An 8 bit register is also provided for the setting of the refresh rate. Setting this register to 01 will cause refresh cycles to be inserted at the maximum rate which is one cycle out of two. Activating the $\overline{\text{RESET}}$ line also sets the refresh to its maximum rate. Setting this register to 255 will cause one refresh cycle to be inserted for every 256 memory cycles. Setting this register to 00 will cause refresh to be disabled.

The refresh cycles are inserted into otherwise unused memory cycles whenever possible to maximize system performance. For example: If the rate register is set to 255 and there are any unused cycles during the first 255 cycles of the refresh period, the refresh will be inserted into the first of them and it will be totally invisible to the rest of the system.

During a refresh cycle, the $\overline{\text{ACKNOWLEDGE}}$, $\overline{\text{STOP}}$ and $\overline{\text{WRITE}}$ lines will be high simultaneously. The refresh address will be on the MA0 to MA7 lines. If the refresh address is at hexadecimal FF, then the $\overline{\text{CARRY}}$ line will also be low.

Timing Specifications

This section is devoted to the timings of signals and their relationship to each other in order to make the maximum use of the UM83C002. The following tables and diagrams are to be used as design tools when incorporating the UM83C002 into your system.

Signal	Min.	Typ.	Max.	Unit
MCLK		10	20	MHz

Table 4. Clock Frequency

Signal	LO	HI	Unit
MCLK	20	30	ns
ALE		20	ns
RESET	100		ns

Table 5. Signal Widths

Delays From	TO	Typ.	Max.	Unit
MCLK HI	WRITE	35	70	ns
	STOP	35	69	ns
	CARRY	37	73	ns
	ACK1, ACK2	26	52	ns
	ACK	29	57	ns
	MA0 TO MA7	40	80	ns
MCLK LO	MA0 TO MA7	39	78	ns
CSEL LO & WRT HI & MCLK LO	AD0-AD7 ACTIVE	36	72	ns

Table 6. Delays

Set-Up and Hold Times	Set-Up	TO	Hold	Unit
REQ3, REQ2, REQ1, REQH	15	MCLK HI	15	ns
WRITE	15	MCLK LO		ns
WRITE		MCLK HI	15	ns
CHIP SELECT	15	MCLK LO		ns
CHIP SELECT		MCLK HI	15	ns
AO	15	MCLK LO		ns
AO		MCLK HI	15	ns
STOP	15	MCLK HI	10	ns

Table 7. Set-Up and Hold Times

UMC

UM83C003

Hard Disk Controller Interface

Features

- Interfaces to PC XT systems with Hard-Disk controller
- I/O channel ready signal generator (generates wait state)
- Clock generator
- Sector buffer RAM addressing and control
- Data bus drives directly to slot.
- 68-pin PLCC package.
- Supports MFM Disk Controller

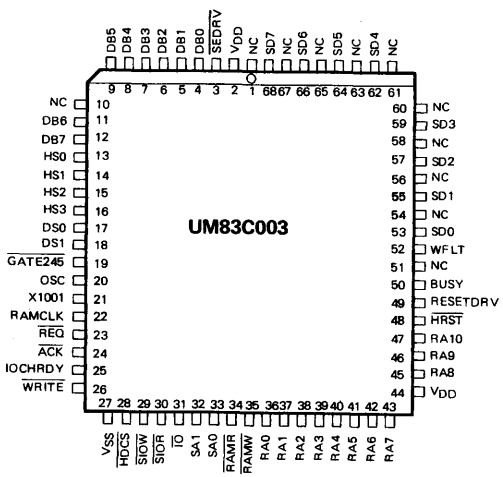
General Description

The UM83C003 incorporates several functions in a single package. Implementation of these functions occurs by combining random logic. The UM83C003 contains the following circuits:

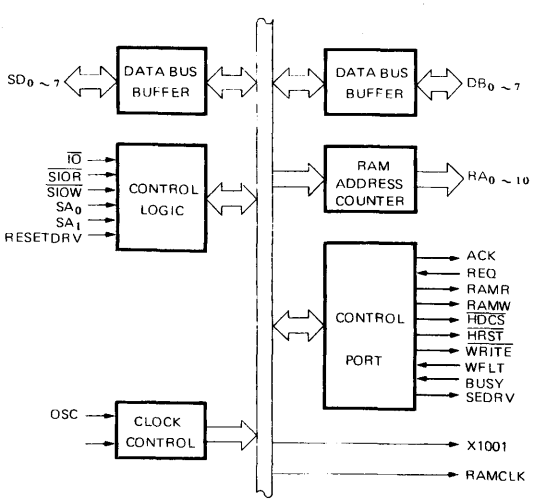
Clock Generator
Sector Buffer RAM Addressing and Control
Data Bus Interface Control
HDC Status & Control Port

The UM83C003 connects directly to the Host interface Data/Command and intraboard Command/Data buses.

Pin Configuration



Block Diagram



Storage

Absolute Maximum Ratings*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . −55°C to +150°C
All Output Voltages . . . . . −0.5 to + 7 V
All Input Voltages . . . . . −0.5 to + 7 V
Supply Voltage V_{CC} . . . . . −0.5 to + 7 V
Power Dissipation 1W

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{CC} = 5.0V ± 5%, T_A = 0 ~ 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage	2.0	–	V_{CC}	V
V_{IL}	Input Low Voltage	0	–	0.8	V
V_{OH}	Output High Voltage				
	I_{Load} = −6.4mA (SD0 ~ SD7)	2.4	–	–	V
	I_{Load} = −3.2mA (all others)	2.4	–	–	V
V_{OL}	Output Low Voltage				
	I_{Load} = 6.4mA (SD0 ~ SD7)	–	–	0.4	V
	I_{Load} = 3.2mA (all others)	–	–	0.4	V

AC Characteristics

Symbol	Parameter	Min.	Max.	Unit
t_1	Address hold time	10	–	ns
t_2	$\overline{RAMW}$ time delay	–	50	ns
t_3	$\overline{RAMW}$ low to data output	–	60	ns
t_4	Data hold time	–	15	ns
t_5	$\overline{RAMR}$ time delay	–	40	ns
t_6	$\overline{RAMR}$ low to data output	–	140	ns
t_7	$\overline{RAMR}$ high to data High Z	–	60	ns
t_8	OSC to X1001 delay time	–	50	ns
t_9	X1001 to RAMCLK delay time	–	25	ns

Capacitance

Parameter	Max.	Unit
Output Capacitance		
SD0 ~ SD7	50	pF
All others	20	pF

Pin Description

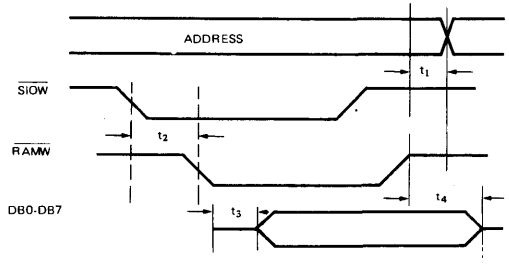
Number	Symbol	I/O	Description
53, 55, 57 59, 62, 64, 66, 68	SD0-SD7	I/O	These lines provide data bus bit0-bit7 for system microprocessor.
4, 5, 6, 7, 8, 9, 11, 12	DB0-DB7	I/O	These lines provide data bus bit0-bit7 for static RAM, & controller.
3	$\overline{SEDRV}$	I	This command line indicates selection of drive no, or drive head no. This signal is active low.
20	OSC	I	This signal is supported by the external oscillator. The working frequency is 30 MHz.
23 24	$\overline{REQ}$ $\overline{ACK}$	I O	These signal pins indicate that another master is requesting a local bus. The chip receiving the REQ will issue ACK as an acknowledgement in the RAM CLK clock cycle. These signals are active low.
29	$\overline{SIOW}$	I	This command line is an input control signal used by the CPU to load information into the chip. This signal is active low.
30	$\overline{SIOR}$	I	This command line is an input control signal used by the CPU to read the control signal. It is active low.
31	$\overline{IO}$	I	A "Low" on this chip enables the chip. No reading or writing will occur unless the chip is selected. This signal is active low.
33 32	SA0 SA1	I I	These inputs are normally connected to the address bus.
49	RESETDRV	I	A "High" on the input which resets all control registers on the chip.
50	BUSY	I	BUSY is high when the operation is in process. The CPU can read the status of the controller used by this pin.
51	NC		Not Connected.
52	WFLT	I	When the drive encounters an error in process. It sends an error signal to the controller to indicate "Write fault". The CPU can read the error message of the controller used by this pin. It is active high.
13, 14, 15, 16	HS0, HS1 HS2, HS3	O	No. of the drive head. 16 heads are selected.
17, 18	DS0, DS1	O	No. of the disk. 4 disks are selected.
19	$\overline{GATE245}$	O	This signal pin is optional. If the sink current of SD0-SD7 is not enough to drive the system data bus, the gate 74LS245 is directly connected by using this pin.
21	X1001	O	When MFMSW is high, X1001 is OSC/3. Otherwise, X1001 is OSC/2.
22	RAMCLK	O	When MFMSW is high. RAMCLK is OSC/9. Otherwise, RAMCLK is OSC/6.
25	IOCHRDY	O	When this signal is active high, it may use this line during a write operation if more time is needed to store the data from the bus. It also holds the data long enough for the system microprocessor to sample.
26	$\overline{WRITE}$	O	This command line indicates that the UM83C001 chip fetches a read or write operation. This signal is active low.

Pin Description (Continued)

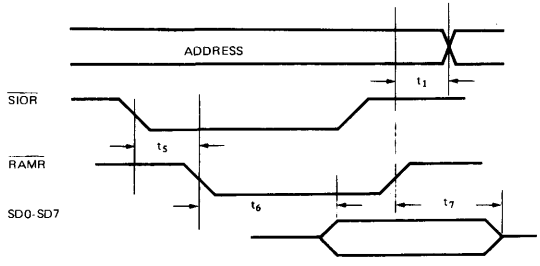
Number	Symbol	I/O	Description
28	$\overline{HDCS}$	O	A "Low" on this input enables the UM83C001 chip. No reading or writing will occur unless the UM83C001 chip is selected.
35	$\overline{RAMW}$	O	The command line indicates that the CPU is loading information into static RAM. This signal is active low.
34	$\overline{RAMR}$	O	The command line indicates that the static RAM is sending data to the data bus. This signal is active low.
48	$\overline{HRST}$	O	$\overline{HRST}$ is an active low output dervied from the RESETDRV input.
36, 37, 38, 39, 40, 41, 42, 43, 45, 46, 47	RA0-RA10	O	The signals are connected to the static RAM address. The data in the static RAM is read or written by the controller.

Timing Waveforms

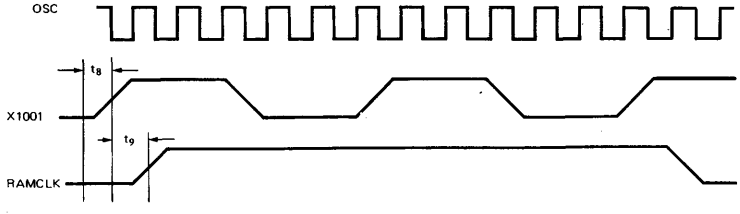
Write Cycle



Read Cycle



Clock Timing



UMC

UM83C004

Hard Disk Controller Interface

Features

- Interfaces to PC XT systems with Hard-Disk controller
- I/O channel ready signal generator (generates wait state)
- Clock generator
- Sector buffer RAM addressing and control
- Data bus drives directly to slot.
- 68-pin PLCC package.
- Supports RLL/MFM Disk Controller

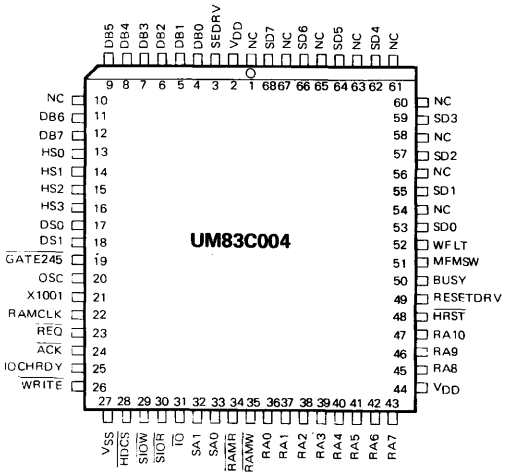
General Description

The UM83C004 incorporates several functions in a single package. Implementation of these functions occurs by combining random logic. The UM83C004 contains the following circuits:

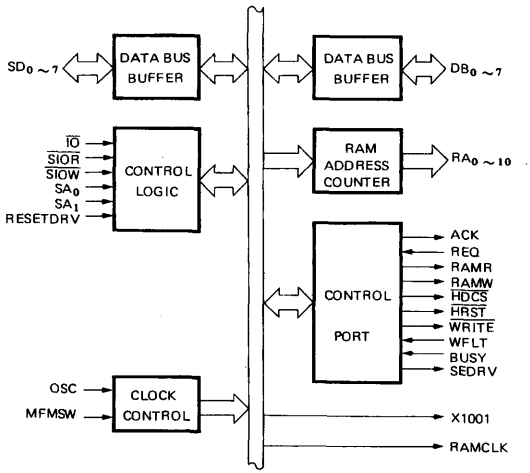
Clock Generator
Sector Buffer RAM Addressing and Control
Data Bus Interface Control
HDC Status & Control Port

The UM83C004 connects directly to the Host interface Data/Command and intraboard Command/Data buses.

Pin Configuration



Block Diagram



Storage

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Storage Temperature . . . . . –55°C to +150°C
All Output Voltages . . . . . –0.5 to + 7V
All Input Voltages . . . . . –0.5 to + 7V
Supply Voltage V_{CC} . . . . . –0.5 to + 7V
Power Dissipation 1W

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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Symbol	Characteristic	Min.	Typ.	Max.	Unit
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V_{IL}	Input Low Voltage	0	–	0.8	V
V_{OH}	Output High Voltage				
	I_{Load} = –6.4mA (SD_0 ~ SD_7)	2.4	–	–	V
	I_{Load} = –3.2mA (all others)	2.4	–	–	V
V_{OL}	Output Low Voltage				
	I_{Load} = 6.4mA (SD_0 ~ SD_7)	–	–	0.4	V
	I_{Load} = 3.2mA (all others)	–	–	0.4	V

AC Characteristics

Symbol	Item	Min.	Max.	Unit
t_1	Address hold time	10	–	ns
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t_3	$\overline{RAMW}$ low to data output	–	60	ns
t_4	Data hold time	–	15	ns
t_5	$\overline{RAMR}$ time delay	–	40	ns
t_6	$\overline{RAMR}$ low to data output	–	140	ns
t_7	$\overline{RAMR}$ high to data High Z	–	60	ns
t_8	OSC to X1001 delay time	–	50	ns
t_9	X1001 to RAMCLK delay time	–	25	ns

Capacitance

Parameter	Max.	Unit
Output Capacitance		
SD0 ~ SD7	50	pF
All others	20	pF

Pin Descriptions

Pin No.	Symbol	I/O	Description
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3	$\overline{\text{SEDRV}}$	I	This command line indicates selection of drive no, or drive head no. This signal is active low.
20	OSC	I	This signal is supported by the external oscillator. The working frequency is 30 MHz.
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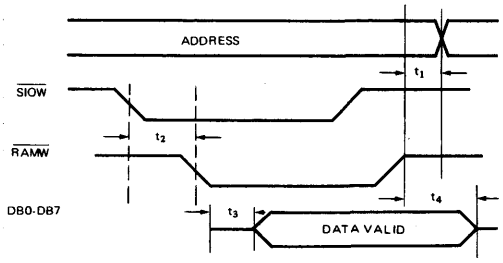
30	$\overline{\text{SIOR}}$	I	This command line is an input control signal used by the CPU to read the control signal. It is active low.
31	$\overline{\text{IO}}$	I	A "Low" on this chip enables the chip. No reading or writing will occur unless the chip is selected. This signal is active low.
33 32	SA0 SA1	I I	These inputs are normally connected to the address bus.
49	RESETDRV	I	A "High" on the input resets all control registers on the chip.
50	BUSY	I	BUSY is high when the operation is in process. The CPU can read the status of the controller used by this pin.
51	MFMSW	I	If the signal is high, it selects MFM code. Otherwise, it selects RLL code.
52	WFLT	I	When the drive encounters an error in process, it sends an error signal to the controller to indicate "Write fault". The CPU can read the error message of the controller used by this pin. It is active high.
13, 14, 15, 16	HS0, HS1 HS2, HS3	O	No. of the drive head. 16 heads are selected.
17, 18	DS0, DS1	O	No. of the disk. 4 disks are selected.
19	GATE245	O	This signal pin is optional. If the sink current of SD0-SD7 is not enough to drive the system data bus, the gate 74LS245 is directly connected by using this pin.
21	X1001	O	When MFMSW is high, X1001 is OSC/3. Otherwise, X1001 is OSC/2.
22	RAMCLK	O	When MFMSW is high. RAMCLK is OSC/9. Otherwise, RAMCLK is OSC/6.
25	IOCHRDY	O	When this signal is active high, it may use this line during a write operation if more time is needed to store the data from the bus. It also holds the data long enough for the system microprocessor to sample.
26	$\overline{\text{WRITE}}$	O	This command line indicates that the UM83C001 chip fetches read or write operation. This signal is active low.
28	$\overline{\text{HDCS}}$	O	A "Low" on this input enables the UM83C001 chip. Noreading or writing will occur unless the UM83C001 chip is selected.

Pin Descriptions (Continued)

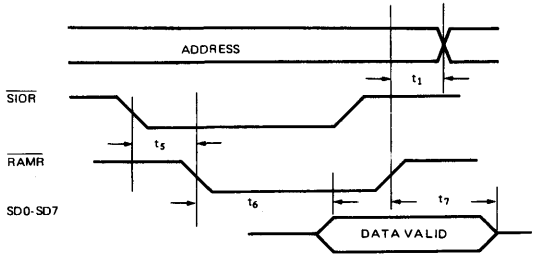
Pin No.	Symbol	I/O	Description
35	$\overline{RAMW}$	O	The command line indicates that the CPU loads information into static RAM. This signal is active low.
34	$\overline{RAMR}$	O	The command line indicates that the static RAM sends data to the data bus. This signal is active low.
48	$\overline{HRST}$	O	$\overline{HRST}$ is an active low output derived from the RESETDRV input.
36, 37, 38, 39, 40, 41, 42, 43, 45, 46, 47	RA0-RA10	O	The signals are connected to the static RAM address. The data in the static RAM is read or written by the controller.

Timing Waveforms

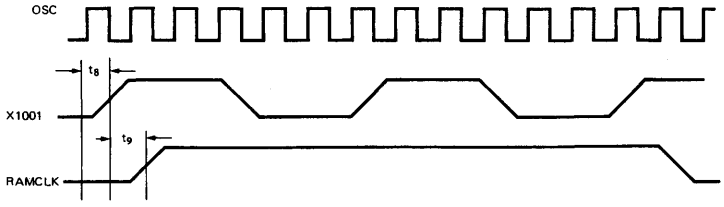
Write Cycle



Read Cycle



Clock Timing



UMC

UMC

UM83C021

Hard Disk Controller

Features

- Serializer-deserializer
- Programmable track format, compatible with WD Track format
- External drive select and head select registers for expandability
- With Hardware ECC capability
- Internal phase detector for phase lock oscillator
- Interface options: ST-506, ST-412, ST-412HP, ESDI, FLOPPY, and QIC-36 TAPE
- Sector options: SOFT, HARD, ESDI ADDRESS MARKS, ESDI BYTE and ESDI BYTE CLOCKS
- Recording options: UNENCODED, FM, MFM or RLL
- Error checking and correcting options: ECC or CRC
- Write data options: PULSE, NRZ or NRZI
- Read data options: PULSE, NRZ or NRZI
- TTL compatible inputs and outputs. Outputs drive 8 LSTTL loads

General Description

The UM83C021 Hard Disk Controller is a CMOS LSI device which performs a majority of the functions for controlling floppy drives, Winchester drives and QIC-36 streaming tape drives.

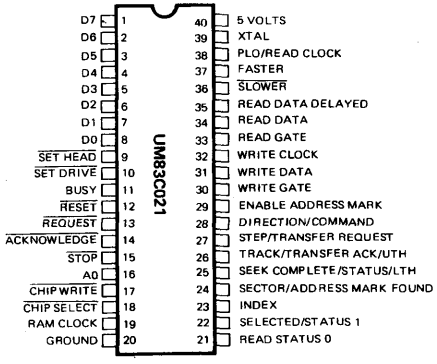
Interface Options

ST-506 (non-buffered seek Winchesters)
ST-412 (buffered seek Winchesters)
ST-412HP (10 mbos buffered seek Winchesters)
ESDI STEP/SERIAL MODES (10 mbos Winchesters)
SA-450 (5" and 3" floppies)
SA800/850 (8" floppies)
QIC-36 (streaming tape drives)

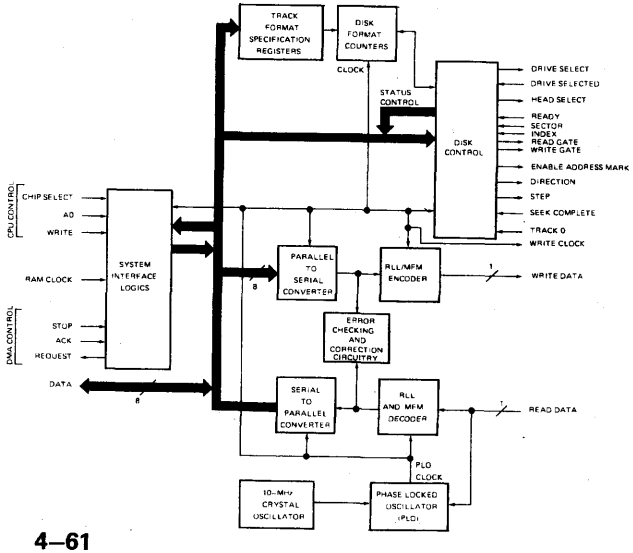
Sector Options

SOFT-SECTORING (floppy and Winchester)
HARD-SECTORING (floppy and Winchester)
ESDI ADDRESS MARKS (ESDI drives)
ESDI BYTE CLOCKS (ESDI drives)

Pin Configuration



Block Diagram



Storage

Recording Codes

UNENCODED (for ESDI drives)
FM (Frequency Modulation)
MFM (Modified Frequency Modulation)
RLL (Run Length Limited)

Error Checking

CRC (CCITT CRC-16)
ECC (4 byte, corrects 11 contiguous erroneous bits)

Data Options

NRZ (non-return to zero)
NRZI (non-return to zero inverted)
PULSE

Track Format

Extensive control over the track format is provided by allowing the length of fields and content of ADDRESS MARKS and identifier bytes, etc. to be programmed into registers.

There are 23 registers related to TRACK FORMAT inside the UM83C021 (Refer to Figure 1). 18 of these registers contain lengths of fields within a track. Others contain "content" information. Length fields are written with length−1 giving them a range of 1 to 256 inclusive. The Data Field Length Register is 2 bytes yielding a maximum data field length of 65,536 bytes. .

Absolute Maximum Ratings*

Power Supply Voltage, V_{DD} . . . . . −0.5 to +7.0V
Input Voltage, V_I . . . . . −0.5V to V_{DD} +0.5V
Operating Temperature, T_{OPT} . . . . . 0°C to +85°C
Storage Temperature, T_{STG} . . . . . −65 to +150°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

(T_A = 0 to +70°C, V_{DD} = 5V ± 5%)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Power Supply Voltage	V_{DD}	4.5	5	5.5	V	
Input Voltage	V_I	0		V_{DD}	V	
Low-level Input Voltage	V_{IL}	0		0.8	V	TTL Level
High-level Input Voltage	V_{IH}	2.0		V_{DD}	V	TTL Level
Input Rise/Fall Times	t_R, t_F	0		10	us	

DC Electrical Characteristics

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Static Current	I_L		0.1	200	μA	$V_I = V_{DD}$ or GND
Dynamic Current	I_{DD}		4		μA	1 MHz/cell
Input Current	I_I	0.1		10	μA	$V_I = V_{DD}$ or GND
Low-level Output Current	I_{OL}	3.2	9		mA	$V_{OL} = 0.4V$
High-level Output Current	I_{OH}	1	3		mA	$V_{OH} = V_{DD} - 0.4V$
Low-level Output Voltage	V_{OL}			0.1	V	$I_O = 0$
High-level Output Voltage	V_{OH}	$V_{DD} - 0.1$			V	$I_O = 0$

AC Characteristics

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Maximum Operating Frequency	f_{MAX}	DC		20	MHz	
Output Rise Time	t_R		8		ns	$C_L = 15$ pF
Output Fall Time	t_F		4		ns	$C_L = 15$ pF

Track Format

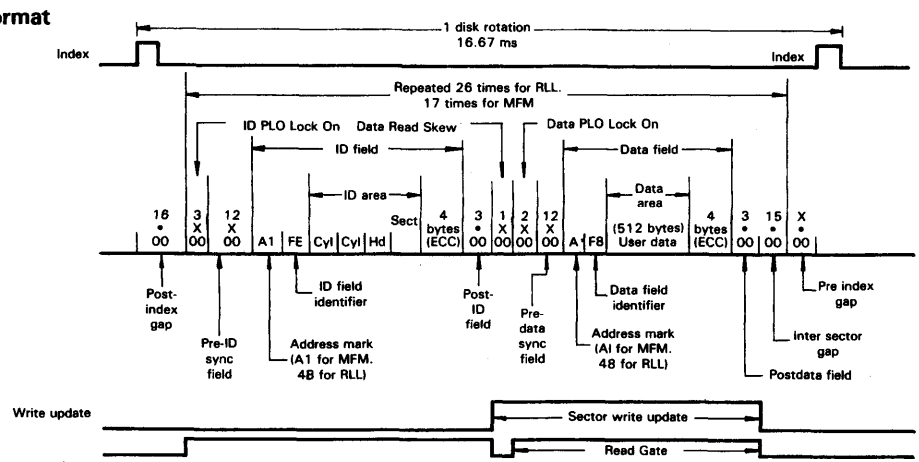


Figure 1. UM83C021 Track Format Diagram

HEX Register Address	Function	***Range (In Bytes)
00	POST INDEX GAP	1 – 256
01	ID PLO LOCK-ON	1 – 64
02	PRE ID	1 – 64
03	ID ADDRESS MARK	1 – 4
04	FE BYTE	1 (fixed)
05	ID	1 – 16
06	ID ECC	1 – 4
07	POST ID	1 – 4
08	DATA READ SKEW	1 – 64
09	DATA PLO LOCK-ON	1 – 64
A	PRE DATA	1 – 64
B	DATA ADDRESS MARK	1 – 4
C	F8 BYTE	1 (fixed)
D	DATA FIELD	
	LOW BYTE	1 – 65, 536
0E	HIGH BYTE	
0F	DATA ECC	1 – 4
10	POST DATA	1 – 4
11	INTER-RECORD GAP	1 – 256
12	SECTORS PER TRACK	1 – 256
1C	** GAP VALUE REGISTER	1

*** SET REGISTERS TO n–1 TO GET n BYTE LENGTH
** WRITE 4E for MFM encoding, 33 for RLL encoding

Table 1. Programmable Format Variables

Pin Description

Pin No.	Symbol	Description
1 – 8	DATA LINES D0 – D7 (TO/FROM HOST)	These 8 data lines are used for PROCESSOR and DMA READS and WRITES. They change synchronously with RAM CLOCK rising edge.
9	$\overline{\text{SET HEAD}}$	This signal is used to clock the HEAD ADDRESS, for the drive, into an external HEAD SELECT register. Writing to REGISTER ADDRESS 3D produces a pulse for loading the external head select onto this line.
10	$\overline{\text{SET DRIVE}}$	This signal is the load pulse for the external drive selection register. Writing to REGISTER ADDRESS 3E produces the load pulse on this pin.
11	BUSY	Pin 11 goes high to indicate that the DISK CONTROLLER is busy doing a disk READ or WRITE operation. This pin can be used, if desired, to cause an interrupt for the host processor at the end of a disk READ or WRITE operation.
12	$\overline{\text{RESET}}$	The $\overline{\text{RESET}}$ line is intended to be an initial power on reset line. In order to be efficient, it should go low or be low for a minimum of 100 nanoseconds at the beginning of power on. This line is a hard reset line and will immediately terminate any disk READ or WRITE operations or any other functions and reset the chip to an initial state. It should be used essentially as a power on RESET and is not intended for use as a termination command.

Pin Description (Continued)

Pin No.	Symbol	Description
13	$\overline{\text{REQUEST}}$	The $\overline{\text{REQUEST}}$ line, in conjunction with the $\overline{\text{ACKNOWLEDGE}}$ signal (Pin 14), are the "HANDSHAKING" lines for the DMA data transfer for the chip. The DISK CONTROLLER has a byte of information ready to transfer to RAM or needs a byte of information from RAM to write to the disk when the signal at pin 13 is pulled low. The RAM BUFFER CONTROLLER chip (UM83C002) will respond by driving the $\overline{\text{ACKNOWLEDGE}}$ signal (Pin 14) low and giving the DISK CONTROLLER access to the RAM BUFFER. The DMA transfer operations are run synchronously with the RAM CLOCK signal (Pin 19). The rising edge of the RAM CLOCK pulse defines the cycle boundaries for the RAM.
14	$\overline{\text{ACKNOWLEDGE}}$	This input is driven low to indicate that the requested DMA byte transfer is currently taking place. The $\overline{\text{ACKNOWLEDGE}}$ signal should be a full RAM CLOCK cycle in width. On a disk read operation, the $\overline{\text{ACKNOWLEDGE}}$ signal causes the UM83C021 to gate a byte of data onto the D0 – D7 data lines. On a disk write or verify operation, the $\overline{\text{ACKNOWLEDGE}}$ signal causes the UM83C021 to accept a byte of data from the D0 – D7 data lines. To assure proper "Handshaking" with the $\overline{\text{REQUEST}}$ line, this line must change state while the RAM CLOCK signal is high. If data is not transferred fast enough to keep up with the requirements of the disk or tape, then the OVERRUN/UNDERRUN bit will be set to one (register address 05 bit 1). If this happens, the current disk operation will be terminated at the end of the current sector.
15	$\overline{\text{STOP}}$	This input goes low to indicate the last cycle of a DMA transfer. It is normally driven low by the UM83C002 when the byte counter of the active DMA channel has reached zero. The UM83C021 will continue reading or writing until the end of the current sector is reached and then stop. However, it will not generate any more data requests after the $\overline{\text{STOP}}$ line has been activated. On a sector write, the remainder of the sector will be filled with the last byte that was transferred. This line is ignored unless $\overline{\text{ACKNOWLEDGE}}$ is also low.
16	A0	The UMC DISK CONTROLLER (UM83C021) occupies two I/O port locations selected by the A0 pin. A0 driven low selects the REGISTER ADDRESS POINTER or STATUS REGISTER and A0 driven high selects the READ or WRITE REGISTERS. (Refer to table 2)
17	$\overline{\text{CHIP WRITE}}$	This input is driven by the CPU to indicate whether a register read or write is to be performed. A low indicates a write; a high indicates a read. This line has meaning only when $\overline{\text{CHIP SELECT}}$ is low; and it is ignored when $\overline{\text{CHIP SELECT}}$ is high.
18	$\overline{\text{CHIP SELECT}}$ ($\overline{\text{CSEL}}$)	The $\overline{\text{CHIP SELECT}}$ line ($\overline{\text{CSEL}}$) is driven low by the processor to read from or write to the registers inside the UM83C021. This signal is intended to be gated by processor's ACKNOWLEDGE signal.
19	RAM CLOCK (RAMCLK)	This clock input synchronizes all CPU and DMA operations of the UM83C021. Cycle boundaries are defined by the rising edge of this clock.

Pin Description (Continued)

Pin No.	Symbol	Description
20	GROUND	Negative Supply
21	READY STATUS 0	This input status line is available to the Host Processor at READ REGISTER 04 Bit 6. This line performs no logical function within the UM83C021 and hence the DRIVE READY signal or any other desired status signal may be connected to this pin.
22	SELECTED or STATUS 1	This input status line is available to the Host Processor at READ REGISTER 04 Bit 7. This line performs no logical function within the UM83C021, hence the DRIVE SELECTED signal or any other desired status signal may be connected to this pin.
23	INDEX	The rising edge of this INDEX signal from the selected drive is used to define the beginning of the track. It occurs once per revolution.
24	SECTOR or ADDRESS MARK FOUND	SECTOR For hard sectored drives, the rising edge of this input defines the beginning of sector except sector 0. The beginning of sector 0 is defined by the rising edge of INDEX. ADDRESS MARK FOUND For soft sectored ESDI drives, the rising edge of this ADDRESS MARK FOUND defines the leading edge of every sector except sector 0. The beginning of sector 0 is defined by the rising edge of INDEX.
25	SEEK COMPLETE or STATUS or LTH	SEEK COMPLETE The SEEK COMPLETE input is available to the Host Processor as STATUS REGISTER Bit 2. STATUS For ESDI drives, the serial status line is input at this pin and is available to the Host Processor as STATUS REGISTER Bit 2. LTH (LOWER TAPE HOLE) For QIC-36 tapes the LOWER TAPE HOLE signal is input at this pin and is available to the Host Processor as STATUS REGISTER Bit 2.
26	TRACK 0 or TRANSFER ACK or UTH	TRACK 0 For ST-506 type drives, the TRACK 0 signal is input at this pin and is available to the Host Processor as STATUS REGISTER Bit 1. TRANSFER ACK (ESDI DISK) For ESDI drives, the TRANSFER ACKNOWLEDGE signal is input at this pin and is available to the Host Processor as STATUS REGISTER Bit 1. UTH (UPPER TAPE HOLE – QIC-36 TAPE) For QIC-36 tapes, the UPPER TAPE HOLE signal is input at this pin and is available to the Host Processor as STATUS REGISTER Bit 1.

Pin Description (Continued)

Pin No.	Symbol	Description
27	STEP TRANSFER REQUEST	STEP This output is the STEP pulses for ST-506 drives. This line goes high whenever a one is written to register 1F bit 0. This line goes low whenever a zero is written to register 1F bit 0. TRANSFER REQUEST This output is used for TRANSFER REQUEST for ESDI drives.
28	DIRECTION COMMAND	DIRECTION This output is the DIRECTION signal for ST-506 drives and goes high whenever a one is written to register 1E Bit 7. COMMAND This output is the SERIAL COMMAND line for ESDI drives.
29	ENABLE ADDRESS MARK	This signal is required for the ESDI interface. When writing, it causes the ESDI drive to write an address mark on the track. When reading, it causes the ESDI drive to search for an ADDRESS MARK. When the ESDI drive finds an ADDRESS MARK it will activate the ADDRESS MARK FOUND signal at Pin 24. For ESDI drives, WRITE REGISTER 1 should be set to 2 to produce a 3 byte wide ENABLE ADDRESS MARK signal on format writes.
30	WRITE GATE	This signal goes directly to the disk interface and must be HIGH to write data to the disk.
31	WRITE DATA	This signal is the WRITE DATA that goes to the disk drive. This WRITE DATA may be un-encoded or encoded either MFM or RLL and may be either in a pulse format, an NRZ format or NRZI format.
32	WRITE CLOCK	This signal is the code/encoded data rate and is intended for use as a WRITE CLOCK for the ESDI drive interface.
33	READ GATE	This signal indicates that the controller is in an ID for DATA area and is attempting to phase lock onto the READ DATA. This signal is used in the ESDI interface. This signal remains ACTIVE even though the DISK CONTROLLER chip is not actually performing a READ. The BUSY signal (Pin 11) can be used in conjunction with the READ GATE signal to produce a signal enabling an external phase comparator if desired.
34	READ DATA	This signal is the raw DATA pulses that are sent directly from the drive.
35	READ DATA DELAYED	This signal is the same as the READ DATA (Pin 34) with the exception that it is delayed by one half of a READ DATA CYCLE. For example: If you are running MFM data with a code rate of 10 MHz yielding a READ DATA CYCLE of 100 nanoseconds, then the data on this pin would be DELAYED by one half of the 100 nanoseconds equaling 50 nanoseconds. An external delay line is utilized to produce this READ DATA DELAYED signal.

Pin Description (Continued)

Pin No.	Symbol	Description
36 37	$\overline{\text{SLOWER}}$ and FASTER	These two signals are used as comparison inputs to an external VOLTAGE CONTROLLED OSCILLATOR so that it can produce the PLO signal at Pin 38.
38	PLO/READ CLOCK	The PHASE LOCK OSCILLATOR (PLO) Input is a READ CLOCK signal which is phase locked onto the READ DATA. The rising edge of the PLO clock should occur at the same time as the rising edge of the READ DATA delayed signal at Pin 35. If the DISK CONTROLLER chip is used to control an ESDI interface drive, the input to this pin would be the READ CLOCK signal coming directly from the ESDI interface.
39	XTAL (Crystal)	This is the crystal oscillator input which is the reference clock for writing to the hard disk. The XTAL frequency should be the code frequency going to the disk. For example: If running at MFM with a 5 megabit disk data rate, the MFM code going to the disk would be at a 10 MHz rate and the XTAL input would be at 10 MHz. If using RLL code with a 7 1/2 megabit disk data rate, the code rate going to the disk would be 15 MHz and the XTAL input would be 15 MHz. For ESDI drives, the READ CLOCK would be input at this pin.
40	5 VOLTS	Positive Supply

Register Addresses

Data Lines (D0-D7), in conjunction with the software controlled A0 signal (as an enabling signal), are decoded to select either a write or read operation to be performed and the REGISTER ADDRESSES to be utilized. (Table 2 is a chart of the A0 REGISTER ADDRESSES)

		Read	Write
	BIT	STATUS	REGISTER ADDRESS
A0 = 0	7	CONTROLLER BUSY	AUTO-INCREMENT
	6	DISK OP IN PROGRESS	DISK DATA
	5	WRITE GATE	REG A5
	4	DATA REQUESTED	REG A4
	3	DATA AVAILABLE	REG A3
	2	SEEK COMPLETE	REG A2
	1	TRACK 0	REG A1
	0	ERROR	REG A0
A0 = 1	BIT	DATA	DATA
	7	D7	D7
	6	D6	D6
	5	D5	D5
	4	D4	D4
	3	D3	D3
	2	D2	D2
	1	D1	D1
	0	D0	D0

Table 2. Register Addressing

Auto-Increment

If bit 7 of the REGISTER ADDRESS is set, the address will be automatically incremented after every register read or write.

There are two exceptions to AUTO-INCREMENT: (1) There is no increment after writing the STEP REGISTER (address 9F); and (2) After reading or writing the DATA REGISTER (address C0).

Status Register

The STATUS REGISTER informs the host of certain events performed by the UM83C021 as well as reporting status from the drive control.

Bit	Signal	Description
7	Controller Busy	If bit 7 comes up, this indicates that either a disk read/write is in progress or the controller is still working on the last byte written or it is incrementing the register address.
6	Disk Operation in Progress	If bit 6 comes up, a disk read/write operation is in progress.
5	Write Gate	This bit reflects the state of the WRITE GATE pin from the UM83C021 indicating that the controller is writing to the drive. Normally, registers should not be changed while writing to the disk.
4	Data Request	This bit indicates that the controller requires a byte to be written into the DISK DATA register. It is used for non-DMA data transfers.
3	Data Available	This bit indicates that there is a byte for the host processor to read from the data disk register. It is used for non-DMA data transfers.
2	Track 0/XFR ACK/UTH	This bit reflects the state of its pin (Pin 26) on the UM83C021 (i.e. if the signal at this pin is high, bit 2 will be high). It is used to indicate that the selected drive is at track 0; that an ESDI drive has acknowledged a COMMAND/STATUS transfer; or that a QIC-36 tape drive has detected the upper tape hole.
1	Seek Complete/ Status Data/LTH	This bit reflects the state of its pin (Pin 25) on the UM83C021 (i.e. if the signal at this pin is high, bit 1 will be high). It is used to indicate that the selected drive has completed any head positioning sequence; the state of a bit in the CONFIGURATION/ STATUS word on an ESDI drive; or that a QIC-36 tape has detected the lower tape hole.
0	Error	This bit is set whenever any bit in the CONTROLLER ERROR register is set. It is the logical OR of the CONTROLLER ERROR register bits and may be used by the host to quickly check successful completion of a command. This bit is reset when a new command is written into the DISK OPERATION register.

Available Registers

There are 64 available REGISTER ADDRESSES in the UM83C021; however, only 41 are used. Table 3 is a list of available WRITE registers and Table 4 is a list of available READ registers.

Register Address Decimal	HEX	Auto Incr HEX	Register
0	00	80	POST-INDEX GAP
1	01	81	ID PLO LOCK-ON
2	02	82	PRE-ID
3	03	83	ID ADDRESS MARK
4	04	84	FE BYTE
5	05	85	ID
6	06	86	ID ECC
7	07	87	POST-ID
8	08	88	DATA READ SKEW
9	09	89	DATA PLO LOCK-ON
10	0A	8A	PRE-DATA
11	0B	8B	DATA ADDRESS MARK
12	0C	8C	F8 BYTE
13	0D	8D	DATA LOW
14	0E	8E	DATA HIGH
15	0F	8F	DATA ECC
16	10	90	POST DATA
17	11	91	INTER-RECORD GAP
18	12	92	SECTORS PER TRACK
19	13	93	ID START LOCATION
20	14	94	ADDRESS MARK FIRST HALF
21	15	95	ADDRESS MARK LAST HALF/UNENCODED ADDRESS MARK
22	16	96	RECORDING CODE
23	17	97	CLOCK DIVIDER
24	18	98	FE
25	19	99	F8
26	1A	9A	SECTOR SIZE
27	1B	9B	SECTOR OPTIONS
28	1C	9C	GAP VALUE
29	1D	9D	
30	1E	9E	DIRECTION
31	1F	9F*	STEP
56	38	B8	CYLINDER HI
57	39	B9	CYLINDER LO
58	3A	BA	HEAD
59	3B	BB	SECTOR
60	3C	BC	TRANSFER COUNT
61	3D	BD	HEAD SELECT
62	3E	BE	DRIVE SELECT
63	3F	BF	DISK OP
64	40	C0*	DATA TO/FROM DISK READ/WRITE

*These Addresses do not Auto-Increment.

Table 3. Write Register Addresses

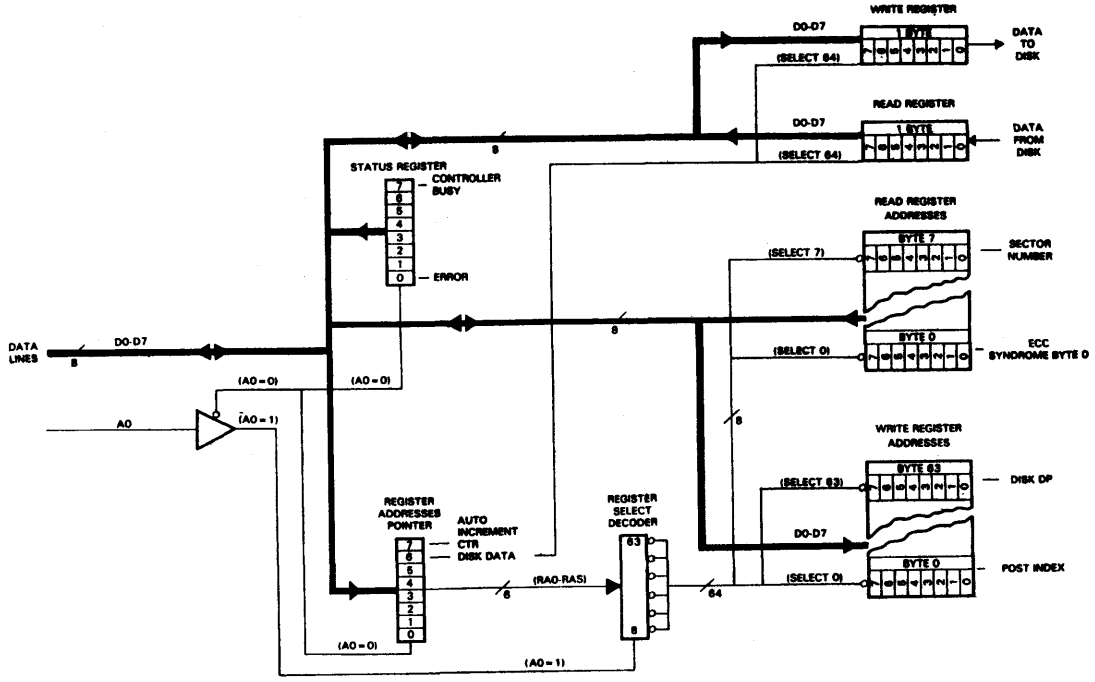


Figure 3. UM83C021 Register Addresses and Selection

Write Register Address Descriptions

The WRITE registers, Hex 0 – 17, control the length of the fields of the track format. To set the length, set the appropriate register with the desired byte count–1.

The following is a description of the available registers within the UM83C021 including the appropriate hex Register Address:

(HEX 00) POST INDEX GAP

Number of bytes after the index pulse.
FIELD LENGTH = 1 – 256 BYTES

(HEX 01) ID PLO LOCK-ON

Read gate starts at the beginning of this field. This field is to allow the PLO to lock onto the read data.
FIELD LENGTH = 1 – 64 BYTES

(HEX 02) PRE-ID

The Address Mark search begins in this field.
FIELD LENGTH = 1 – 64 BYTES

(HEX 03) ID ADDRESS MARK

This field is used on soft sectored media so that the controller can identify the start of ID and DATA fields. ADDRESS MARKS in FM or MFM are recorded with certain clock pulses missing and are unique from all other data and gap bytes recorded on the track. ADDRESS MARKS in RLL use an illegal sequence violating the Encoding scheme of 2 to 7 zeros between flux reversals.
FIELD LENGTH = 1 – 4 BYTES

(HEX 04) FE BYTE

This field is used to identify that you are in an ID field. The value of register 18, field identifier byte, (normally an FE) is expected in this field.
FIELD LENGTH = 1 BYTE (fixed)

(HEX 05) ID

The ID information: CYL-HI, CYL-LO, HEAD and SECTOR NUMBER areas are stored in this field.
FIELD LENGTH = 1 – 16 BYTES

(HEX 06) ID ECC

This field contains the CRC or ECC bytes for the ID area.
FIELD LENGTH = 1 – 8 BYTES

(HEX 07) POST-ID

This field should contain 00's. It is required to ensure proper recording and recovery of the last bits of the ID CRC/ECC field. On write data operations, the WRITE GATE goes active at the end of this field.
FIELD LENGTH = 1 – 4 BYTES

(HEX 08) DATA READ SKEW

On READ DATA operations, the READ GATE goes active at the end of this field. This field is intended to allow the PLO to skip over the write splice area before it begins trying to sync onto the read data.
FIELD LENGTH = 1 – 64 BYTES

(HEX 09) DATA PLO LOCK-ON

The READ GATE goes active at this point.
FIELD LENGTH = 1 – 4 BYTES

(HEX 0A) PRE-DATA

The search for ADDRESS MARK starts here.
FIELD LENGTH = 1 – 64 BYTES

(HEX 0B) DATA ADDRESS MARK

See ID ADDRESS MARK
FIELD LENGTH FOR HARD DISK = 1 BYTE
FIELD LENGTH FOR FLOPPY = 3 BYTES

(HEX 0C) F8 BYTE

FIELD LENGTH = 1 BYTE (fixed)

(HEX 0D) DATA LOW
(HEX 0E) DATA HIGH

These two bytes define the length of the DATA FIELD

0D = Low Byte of DATA LENGTH
0E = High Byte of DATA LENGTH

FIELD LENGTH = 1 – 65,536 BYTES

(HEX 0F) DATA ECC

See ID CRC/ECC field.
FIELD LENGTH = 1 – 8 BYTES

(HEX 10) POST DATA

Data WRITES stop at the end of this field.
FIELD LENGTH = 1 – 4 BYTES

(HEX 11) INTER-RECORD GAP

This field provides a separation between each sector to allow speed tolerances; write to read recovery time (time between deassertion of WRITE GATE and assertion of READ GATE) head switching time and controller decision making time between sectors and variations in detecting INDEX and SECTOR.
FIELD LENGTH = 1 – 256 BYTES

(HEX 12) SECTORS PER TRACK

Write N-1 to this register
FIELD LENGTH = 1 – 256 BYTES

(HEX 13) ID START LOCATION

This register is set to specify which internal register follows the FE register in the ID field. This register is set as shown below.

ID Start Value	Next Byte Following FE	
00	FE	(causes FE to be used twice)
01	CYLINDER HI	(normal setting for hard disk)
02	CYLINDER LO	(normal setting for floppy)
03	HEAD	
04	SECTOR	
05	SECTOR SIZE	

(HEX 14) ADDRESS MARK FIRST HALF
(HEX 15) ADDRESS MARK SECOND HALF

HEX 14 = The first half of the encoded ADDRESS MARK
HEX 15 = The second half of the encoded ADDRESS MARK or the whole unencoded ADDRESS MARK when running in unencoded mode.

ADDRESS MARKS are special bytes recorded at the beginning of each ID and DATA field. These bytes are unique and do not occur anywhere else on the disk. They are used to identify the exact beginning of the ID and DATA fields. These ADDRESS MARKS are made unique by violating the rules for encoding the data.

When using MFM encoding, the ADDRESS MARK is an A1 data byte with one of the clock bits dropped.

MFM CLOCK BITS 0 0 0 0 1 1 1 0
DATA BITS 1 0 1 0 0 0 0 1

MFM ADDRESS MARK
01000100 10001001 = HEX 44 and HEX 89
└ This bit has been dropped
HEX 44 = First half in location HEX 14
HEX 89 = Second half in location HEX 15

Storage

When using UM83C021 RLL encoding, the ADDRESS MARK is a 4B data byte with one of the bits dropped. This results in a unique pattern with 8 zeros in a row.

	4B	010 010 11
RLL CODE FOR 4B		000100 000100 1000
RLL ADDRESS MARK		000100 000000 1000 = HEX 10 and HEX 08

This bit has been dropped

HEX 10 = First half in location HEX 14
HEX 08 = Second half in location HEX 15

In 2,7 RLL encoding, the maximum number of zeros in a row is 7.

(HEX 16) RECORDING CODE

80	00	NRZ WRITE DATA
40	01	NRZI WRITE DATA
	10	PULSE WRITE DATA
	11	
20	00	NRZ READ DATA
10	01	NRZI READ DATA
	10	PULSE READ DATA
	11	
08	000	UNENCODED
04	001	FM
02	010	MFM
	011	RLL 2,7
01	Should be 0	

(HEX 17) CLOCK DIVIDER

Through the use of a PLO divider circuit, the disk controller chip is capable of controlling several devices that do not operate at the same data rates without requiring a separate PLO circuit for each. For example, the controller can operate a hard disk, a floppy disk, and a tape drive using only a single PLO running at 10 MHz or 15 MHz. If running a 15 MHz PLO for an RLL encoded hard disk, the controller is divided by 15 to run the tape drive and divided by 30 to run the floppy disk.

The PLO divider can divide from 1 to 256. To divide by a number n, the number n-1 must be written into the Clock Divider at register address 17 hexadecimal.

In order to improve PLO lock-on performance, the Clock Divider is synchronized to the first data pulse at the beginning of every read operation.

Bytes that are written to or read from the UM83C021 at RAM CLOCK speed are internally synchronized to the WRITE CLOCK. This synchronization can take up to 5 write clock cycles. During this synchronization, the CONTROLLER BUSY bit (Status Register bit 7) will be one.

If additional bytes are written to or read from the chip during this synchronization, the results will be unpredictable.

When using a divided down clock, the length of time required for this synchronization may become significant. For example: when working with a 5-1/4 inch floppy, the disk clock would be 2 microseconds. The synchronization could take up to 5 x 2 = 10 microseconds. When designing your system, insure that reads and writes to the UM83C021 are always farther apart than 10 microseconds whenever the clock is divided down to a 2 microsecond period. This can be done by inserting extra instructions in the host program or by monitoring the CONTROLLER BUSY bit.

(HEX 18) FE

ID field identifier byte
Write FE to this register.

(HEX 19) F8

Data field identifier byte.
Write F8 to this register for hard disk or FB for floppies.

(HEX 1A) SECTOR SIZE

This byte follows the sector number in the ID field and is normally used with floppies – not with a hard disk.

(HEX 1B) SECTOR OPTIONS

The UM83C021 handles soft or hard sectored disks or ESDI disks using ESDI Address Marks. ESDI byte clock operation requires an external counter to create hard sector pulses.

BIT 7 to 2 = 0		
BIT 1	= 02	00 SOFT SECTORED
BIT 0	= 01	01 HARD SECTORED
		10 ESDI ADDRESS MARKS
		11 ESDI BYTE CLOCKS

(HEX 1C) GAP VALUE

Write 4E for MFM encoding
Write 33 for RLL encoding

(HEX 1E) DIRECTION

Bit 7 of the register is sent directly to the DIRECTION output pin. Writing a HEX 80 to this address will make the pin high; a HEX 00 will make it low. This pin is used for direction control of ST506 drives or for command data on ESDI drives.

(HEX 1F) STEP

Bit 0 of this register is sent directly to the STEP output pin. Writing a HEX 01 to this address will make the pin high; a HEX 00 will make it low. This pin is used for STEP CONTROL of ST506 drives or for TRANSFER REQUEST on ESDI drives. Auto-increment is disabled for this address because it must be written repetitively to create multiple STEP pulses at the drive interface.

(HEX 38) CYLINDER HI

This register contains the HI 8 bits of the cylinder number. The contents of this register and the next 3 registers are used for writing or searching for ID FIELDS on the disk.

(HEX 39) CYLINDER LO

This register contains the LO 8 bits of the cylinder number.

(HEX 3A) HEAD

This register contains the HEAD number.

(HEX 3B) SECTOR

This register contains the SECTOR number. On multi-sector operations, this register is incremented after each sector is read or written and may be read at address 07.

(HEX 3C) TRANSFER COUNT

This register contains the number of sectors desired for this command −1. On multi-sector operations, this register is decremented after each sector is read or written and may be read at address 06.

(HEX 3D) HEAD SELECT

When this register is written, the external $\overline{\text{SET HEAD}}$ pin strobes low to latch the head number from the data bus.

(HEX 3E) DRIVE SELECT

When this register is written, the external $\overline{\text{SET DRIVE}}$ pin STROBES low so that the external drive register can latch the drive number from the data bus.

(HEX 3F) DISK OP

Writing to this register starts or stops DISK READ or WRITE operations. The commands are listed below and are described in more detail in the DISK COMMAND section.

00 STOP DISK OPERATION
80 NO-OP
81 WRITE DATA
82 READ DATA
83 READ ID
84 WRITE FIRST SECTOR
85 WRITE NEXT SECTOR
86 FORMAT WRITE INTERLEAVED
87 FORMAT WRITE SEQUENTIAL
88 READ DATA IMMEDIATE
89 WRITE SECTOR IMMEDIATE
8A WRITE GAP IMMEDIATE
8B VERIFY DATA
8C READ LONG
8D WRITE LONG
8E COMPUTE ERROR SHORT, CORRECTION SPAN 5, 11 BITS
8F COMPUTE ERROR LONG, CORRECTION SPAN 11, 22 BITS

(HEX 40) DATA TO/FROM DISK

Data written to this register is serialized and sent as data to the disk. Writing to this register resets the DATA REQUESTED status bit (Bit 4). If data is not written fast enough to keep up with the disk, the OVERRUN/UNDERRUN status bit (register 05 Bit 1) will be set.

Read Register Address Descriptions

Register Address Decimal	Hex	Auto Inch Hex	Register		ECC 56 Bit	ECC 32 Bit	CRC 16 Bits
0	00	80	Not used				
1	01	81	Not used				
2	02	82	Not used				
3	03	83	Not used				
4	04	84	Disk status				
5	05	85	Controller status				
6	06	86	Transfer count				
7	07	87	Sector number				
8	08	88			Not used	Not used	Not used
9	09	89			0	Not used	Not used
10	0A	8A		Error	1	Not used	Not used
11	0B	8B		Syndrome	2	Not used	Not used
12	0C	8C		Bytes	3	0	Not used
13	0D	8D			4	1	Not used
14	0E	8E			5	2	0
15	0F	8F			6	3	1
64	40	C0 *	Data from disk				

* This address does not auto-increment

Table 4. Read Register Addresses

(HEX00 – HEX03) NOT USED

(HEX04) DISK STATUS

BIT 7 = DRIVE SELECTED/STATUS 1 (HEX 80)
This bit has a dual role when controlling a Winchester drive. It indicates that a drive has been successfully selected. This pin directly reads the logic level of pin 27 on the chip.

BIT 6 = READY/STATUS 0 (HEX 40)

This bit also has a dual role. When controlling floppy and Winchester drives, it indicates that a drive is up to speed and ready for read or write. This pin directly reads the logic level of pin 21 on the chip.

BIT 5 = SECTOR ADDRESS MATCH (HEX 20)

This bit is set when a sector ID matches what was set into the Sector Address Registers during a read/write operation.

BIT 4 = LAST SECTOR ON TRACK (HEX 10)

This bit is set during the last sector of a track. (Sector # in ID field = Sector per track.) See Multi-Sector transfers.

BITS 3 THRU 0 = FIELD COUNTER

The FIELD COUNTER indicates what field is passing under the heads on a read or write.

FIELD COUNT	HEX COUNT	FIELD LOCATION ON DISK
0	00	INTER-RECORD GAP or POST-INDEX GAP
1	01	ID PLO LOCK-ON
2	02	PRE-ID
3	03	ID AM
4	04	FE
5	05	ID
6	06	ID ECC
7	07	POST-ID
8	08	DATA READ SKEW
9	09	DATA PLO LOCK-ON
10	0A	PRE-DATA
11	0B	DATA AM
12	0C	F8
13	0D	DATA
14	0E	DATA ECC
15	0F	POST-DATA

(HEX 05) CONTROLLER STATUS

BIT 7 = NO RECORD FOUND (HEX 80)

Indicates that on a read or write, the controller has received two successive index pulses without finding an ID field that matched the Sector Address registers. Sector pulses are not input on the INDEX pin).

BIT 6 = MISSING DATA AM (F8 MISCOMPARE) (HEX 40)

This bit is set if the byte after the Data Address Mark does not match the contents of register 19, the Data Field Indentifier byte, indicating that a data field probably does not exist.

BIT 5 = ID ECC/CRC ERROR (HEX 20)

When set indicates that a read/write sector to the addressed sector was found, but that the CRC/ECC was in error.

BIT 4 = DATA ECC ERROR (HEX 10)

When set indicates that a read of the addressed sector was found, but that the DATA field CRC/ECC bytes was in error.

BIT 3 = DATA MISMATCH (HEX 08)

Indicates that the Verify command has stopped with a data mismatch error. See Verify command.

BIT 2 = DATA TRANSFER STOPPED (STOP RECEIVED) (HEX 04)

Indicates that during a read or write the DMA-STOP pin was activated and that the transfer has stopped.

BIT 1 = OVERRUN/UNDERRUN (HEX 02)

Indicates that data was not transferred to or from the controller quick enough for the Serializer/Deserializer section.

BIT 0 = NOT USED

(HEX 06) TRANSFER COUNT

This register contains the number of sectors remaining (including the current) for Multi-sector operations and it is decremented after each successful sector read or write.

(HEX 07) SECTOR NUMBER

This register contains the SECTOR NUMBER for the operation that the controller is currently performing. It is incremented after each multi-sector operation but is not incremented if an error occurs.

(HEX 08) NOT USED

(HEX 09) 56 BIT ECC SYNDROME BYTE 0

(HEX 0A) 56 BIT ECC SYNDROME BYTE 1

(HEX 0B) 56 BIT ECC SYNDROME BYTE 2

(HEX 0C) 56 BIT ECC SYNDROME BYTE 3

(HEX 0D) 56 BIT ECC SYNDROME BYTE 4

(HEX 0E) 56 BIT ECC SYNDROME BYTE 5

(HEX 0F) 56 BIT ECC SYNDROME BYTE 6

Disk Commands

Writing to the COMMAND register at location 3F causes a disk operation to begin. All registers used in the disk operation should be set up prior to writing to the COMMAND register.

(HEX 00) ABORT

This command will immediately terminate any operation in progress.

(HEX 80) NO OP

This command causes no disk operation.

(HEX 81) WRITE DATA

This command writes data from memory into the data field of the sector whose address has been written into the sector address registers in the chip. Multi-sector writes are possible up to 256 sectors.

(HEX 82) READ DATA

This command reads the data field from the sector whose ID has been set into the registers on the disk controller. The data field is transferred to memory by DMA. It may optionally be transferred under program control if the disk speed is slow enough for the computer to keep up with it. The F8 byte immediately following the data address mark is not transferred but is checked to assure that a data field is present.

At the end of every sector transfer, the Transfer Count is checked. If it is zero, the operation stops. If it is non-zero, it is decremented, the sector number is incremented, and the next sector is read. This process continues until the Transfer Count goes to zero, the end of the track is reached, or an error occurs.

The DMA data transfer may be stopped by having $\overline{STOP}$ go low during a DMA cycle ($\overline{ACK}$ low). If this happens, the disk controller will immediately cease data transfer and will halt the operation at the end of the current sector. In this case, the Transfer Count will not be decremented and the sector number will not be incremented.

The residual Transfer Count and the sector number registers can be read to determine where to continue.

(HEX 83) READ ID

This command reads the next ID fields and ID ECC fields that are encountered on the disk or tape. It transfers both fields to memory. The ID ECC field is checked for errors.

It can be used to establish track orientation on tape or disk. It can also be used in error recovery procedures to determine if the read-write heads are positioned over the correct track.

(HEX 84) WRITE FIRST SECTOR

This command begins writing at the Index Pulse and writes both ID fields and data fields. Information for the ID field comes from the internal sector address registers. Information for the data fields is transferred from memory.

Multi-sector writes can write up to 256 sectors.

If this command is terminated by the transfer count going to zero, it stops writing at the end of the post-data field of the last sector. If this command is terminated by the sectors per track counter going to zero, it will continue writing the postdata field until the next Index Pulse is reached or until a Reset Command (00 hexadecimal) is received.

This command can be used to format and write data to a track in a single operation.

(HEX 85) WRITE NEXT SECTOR

This command begins writing at the end of the post-data field of the sector whose address has been set into the internal sector address registers. It writes ID fields as well as data fields. It stops writing at the end of the post-data field when the transfer count goes to zero.

Multi-sector writes can be done up to 256 sectors.

This command can be used to repair the ID field of a damaged sector.

(HEX 86) FORMAT INTERLEAVED

This command is similar to the Format Sequential (See HEX 87) command. However, in this command the ID fields to be written on the disk come from memory rather than from the internal registers on the ID Numbers written are totally programmable and can be interleaved in any manner desired.

For each sector written the disk controller will fetch all bytes of the ID field plus one byte of filler (usually a hexadecimal E5) for the data field. The hexadecimal FE byte immediately following the ID Address Mark is not fetched from memory but is written from the internal register in the disk controller.

For a typical hard disk format the ID field length would be 4, and the following 5 bytes would be fetched from memory for each sector.

Cylinder High
Cylinder Low
Head
Sector
Data Filler Byte (usually E5)

If the track is being formatted with 26 sectors, then a total of 5 x 26 = 130 bytes will be fetched from memory during the Format Interleaved command execution.

(HEX 87) FORMAT SEQUENTIAL

This command is used to format a single track on a disk. It begins writing at index and continues writing to the next index. It writes all ID and data fields using the information set into the on-chip ID and DATA registers.

ID Byte	Register Address	Data Filler Byte	Register Address
CYLINDER HI	HEX 38	DATA	HEX 40
CYLINDER LO	HEX 39		
HEAD	HEX 3A		
SECTOR SIZE	HEX 1A		

After each sector is written, the sector number register is incremented by one and the track size register is decremented by one. When the track size register reaches zero, one last sector is written and the remainder of the track is written with zero.

No data is transferred to or from memory during a format sequential command.

(HEX 88) READ DATA IMMEDIATE

It differs in that when it is issued, the track orientation counters are reset to the post-index gap and the read operation begins there. It is intended primarily for use when controlling tape drives where there is no index pulse to establish position on the track. With this command the microprocessor is responsible for maintaining track orientation.

Data transfer occurs the same as with the Read Data command. Up to 256 sectors can be transferred with a single command.

(HEX 89) WRITE IMMEDIATE

Write Immediate is a formatting type write in that it writes the ID field of each sector as well as the data field. It is intended primarily for use when controlling tape where there is no index pulse to establish track orientation. When it is issued, the track orientation counters are set to post-index gap and WRITE GATE goes high immediately.

ID field information is written from the internal sector address registers. Data field information is transferred from memory. The sector number is incremented after every sector is written. Up to 256 sectors can be written with a single Write Immediate command.

Writing stops at the end of the post-data field when the transfer count goes to zero.

If Write Immediate is terminated by the physical sector count going to zero, the controller will continue writing the post-data field until it is stopped by the microprocessor issuing a Reset Command (00 hexadecimal) or until an Index Pulse is received. This allows tapes to be written with a long trailer gap after the last data block.

(HEX 8A) WRITE GAP IMMEDIATE

When the Write Gap command is issued, the track orientation counters are set to post-index gap and the controller immediately begins writing zeroes. Writing continues until index is reached or until this command is terminated by issuing another command or a halt command.

This command is intended primarily for writing header or trailer zero fields on tape.

(HEX 8B) VERIFY DATA

This command begins reading data from the disk at the addressed sector and comparing it to the data transferred from memory. If the disk data and the data from memory do not match, this command will terminate with the Data Mismatch bit set (Read Register 05 bit 3).

(HEX 8C) READ LONG

This command is used primarily for checking the ECC and CRC circuitry. It reads and transfers to memory the data field and data ECC field of the addressed sector.

The ID ECC field and the data ECC field are checked and error latches are set if they are not correct. An error in the ID ECC field will not stop the data field from being transferred as it would with the Read Data command. However, an error in either ECC field will terminate a multi-sector Read Long at the end of the post-data field of the sector containing the error.

After using the Read Long command, the ECC Syndrome registers containing the ECC bits read from the disk instead of error bits.

This command also allows the reading of records that were written by controllers that use different ECC or CRC generators.

(HEX 8D) WRITE LONG

This command is used primarily for checking the ECC and CRC circuitry. It writes from memory the data field and the data ECC field of the addressed sector. This command permits the creation of errors to assist in testing the error detection circuits.

An error in the ID ECC field will not prevent writing to the addressed sector.

(HEX 8E) COMPUTE ERROR

This command is used to compute ECC error. It's correction span is 5 & 11 bits for 32 & 56 bits ECC.

(HEX 8F) COMPUTE ERROR LONG

This command is used to compute ECC error. It's correction span is 11 and 22 bits for 32 and 56 bits ECC.

Timing Specs and Diagrams

This section is devoted to the timing of signals and their relationship to each other in order to make the maximum use of the UM83C021. The following tables and diagrams are to be used as design tools when incorporating the UM83C021 into your system.

Signal	Min.	Typ.	Max.	Unit
XTAL		20		MHz
PLO		20		MHz
READ DATA		10		MBITS/SEC

Table 5. Signal Frequencies

Signal	LO	HI	Unit
XTAL	13	20	NANOSECONDS
PLO	13	20	
MCLK	30	30	
RESET	100		

Table 6. Signal Widths

Delays From	To	Min.	Typ.	Max.	Unit
XTAL HI	WRITE DATA		35	70	NANOSECONDS
XTAL	WRITE CLOCK		30	60	
XTAL OR PLO HI	REQUEST LO		32	63	
ACK & MCLK LO	REQUEST HI		36	72	
MCLK LO	SET HEAD LO		30	59	
MCLK HI	SET HEAD HI		21	42	
MCLK LO	SET DRIVE LO		30	59	
MCLK HI	SET DRIVE HI		21	42	
XTAL OR PLO HI	DIRECTION		43	85	
XTAL OR PLO HI	STEP		38	77	
CSEL HI OR WRT LO	D0-D7 TRI-STATE		25	50	
CSEL LO & WRT HI	D0-D7 ACTIVE		29	57	
ACK HI OR WRT LO	D0-D7 TRI-STATE		31	61	
ACK LO & WRT HI	D0-D7 ACTIVE		29	57	
XTAL HI	WRGT		32	63	
PLO HI	RDGT		36	71	
XTAL OR PLO HI	ENAM		36	71	
XTAL OR PLO HI	BUSY		31	62	
RDEL HI	FSTR HI		26	51	
PLO HI	FSTR LO		26	51	
PLO HI	SLWR LO		26	51	
RDEL HI	SLWR HI		26	51	

Table 7. Delays

From Changing Signal	Set-Up	To	Hold	Unit
ACKNOWLEDGE	4.0	RAMCLK LO		NANOSECONDS
ACKNOWLEDGE		RAMCLK HI	0	
WRITE	15	RAMCLK LO		
WRITE		RAMCLK HI	15	
CHIP SELECT	15	RAMCLK LO		
CHIP SELECT		RAMCLK HI	15	
A0	15	RAMCLK LO		
A0		RAMCLK HI	15	
NOTE THAT ALL THE ABOVE SIGNALS SHOULD CHANGE WHEN RAMCLK IS HIGH AND BE STABLE WHEN RAMCLK IS LOW				
DATA (D0 – D7)	2	RAMCLK HI	12	NANOSECONDS
STOP	6	RAMCLK HI	3	

Table 8. Set Up and Hold Time

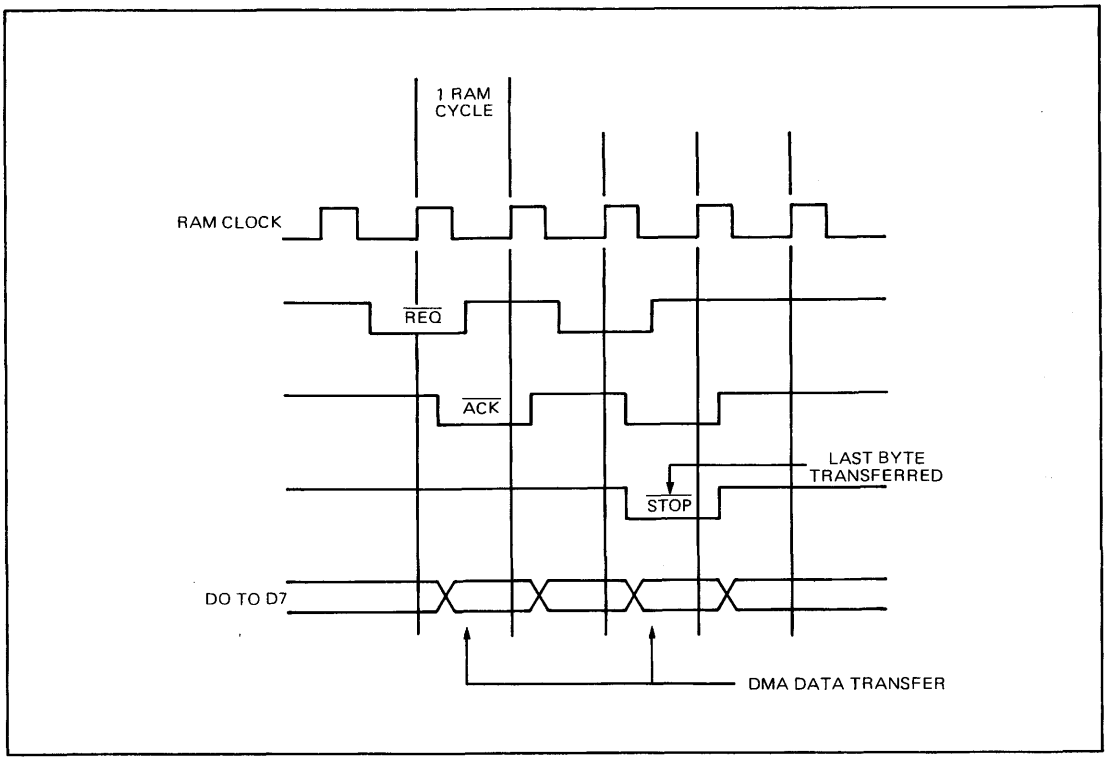


Figure 4. DMA Data Transfer Cycles

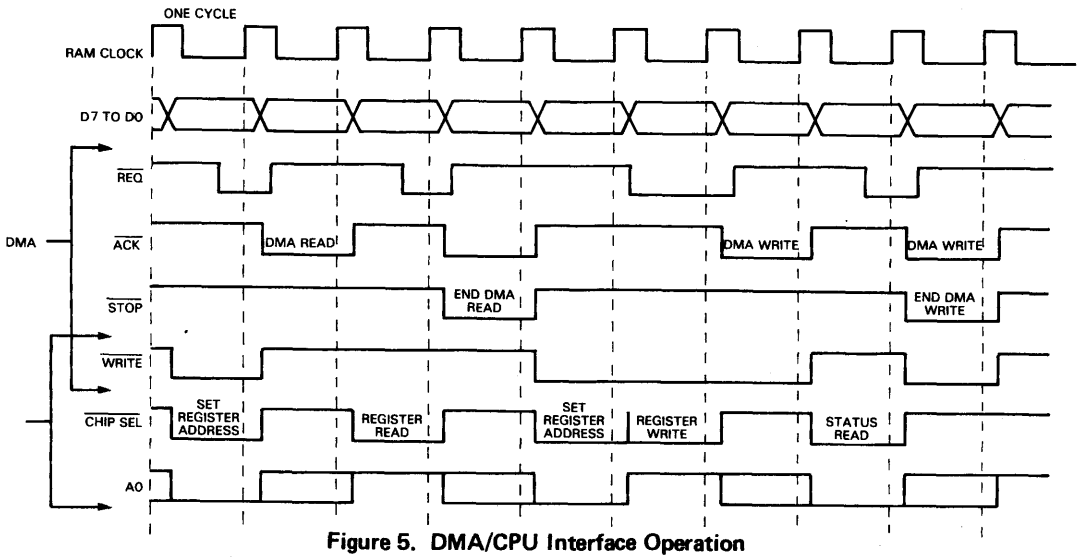


Figure 5. DMA/CPU Interface Operation

UM83C022

AT HDC Interface

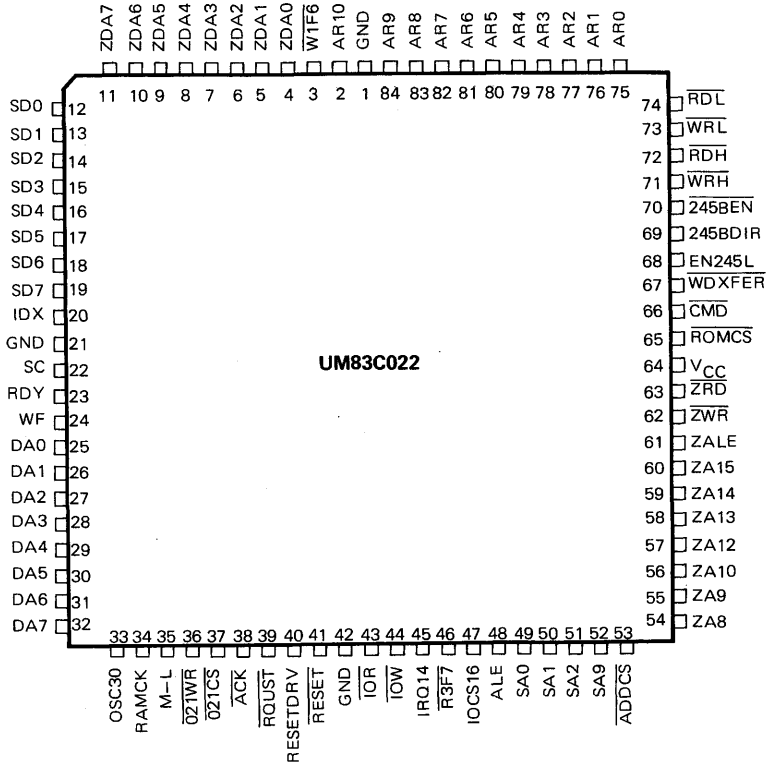
Features

- IBM PC/AT interface compatible
- Jumper selectable for RLL/MFM disk interface
- 1:2 interleave
- Buffer size 4k bytes
- Sector size 512 bytes
- 84-pin PLCC package

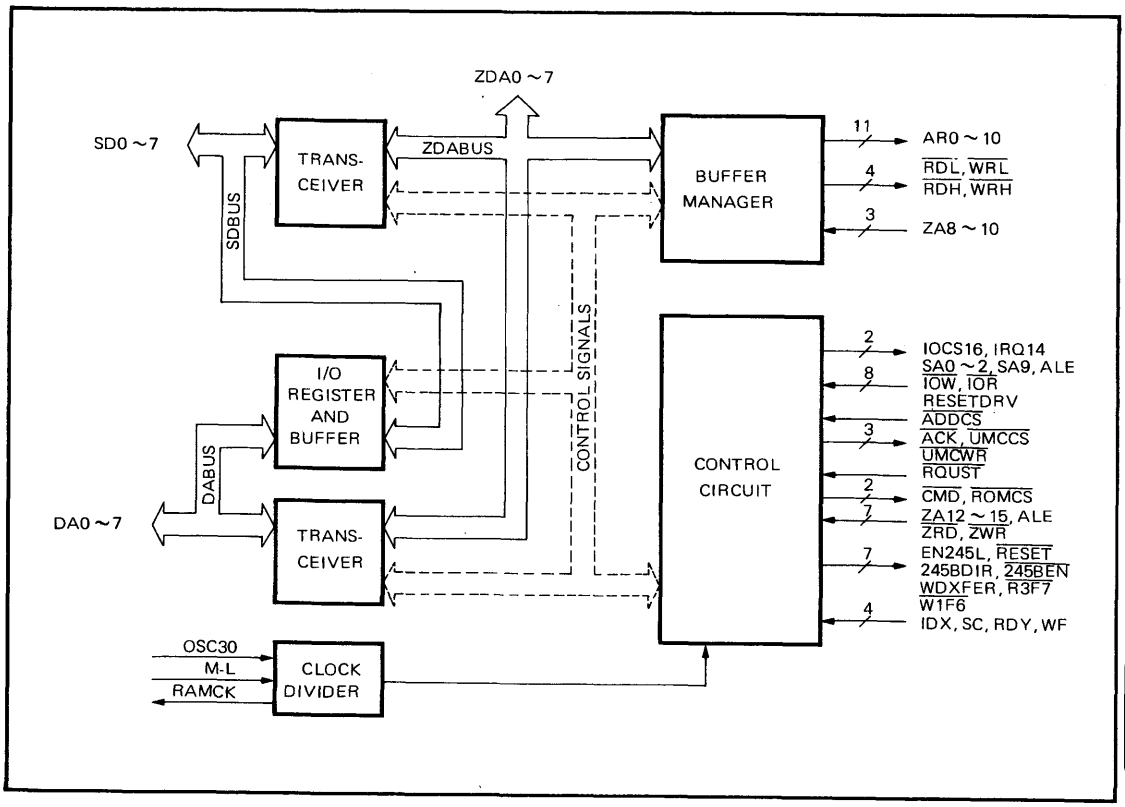
General Description

UM83C022 is a component for Winchester disk controller interface applications. It is designed to attach two 5.0/7.5 Mbit/sec MFM/RLL encoded ST-506 (ST-412) Winchester disk drives to IBM PC/AT compatible personal computers. The controller implements the host interface and the command set compatible to the original IBM PC/AT Disk Controller. UM83C022 supports the 4K-byte sector buffers, and track formats compatible to IBM PC/AT hard disk formats.

Pin Configuration



Block Diagram



Absolute Maximum Ratings *

Power Supply Voltage, V_{DD} . . . . . −0.5 to +7.0V

Input Voltage, V_I . . . . . −0.5V to V_{DD} + 0.5V

Operating Temperature, T_{OPT} . . . . . −40 to +85°C

Storage Temperature, T_{STG} . . . . . −65 to +150°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = 0°C to 70°C, V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Min.	Max.	Unit	Conditions
V_{IL}	Input Low Voltage	–	0.8	V	
V_{IH}	Input High Voltage	2.0	–	V	V_{DD} = 5V V_{IN} = 0 – 5V
I_I	Input Leakage Current	–	± 50	μA	All others pin = 0V
V_{OL}	Output Low Voltage	–	0.4	V	I_{OL} = 8 mA V_{DD} = 5V
V_{OH}	Output High Voltage	2.4	–	V	I_{OH} = −8 mA V_{DD} = 5V

AC Characteristics (T_A = 0°c to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Min.	Max.	Unit	Conditions
T1	Address setup to EN245L low		25	ns	
T2	Address setup to EN245L high		25	ns	
T3	$\overline{IOR}$/$\overline{IOW}$-pulse width	100		ns	
T4	$\overline{IOR}$ setup to $\overline{RDL}$, $\overline{RDH}$ low		25	ns	
T5	$\overline{IOR}$ setup to $\overline{RDL}$, $\overline{RDH}$ high		20	ns	
T6	$\overline{IOW}$ setup to $\overline{WRL}$, $\overline{WRH}$ low		25	ns	
T7	$\overline{IOW}$ setup to $\overline{WRL}$, $\overline{WRH}$ low		20	ns	
T8	Address setup to IOCS16 low		25	ns	
T9	Address setup to $\overline{WDXFEF}$ low		25	ns	
T10	RAMCK setup to $\overline{ACK}$ low		20	ns	
T11	RAMCK setup to $\overline{WRL}$ low or to $\overline{RDL}$ low		20	ns	
T12	RAMCK setup to $\overline{WRL}$ high or $\overline{RDL}$ high		20	ns	
T13	RAMCK setup to $\overline{WRH}$ low or to $\overline{RDH}$ low		20	ns	
T14	RAMCK setup to $\overline{WRH}$ high or $\overline{RDH}$ high		20	ns	

Pin Description

Pin No.	Symbol	I/O	Description
2	AR10	O	Address 10 for buffer address decoding.
3	$\overline{W1F6}$	O	Write I/O port 1F6H/176H to select hard disk drive.
4-11	ZDA0 ~ 7	I/O	Data (address) bus for translation among HOST interface, CONTROLLER, and BUFFER.
12-19	SD0 ~ 7	I/O	System data bus provides bits 0 through 7 for PC bus.
20	IDX	I	INDEX pin provided by drive to indicate the beginning of a track.
22	SC	I	This signal, seek complete, goes active when the R/W head settles on the desired track at the end of a seek command.
23	RDY	I	Ready, when this signal and SC are active, it indicates the drive is ready to Read, Write, and Seek and the I/O signals are ready.
24	WF	I	Write fault, the signal means an improper operation of the disk at the driver.
25-32	DA0 ~ 7	I/O	These signals are provided for 8031 to control the address and data used.
33	OSC30	I	Provides 30 MHz oscillation signal.
34	RAMCK	O	This signal provides 10/15 MHz clock for UM83021 and 8031 to synchronize all CPU and DMA operations.
35	M-L	I	This signal is used to identify MFM (high) or RLL (low) drive operation.
36	$\overline{021WR}$	O	This signal is driven by the 8031 address decoder to indicate whether a register read or write is to be performed in the UM83C021.
37	$\overline{021CS}$	O	UM83C021 chip selection, this signal is driven by 8031's address port to enable the registers of the UM83C021 to be read or written. The address port is 4000H-5FFFH.
38	$\overline{ACK}$	O	Acknowledge, this signal is driven low to response UM83021 DMA transferring request.
39	$\overline{RQUST}$	I	This request signal is used in conjunction with the $\overline{ACK}$ signal for handshaking during the UM83C021 DMA transferring.
40	RESETDRV	I	This signal is active high to clear the system status.
41	$\overline{RESET}$	O	This signal provides external logic reset capability.
43	$\overline{IOR}$	I	PC-BUS I/O read operation control.
44	$\overline{IOW}$	I	PC-BUS I/O write operation control.

Pin Description (Continued)

Pin No.	Symbol	I/O	Description
45	IRQ14	O	Interrupt request to HOST.
46	$\overline{R3F7}$	O	Read I/O port 3F7H/377H control.
47	IOCS16	O	This signal indicates the present operation is a 16-bit data transfer I/O cycle.
48	ALE	I	This signal latches the valid addresses from the HOST.
49-52	SA0 ~ 3 SA9	I	This signal indicates the present operation is a 16-bit data transfer I/O cycle.
53	$\overline{ADDRCS}$	I	Address chip select decoded from SA3 ~ 8.
54-60	ZA8 ~ 10 ZA12 ~ 15	I	Local address bus from 8031 to be used as high-byte address and control pins.
61	ZALE	I	Local address latch from 8031.
62	$\overline{ZWR}$	I	Looal write enable from 8031.
63	$\overline{ZRD}$	I	Local read enable from 8031.
65	$\overline{ROMCS}$	O	This signal is used to enable the external ROM of the 8031 from 0000H-1FFFH.
66	$\overline{CMD}$	O	This signal is used to interrupt the 8031 when the HOST issues the command execution request.
67	$\overline{WDXFER}$	O	This signal indicates the 16-bit data transfer operation.
68	EN245L	O	Enables low-byte data bus to be transferred between the PC-BUS and UM83C022.
69	245BDIR	O	This signal determines whether the data flow is from the high-byte buffer or from the low-byte buffer.
70	$\overline{245BEN}$	O	This signal enables the transfer between ZDA0 ~ 7 and high-byte buffer.
71	$\overline{WRH}$	O	Write high-byte data to SRAM buffer.
72	$\overline{RDH}$	O	Read high-byte data from SRAM buffer.
73	$\overline{WRL}$	O	Write low-byte data to SRAM buffer.
74	$\overline{RDL}$	O	Read low-byte data from SRAM buffer.
75-84	AR0 ~ 9	O	These signals are provided for the external SRAM buffer addresses.
1, 21, 42	GND	I	Ground.
64	V_{CC}	I	Power supply +5V.

Functional/Register Description

A. HOST CONTROLLER/DRIVE STATUS REGISTER (Read Only)

This register specifies the status of the controller/drive. This register may be accessed by the HOST at any time, however, when the BUSY bit is set, no other bits in the register are valid. Also by reading this register, I/O address 1F7H/166H, any pending interrupts to the HOST are cleared.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BUSY	RDY	WF	SC	DRQ	CORD	IDX	ERROR

Bit 0 ERROR: This bit is set when an error has occurred on the last command or power up diagnostics. The error code is stored in the buffer with address 27F9H and can be accessed by the HOST with I/O address 1F1H.

Bit 1 INDEX: This bit reflects the status of INDEX signal (I/P Pin 20) from the selected disk drive. This signal goes active once per revolution of the disk. This bit will not be set if the drive is not ready (i. e. if Bit 6 is reset).

Bit 2 ECC CORRECTION DATA: This bit is set whenever (on the previous read sector transfer) a sector read off the disk had a correctable ECC error which was corrected.

Bit 3 DATA REQUEST: This bit is set for data transfer to/from the sector buffer. This includes both sector and ECC data. The controller is considered "busy" whenever the DRQ or BUSYL bits are set.

Bit 4 SEEK COMPLETE: This bit indicates the state of the Seek Complete signal (I/P Pin 22) from the selected disk drive. This bit is set when the drive is not seeking.

Bit 5 WRITE FAULT: This bit reflects the state of the Write Fault Signal (I/P Pin 24) from the selected disk drive. When this bit is set, it indicates that the drive is unsafe for read/write transfer.

Bit 6 READY: This bit reflects the state of the Ready signal (I/P Pin 23) from the selected disk drive. When this bit is set, the drive is present, but may not be ready for read/write transfer.

Bit 7 BUSY: When this bit is set, the controller is executing a command. Also, when this bit is set, the HOST may not read or write any other task files except the AT HOST CONTROLLER/DRIVE STATUS REGISTER.

B. HOST FIXED DISK REGISTER (Write Only)

This fixed disk register is used by the HOST to control some of the internal functions. Its I/O port address is 3F6H/376H.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	HS3EN	RST	INTEN	X

Bit 0, 4 ~ 7: Don't care.

Bit 1 INTERRUPT ENABLE: This bit, when reset, enables the IRQ14 (Pin 45) output. When this bit is set, the IRQ14 output is tri-state, regardless of the presence or absence of a pending interrupt. The internal signal and the status will still be valid.

Bit 2 SOFTWARE RESET: Writing a 1 to this bit will cause this IC to be reset. The reset output will be asserted and will remain asserted until this bit is written back to 0.

Bit 3 HEAD SELECT 3 ENABLE: When this bit is set, the Head Select 3 will be output by the local microcontroller. When this bit is reset, the Reduce Write Current will be output by the local microcontroller.

C. MICROCONTROLLER STATUS REGISTER (Read Only)

This register is used to indicate the status of operation and drive for the microcontroller. It's I/O address is 6000H.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	WF	HS3ENB	HS3EN	RDY	SC	ML	DRQ

Bit 1 MFM or RLL mode: When set, it indicates the drive is a MFM recorded drive.

Bit 4, 5 HEAD SELECT 3 ENABLE: These two bits are used to select the Head Select 3 or the Reduce Write Current Operation. The bit 4 reflects the bit 3 of host fixed disk register.

Others are the same as the HOST CONTROLLER/DRIVE STATUS REGISTER.

D. MICROCONTROLLER COMMAND REGISTER (Write Only)

This register is used to control the data operation and sends out the status of the operation. Its I/O address is 8000H sent from the microcontroller.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SBUSY	SETINT	SDRQB	DMAWRB	CRESETB	LONG	CORD	ERROR

Bit 0 ERROR: This bit indicates that a non-recoverable error has occurred. The error information is stored in the buffer and this bit is connected to the bit 0 of HOST CONTROLLER/DRIVE STATUS Register.

Bit 1 ECC CORRECTION DATA: This bit is connected to the bit 2 of HOST CONTROLLER/DRIVE STATUS REGISTER as a report for the data correction.

Bit 2 LONG: When this bit is set, it is used to indicate the Long Command for the read/write operation. This bit must be set before transferring data between Host and buffer for read/write LONG command.

Bit 3 ACKNOWLEDGE RESET: This bit is used to set the Acknowledge signals for the read/write operations of the HDC.

Bit 4 DMA READ/WRITE CONTROL: This bit is set for the read operation of HDC from the drive. When reset, it indicates a write operation of HDC to the drive.

Bit 5 SET DATA REQUEST: This bit, when reset, sets the DRQ bit in Status Register.

Bit 6 SET INTERRUPT: When changed from low to high, this bit is used to set the interrupt request to the HOST.

Bit 7 SBUSY: This bit is used to set the BUSY bit of the HOST CONTROLLER/DRIVE STATUS REGISTER to indicate that the μC is busy except when DRQ is asserted.

E. MICROCONTROLLER READ/WRITE I/O PORT

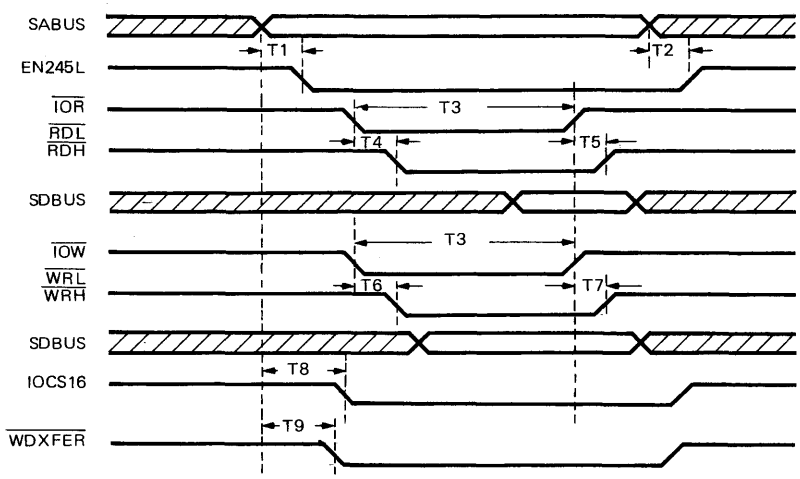
Writing to the A000H port will clear the bit 7 (BUSY) of the HOST CONTROLLER/DRIVE STATUS REGISTER if the SBUSY bit is reset.

Reading from the A000H port will generate a low-active pulse to initiate the buffer (SRAM) control signals.

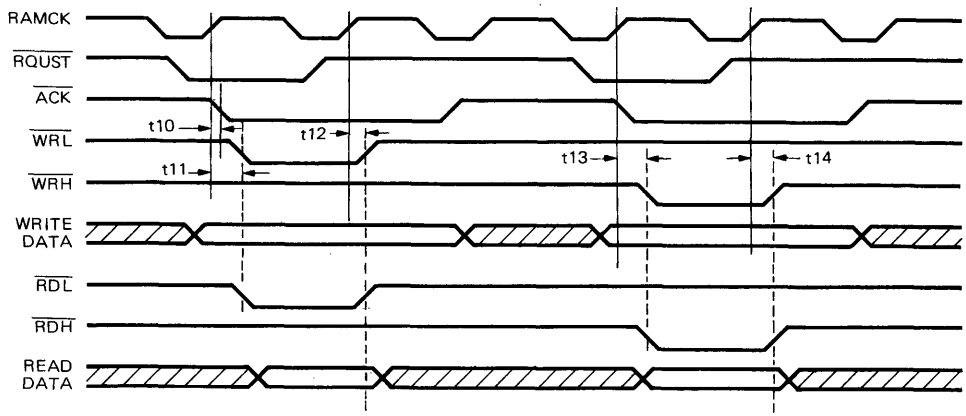
Writing to the C000H port will reset the bit 3 (DRQ) of the HOST CONTROLLER/DRIVE STATUS REGISTER and clear the internal interrupt (IRQ14) to the host.

Writing to the E000H port will set the bit 3 (DRQ) of the HOST CONTROLLER/DRIVE STATUS REGISTER.

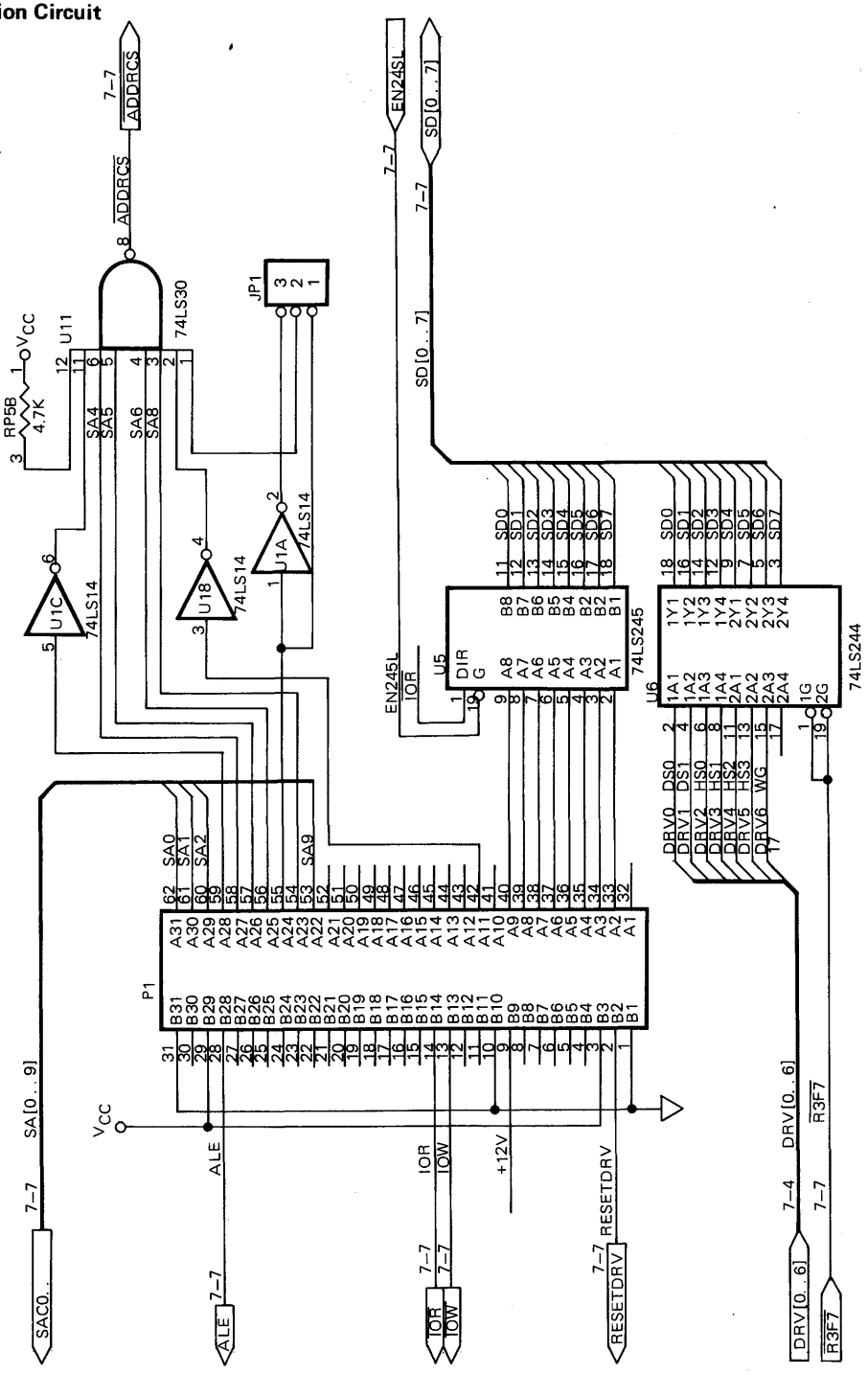
Host Interface Timing



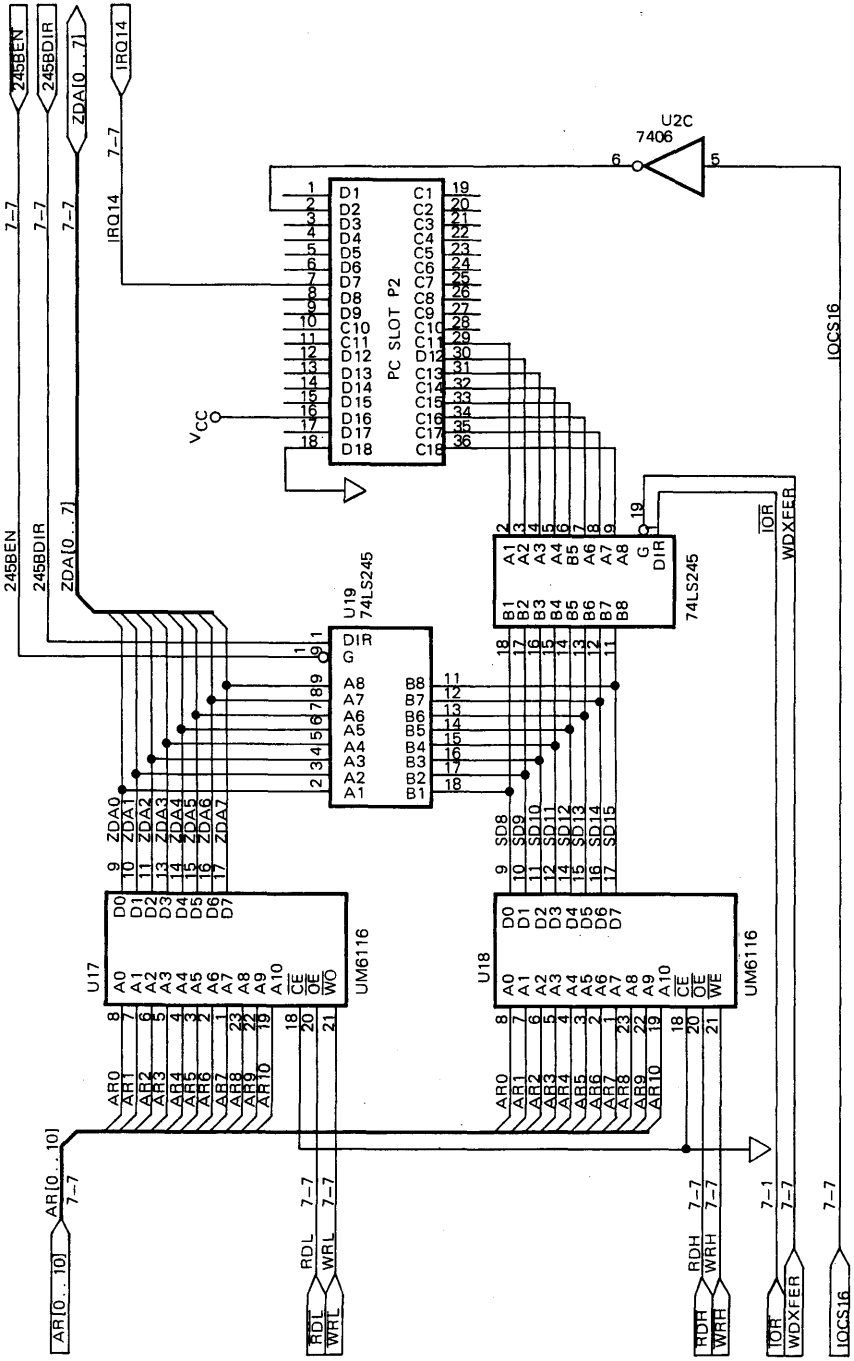
DMA Read/Write Timing



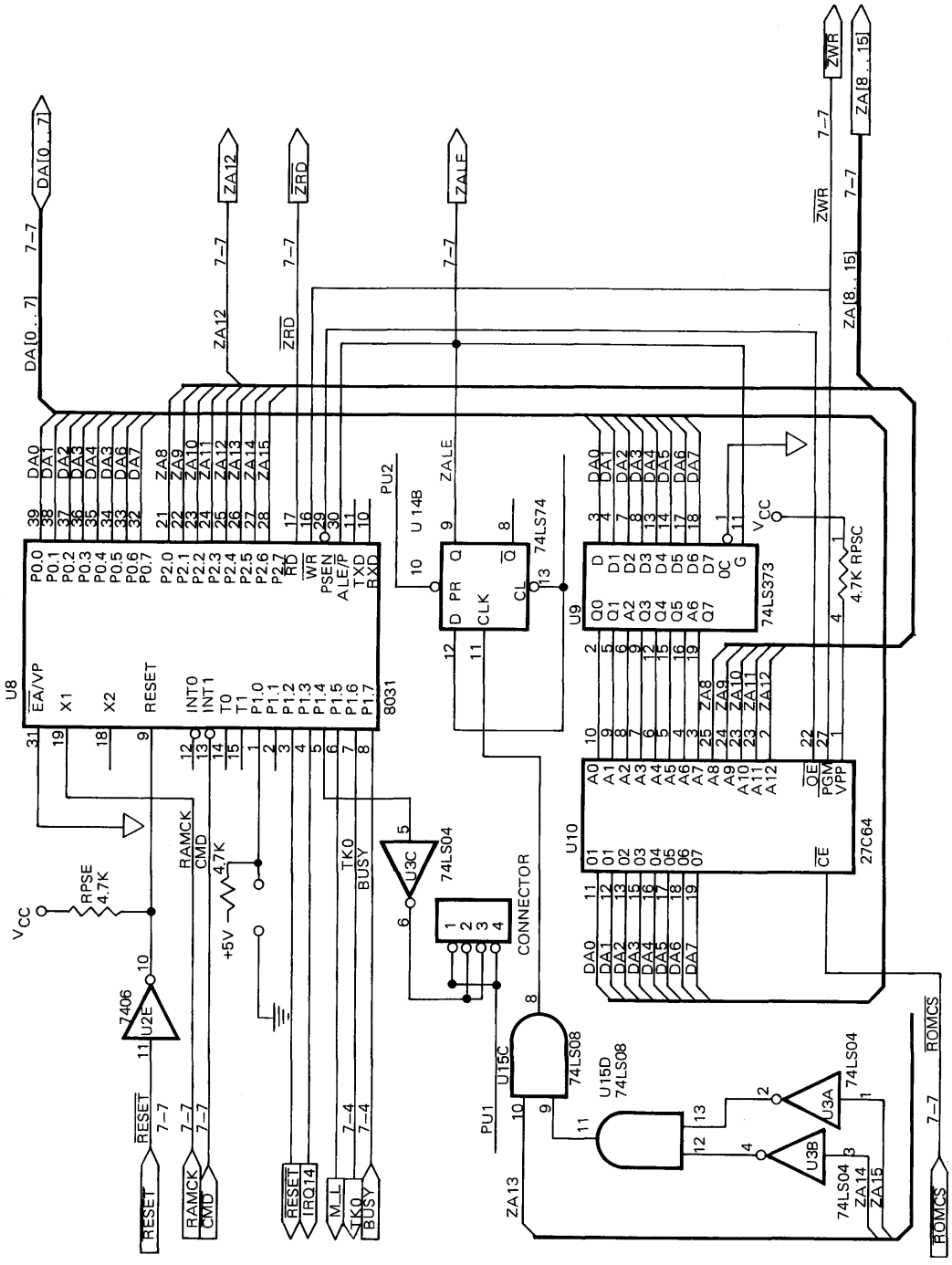
Application Circuit



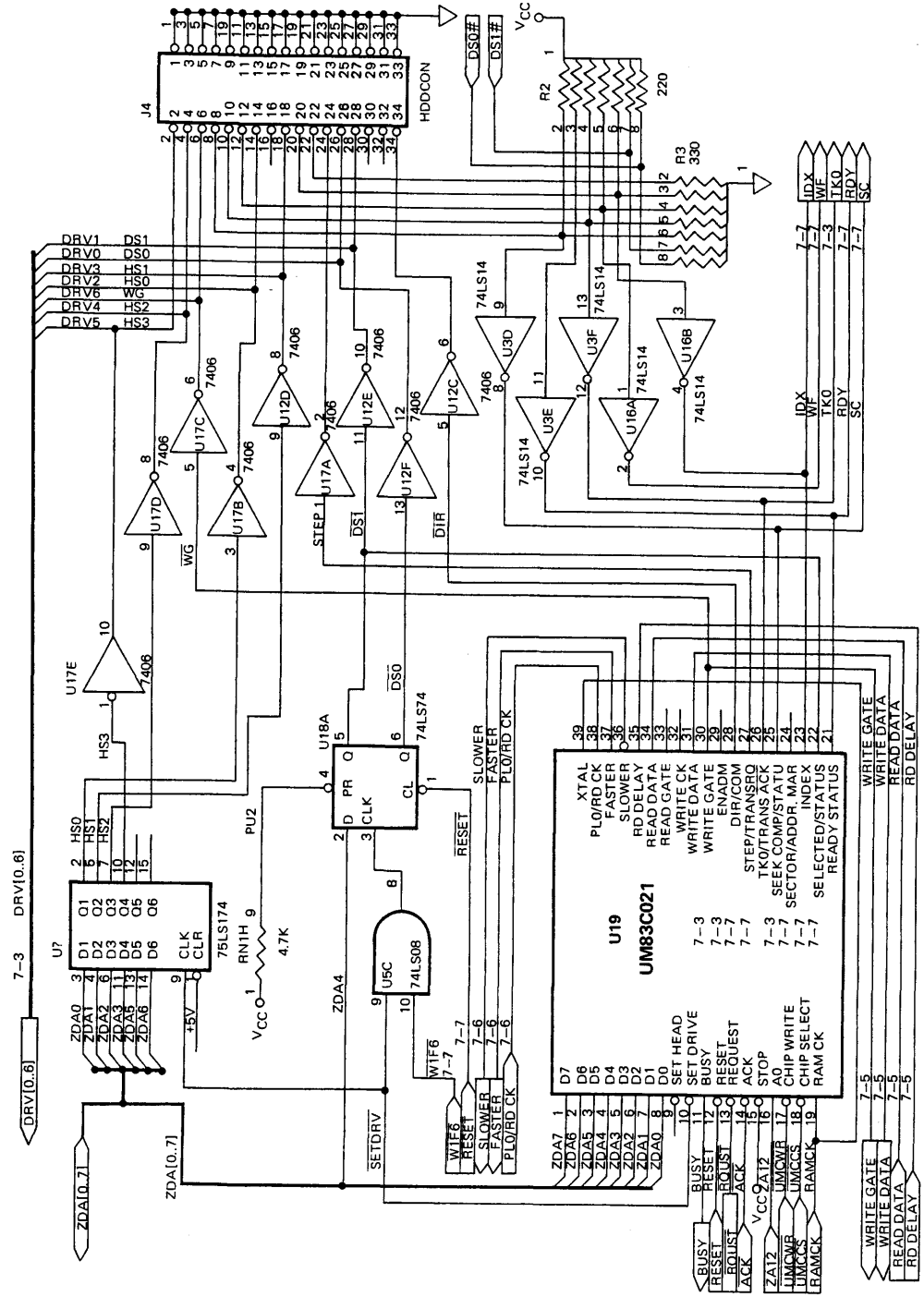
Application Circuit (Continued)



Application Circuit (Continued)

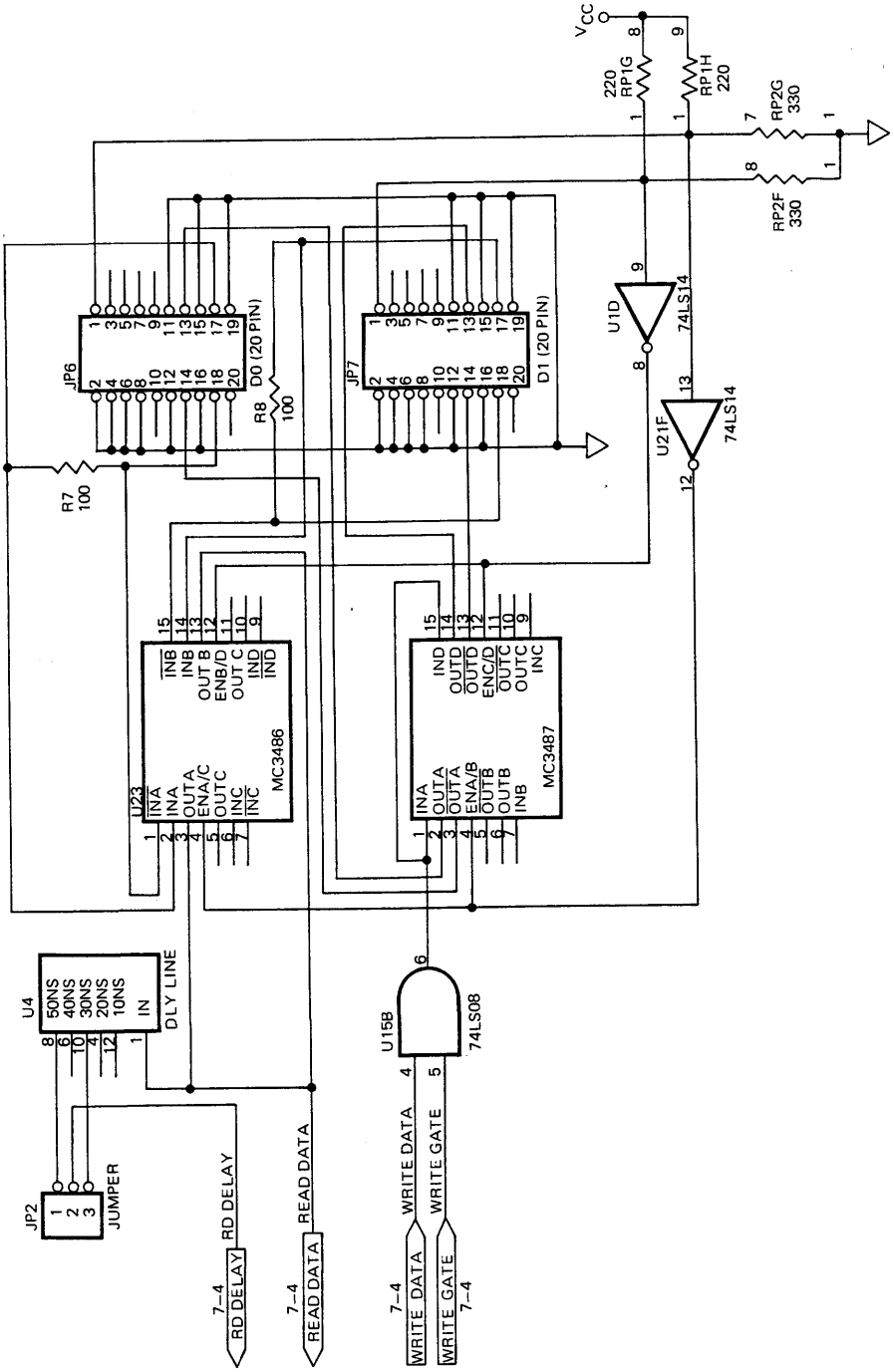


Application Circuit (Continued)

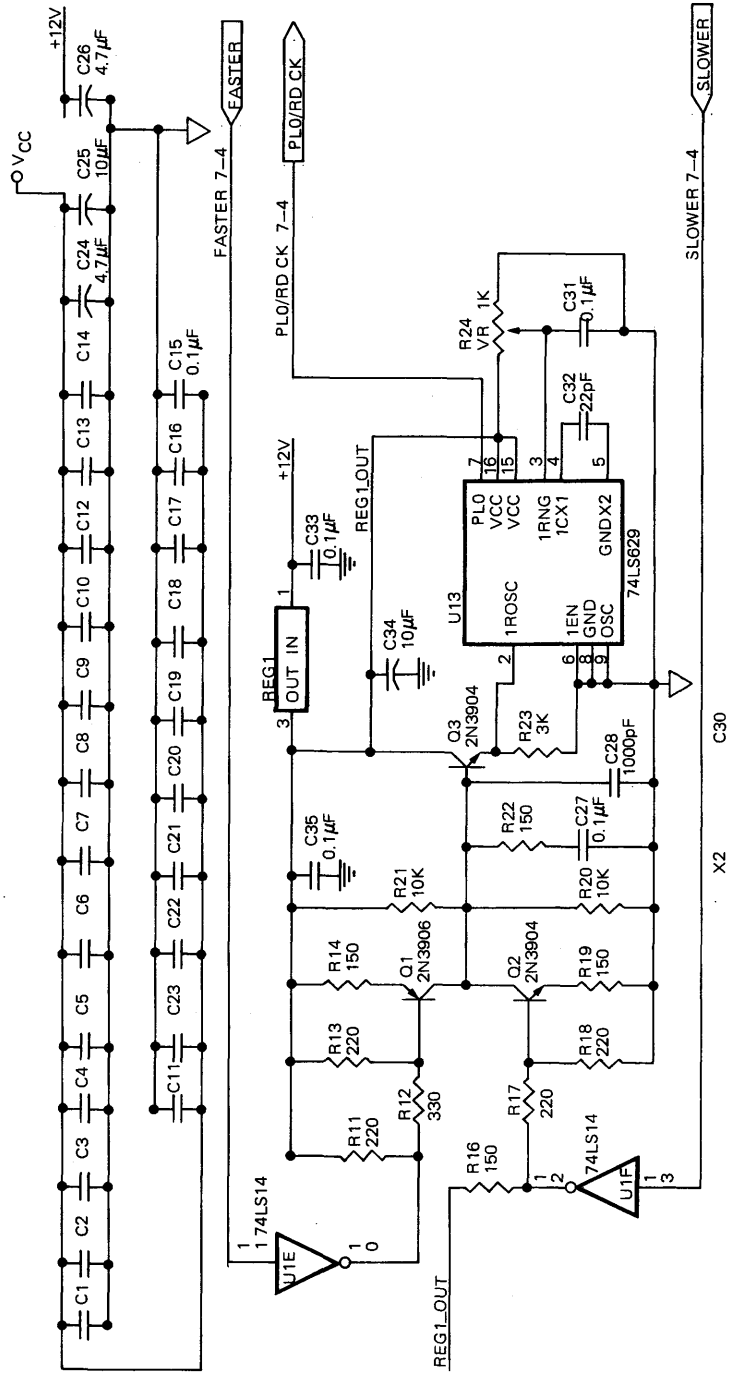


Storage

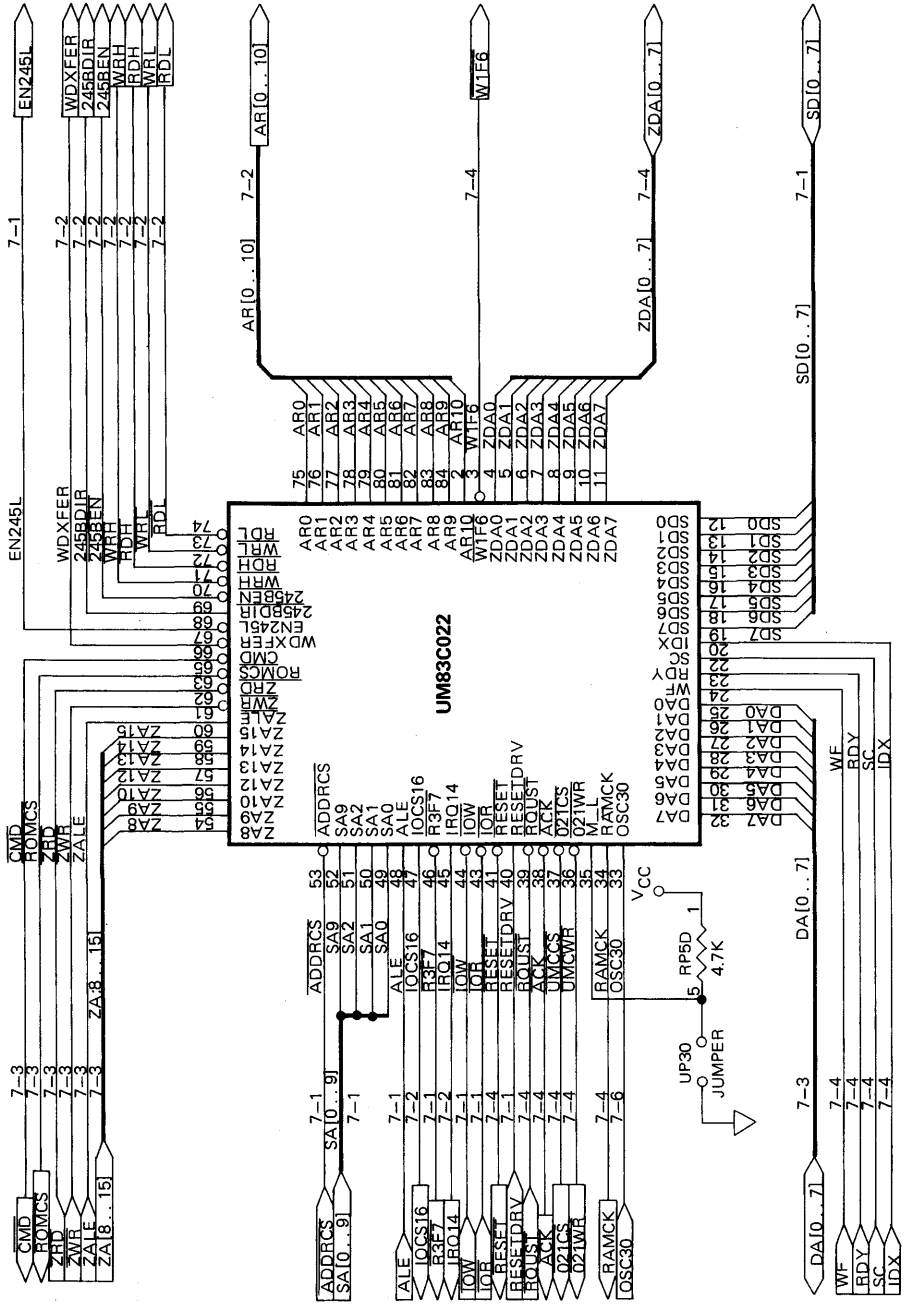
Application Circuit (Continued)



Application Circuit (Continued)



Application Circuit (Continued)



B. AT Interface I/O port

Task file – primary 1F0H to 1F7H (Secondary 170H to 177H) and 3F6H to 3F7H (Secondary 376H to 377H)

Primary	Secondary	ADDRESS	SA9	SA2	SA1	SA0	Read Port Function	Write Port Function
1F0H	170H	0	0	0	0	0	Read data (16 bits)	Write data (16 bits)
1F1H	171H	0	0	0	0	1	Error register	Write precomp cylinder
1F2H	172H	0	0	0	1	0	Sector count	Sector count
1F3H	173H	0	0	0	1	1	Sector number	Sector number
1F4H	174H	0	0	1	0	0	Cylinder number low	Cylinder number low
1F5H	175H	0	0	1	0	1	Cylinder number high	Cylinder number high
1F6H	176H	0	0	1	1	0	SDH	SDH
1F7H	177H	0	0	1	1	1	Status Register	Command register
3F6H	376H	0	1	1	1	0	Alternate status register	Fixed disk register
3F7H	377H	0	1	1	1	1	Digital input register	Not used

C. Microcontroller Task File Read/Write Port

HEX	READ PORT FUNCTION	WRITE PORT FUNCTION
27F9	write precomp register	error register
27FA	sector count	sector count
27FB	sector number	sector number
27FC	cylinder number low	cylinder number low
27FD	cylinder number high	cylinder number high
27FE	SDH	SDH
27FF	host command register	not used

D. Constraints

The PC/AT HDC supports two ST-506/412 Winchester disk drives. The host bus has to be IBM PC/AT BUS or compatible. The BIOS command set must be compatible to the original BIOS of IBM PC/AT. If RLL encoded drive is used, the BIOS must also contain RLL drive type or user defined drive type. If running on network environment, it might not be compatible to WD's HDC.

UMC

UM8326/B

Floppy Disk Data Separator (FDDS)

Features

- Performs complete data separation for floppy disk drives
- Separates FM or MFM-encoded data from any magnetic media
- Eliminates several SSI and MSI devices normally used for data separation
- No critical adjustments required
- Compatible with Standard Microsystems' FDC 1791, FDC 1793 and other floppy disk controllers
- Small 8-pin dual-in-line package
- +5 Volt only power supply
- TTL-compatible inputs and outputs

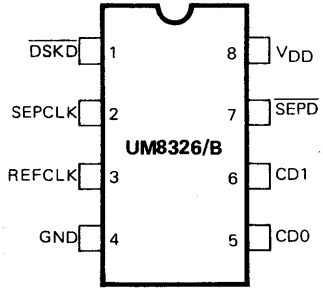
General Description

The Floppy Disk Data Separator provides a low-cost solution to the problem of converting a single stream of pulses from a floppy disk drive into separate clock and data inputs for a floppy disk controller.

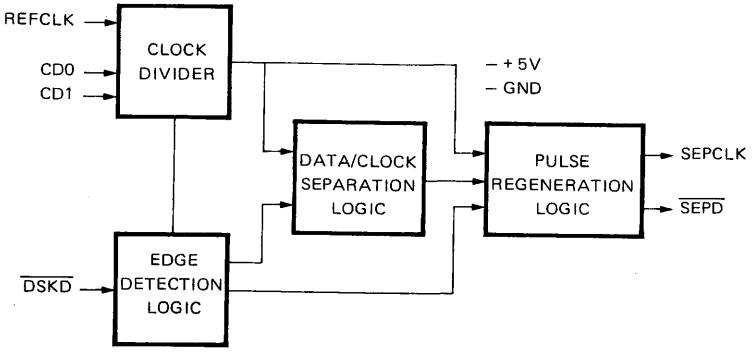
The FDDS consists primarily of a clock divider, a long-term timing corrector, a short-term timing corrector, and a re-clocking circuitry. Supplied in an 8-pin dual-in-Line package to save board real estate, the FDDS operates on +5 volts only and is TTL-compatible on all inputs and outputs.

The UM8326/B is available in two versions: The UM8326, which is intended for 5¼" disks, and the UM8326B for both 5¼" and 8" disks.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Operating Temperature Range . . . . . 0°C to + 70°C
Storage Temperature Range . . . . . −55°C to + 150°C
Positive Voltage on any Pin, with respect to ground
. . . . . + 8.0V
Negative Voltage on any Pin, with respect to ground
. . . . . − 0.3V

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = 0°C to 70°C, V_{DD} = +5V ± 5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Conditions
INPUT VOLTAGE LEVELS					
Low Level V_{IL}			0.8	V	
High Level V_{IH}	2.0			V	
OUTPUT VOLTAGE LEVELS					
Low Level V_{OL}			0.4	V	I_{OL} = 1.6 mA
High Level V_{OH}	2.4			V	I_{OH} = −100μA
INPUT CURRENT					
Leakage I_{IL}			10	μA	$0 \leqslant V_{IN} \leqslant V_{DD}$
INPUT CAPACITANCE					
All Inputs			10	pF	
POWER SUPPLY CURRENT					
I_{DD}			60	mA	

AC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
f_{CY}	REFCLK Frequency	0.2		4.3	MHz	UM8326
f_{CY}	REFCLK Frequency	0.2		8.3	MHz	UM8326B
t_{CKH}	REFCLK High	50		2500	ns	
t_{CKL}	REFCLK Low	50		2500	ns	
t_{SDON}	REFCLK to SEPD "ON" Delay		100		ns	
t_{SDOFF}	REFCLK to SEPD "OFF" Delay		100		ns	
t_{SPCK}	REFCLK to SEPCLK Delay	35			ns	
t_{DLL}	DSKD Active Low	0.1		100	μs	
t_{DLH}	DSKD Active High	0.2		100	μs	

Pin Description

Pin No.	Symbol	Designation	Description
1	$\overline{DSKD}$	$\overline{Disk\ Data}$	Data input signal direct from disk drive. Contains combined clock and data waveform.
2	SEPCLK	Separated Clock	Clock signal output from the FDDS derived from floppy disk drive serial bit stream.
3	REFCLK	Reference Clock	Reference clock input
4	GND	Ground	Ground
5, 6	CD0 CD1	Clock Divisor	CD0 and CD1 control the internal clock divider circuit. The internal clock is a submultiple of the REFCLK according to the following table: CD1 CD0 Divisor 0 0 1 0 1 2 1 0 4 1 1 8
7	$\overline{SEPD}$	$\overline{Separated\ Data}$	$\overline{SEPD}$ is the data output of the FDDS
8	V_{DD}	Power Supply	+5 volt power supply

Operational Description

A reference clock (REFCLK) of between 2 and 8 MHz is divided by the FDDS to provide an internal clock. The division ratio is selected by inputs CD0 and CD1. The reference clock and division ratio should be chosen per table 1.

The FDDS detects the leading edges of the disk data pulses and adjusts the phase of the internal clock to provide the SEPARATED CLOCK output.

Separate short and long-term timing correctors assure accurate clock separation.

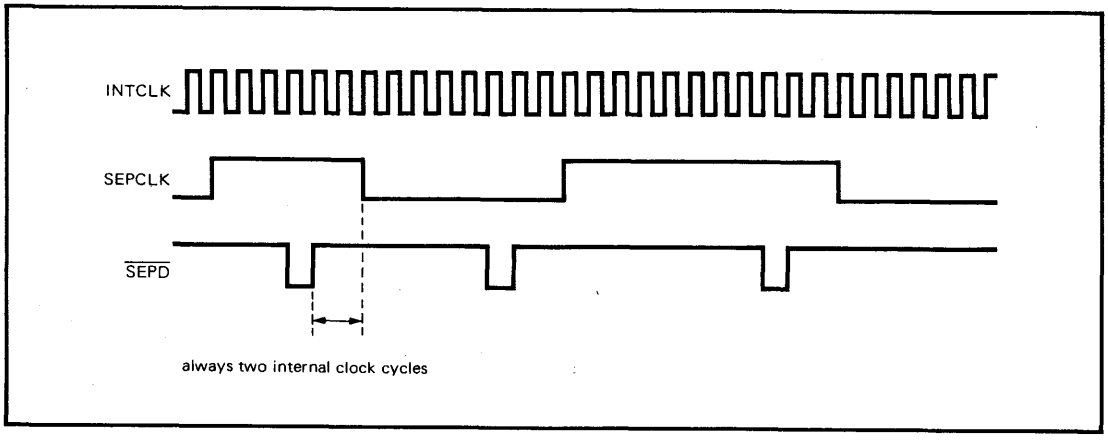
The internal clock frequency is nominally 16 times the SEPCLK frequency. Depending on the internal timing correction, the internal clock may be a minimum of 12 times to a maximum of 22 times the SEPCLK frequency.

The reference clock (REFCLK) is divided to provide the internal clock according to pins CD0 and CD1.

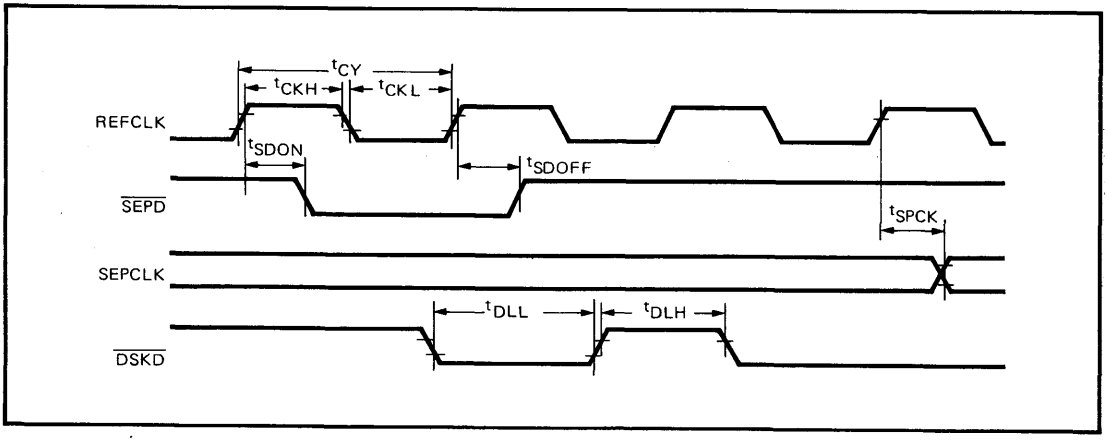
Table 1. Clock Divider Selection Table

Drive (8" or 5¼")	Density (DD or SD)	REFCLK MHz	CD1	CD0	Remarks
8	DD	8	0	0	All selectable
8	SD	8	0	1	
8	SD	4	0	0	
5¼	DD	8	0	1	
5¼	DD	4	0	0	
5¼	SD	8	1	0	
5¼	SD	4	0	1	
5¼	SD	2	0	0	

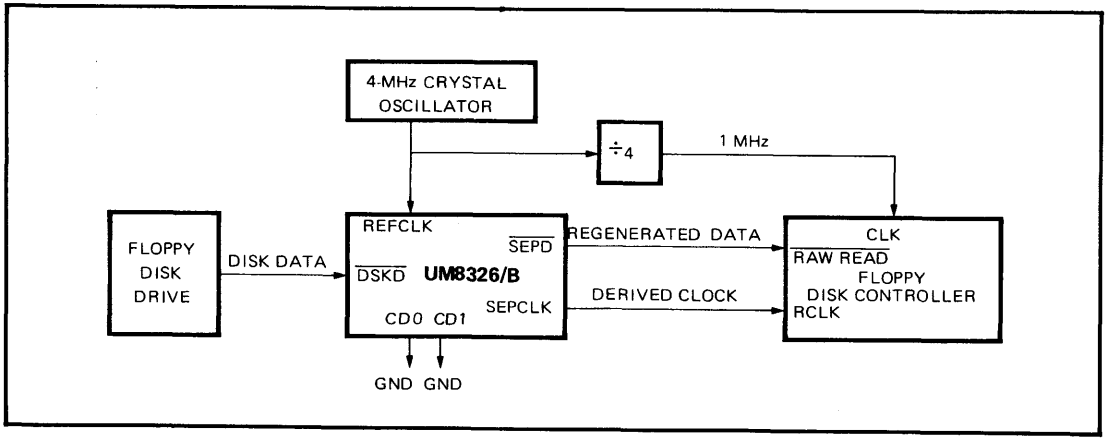
Timing Diagram (1)



Timing Diagram (2)



Typical System Configuration (5¼" Drive, Double Density)



Ordering Information

Part Number	Frequency Option	Drives	Package Type
UM8236	4 MHz	5¼"	8L DIP
UM8326B	8 MHz	5¼", 8"	8L DIP

UMC

PRELIMINARY

UM8388

Single-Chip Floppy Disk Controller

Features

- IBM PC XT/AT drive system compatible
- Supports 2 drives (MS-DOS support)
- 1.44M/1.2M/360K/720K format selectable
- IBM PC drive system address decoder
- Only 4 components needed for the drive
- Internal write precompensation circuit; precompensation values: 250-125 ns
- Internal data separator circuit
- Supports 8", 5¼", and 3½" drives

General Description

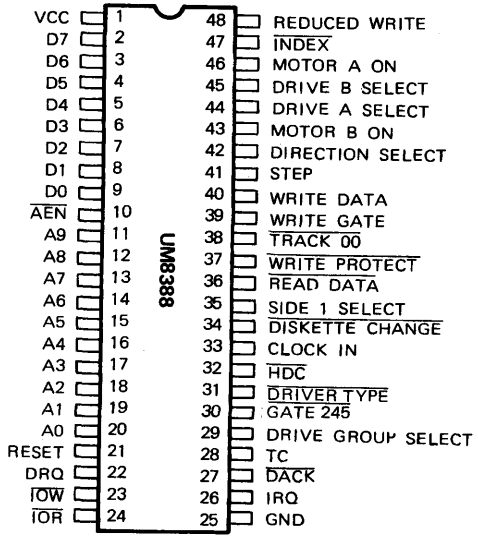
The UM8388 is a VLSI Floppy Disk Controller (FDC) chip, which contains the circuitry and control functions for interfacing a processor with up to 2 floppy disk drives. It is capable of supporting 360K Bytes, 1.2M Bytes (in 5¼" diskette drives), 720K Bytes, and 1.44M Bytes, (in 3½" diskette drives) FDDs using MFM coded, and double sided recording. UM8388 includes an internal data separator, write precompensation, circuit address decoder, timing control and other control logics. It simplifies design of a diskette drive system and only 4 components are needed in the IBM PC/AT drive system.

Handshaking signals are provided in UM8388 which makes DMA operation easy to incorporate with the aid of an external DMA control chip. The FDC will operate in either the DMA or Non-DMA mode. In the Non-DMA mode, the FDC generates interrupts to the processor every time a data byte is available. In the DMA mode, the processor needs only to load the command into the FDC and all data transfers occur under control of the UM8388 and DMA controller.

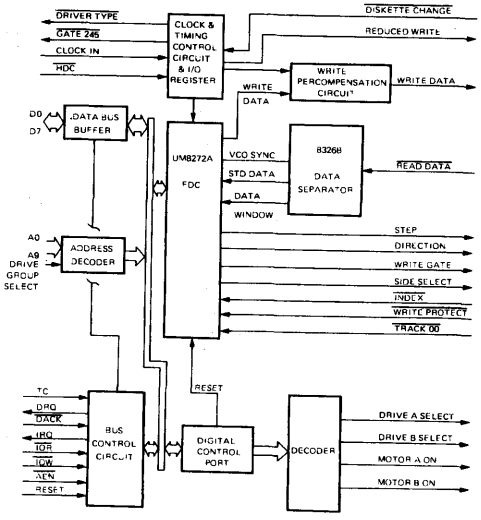
Many diskette drive parameters are programmable and a write-protection feature is supported. One interrupt level is used to indicate when an operation is completed, or a status condition requires the microprocessor's attention.

Storage

Pin Configuration

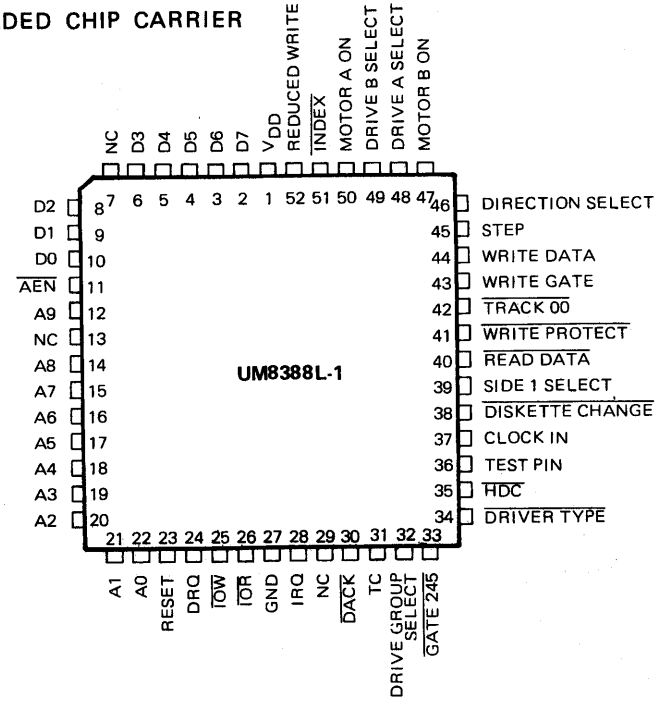


Block Diagram

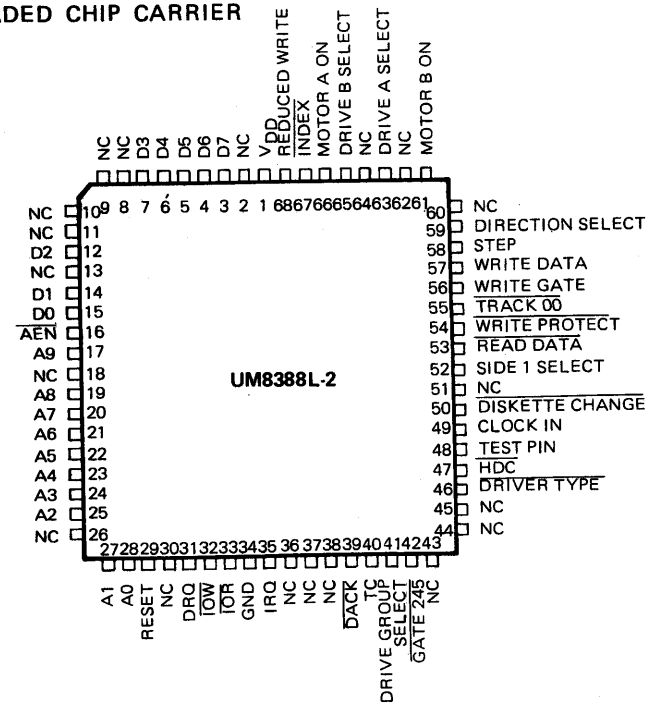


Pin Configurations

52 PIN PLASTIC LEADED CHIP CARRIER



68 PIN PLASTIC LEADED CHIP CARRIER



Absolute Maximum Ratings*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . −55°C to +150°C
All Output Voltages . . . . . −0.5 to +7 Volts
All Input Voltages . . . . . −0.5 to +7 Volts
Supply Voltage V_{CC} . . . . . −0.5 to +7 Volts
Power Dissipation . . . . . 1 Watt

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = 0°C to +70°C, V_{CC} = +5V ± 5%)

Symbol	Parameter	Limits		Unit	Conditions
		Min.	Max.		
V_{IL}	Input low voltage		0.8	V	
V_{IH}	Input high voltage	2.0		V	
V_{OL}	Output low voltage		0.4	V	I_{OL} = 8.0 mA
V_{OH}	Output high voltage	2.4	V_{CC}	V	I_{OH} = 4.0 mA
I_{CC}	V_{CC} supply current		200	mA	
I_{IL}	Input leakage current		10	μA	$0 \leqslant V_O \leqslant V_{CC}$
I_{LOH}	High level output leakage current		10	μA	$V_O = V_{CC}$
I_{OFL}	Output float leakage current		10	μA	$0.4V \leqslant V_O \leqslant V_{CC}$

AC Characteristics (T_A = 0°C to + 70°C, V_{CC} = +5.0V ± 10%)

PROCESSOR WRITE CYCLE

Symbol	Parameter	Min.	Max.
t_{AW}	address setup to $\overline{IOW}$ ↓	10 ns	
t_{WA}	address hold from $\overline{IOW}$ ↑	5 ns	
t_{WW}	$\overline{IOW}$ pulse width	250 ns	
t_{DW}	data setup to $\overline{IOW}$ ↑	150 ns	
t_{WD}	data hold from $\overline{IOW}$ ↑	10 ns	
t_{WI}	IRQ delay from $\overline{IOW}$ ↑		500 ns*

PROCESSOR READ CYCLE

Symbol	Parameter	Min.	Max.
t_{AR}	address setup to $\overline{IOR}$ ↓	10 ns	
t_{RA}	address hold from $\overline{IOR}$ ↑	5 ns	
t_{RR}	$\overline{IOR}$ pulse width	250 ns	
t_{RD}	data delay from $\overline{IOR}$ ↓		230 ns
t_{DF}	output floating delay from $\overline{IOR}$ ↑	10 ns	30 ns
t_{RI}	IRQ delay fro $\overline{IOR}$ ↑		500 ns*

Note: *: The values are for 8 MHz clock rate, multiply timings by 2/1.67 when using 4/4.8 MHz clock rates.

DMA OPERATION*

Symbol	Parameter	Min.	Max.
t_{ROCY}	DRQ cycle period	13 μs	
t_{AKRO}	$\overline{DACK}$ ↓ to DRQ ↓		200 ns
t_{ROR}	DRQ ↑ to $\overline{IOR}$ ↓	800 ns	
t_{ROW}	DRQ ↑ to $\overline{IOW}$ ↓	250 ns	
t_{RORW}	DRQ ↑ to $\overline{IOR}$ ↑ or $\overline{IOW}$ ↑		12 μs

Terminal Count, Reset, Index

Symbol	Parameter	Min.	Typ.	Max.
t_{IDX}	index pulse width		$10t_{CY}$**	
t_{TC}	terminal count width	$1t_{CY}$		
t_{RST}	reset width	$14t_{CY}$		

Notes:
* : The values listed for DMA operation are for 8 MHz clock rate, multiply timings by 2/1.67 when using 4/4.8 MHz clock rates.
**: t_{CY} is the clock rate of Drive System.

FDD INTERFACE

Symbol	Parameter	Min.	Typ.	Max.
t_{WDD}	write data width		125/208/250 ns*	
t_{WCY}	write data cycle time		1/1.67/2 μs*	
t_{RDD}	read data active time (low)	40 ns	125/208/250 ns*	
t_{RCY}	read data cycle time		1/1.67/2 μs*	

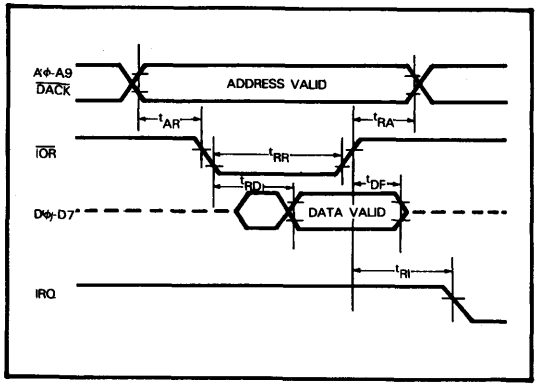
SEEK OPERATION***

Symbol	Parameter	Min.	Typ.	Max.
t_{STP}	step active time		5 μs	
t_{SC}	step cycle time	33 μs		
t_{DST}	DIR setup to step ↑	1 μs		
t_{STD}	DIR hold from step ↓	24 μs		

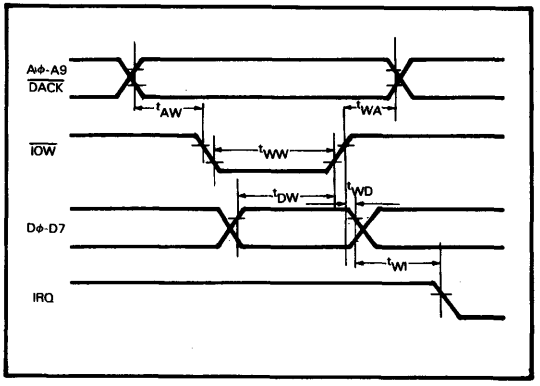
Notes:
* : The specified values are for 8/4.8/4 MHz respectively.
***: The values listed for seek operation are for 8 MHz clock period, multiply timings by 2/1.67 when using 4/4.8 MHz clock rates.

Timing Waveforms

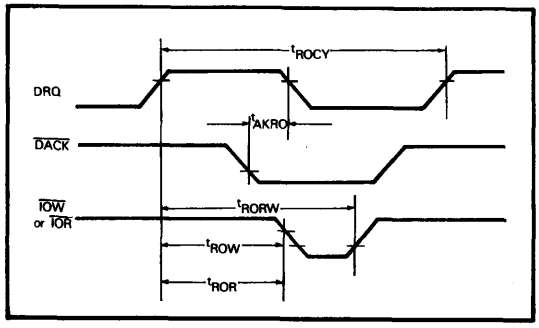
Processor Read Operation



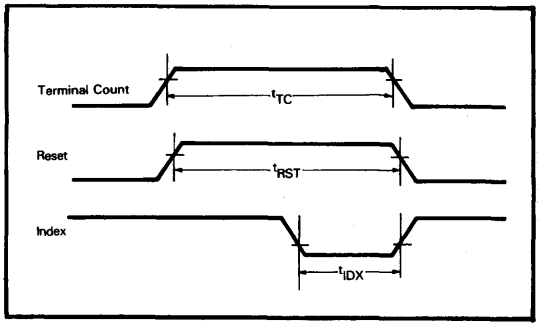
Processor Write Operation



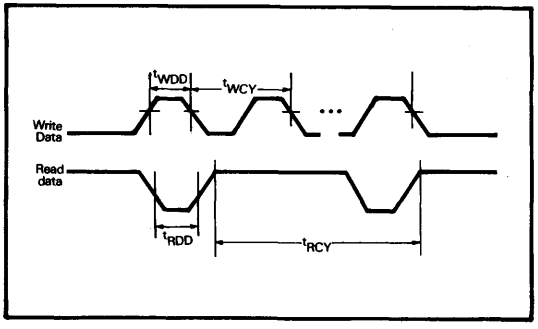
DMA Operation



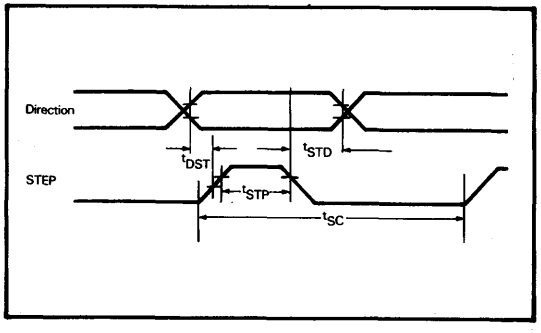
Terminal Count, Reset, Index



FDD Write/Read Operation



Seek Operation



Storage

Pin Description

Pin	Symbol	I/O	Description
1	V_{CC}	I	Power supply, connected to +5V power supply.
2~9	D7 ~ D0	I/O	Bi-directional – 8-bit data bus
10	$\overline{AEN}$	I	Input from DMA – Address Enable. When this line is active (low) the DMA controller has control of the address bus.
11~20	A9 ~ A0	I	Input from processor – 10-bit Address Bus.
21	RESET	I	Input from processor – places FDC in idle state. Resets output lines to FDD to "0" (low). Does not affect SRT, HUT or HLT in Specify command.
22	DRQ	O	Output to DMA – DMA Request is being made by FDC when DRQ = "1".
23	$\overline{IOW}$	I	Input from processor – Control signal for transfer of data to FDC via Data Bus, when "0".
24	$\overline{IOR}$	I	Input from processor – Control signal for transfer of data from FDC to Data Bus, when "0".
25	GND	I	Ground. Normally connected to +0V ground
26	IRQ	O	Output to processor – Interrupt request generated by FDC.
27	$\overline{DACK}$	I	Input from DMA – DMA cycle is active when "0" (low) and controller is performing DMA transfer.
28	TC	I	Input from DMA – Indicates the termination of a DMA transfer when "1" (high). It terminates data transfer during Read/Write/Scan command in DMA or interrupt mode.
29	DRIVE GROUP SELECT	I	The primary address will be applied when this signal is active high (3FX) The secondary address will be applied when this signal is low (37X)
30	$\overline{GATE\ 245}$	O	Output low to enable the extra 74LS245 Buffer on data bus.
31	$\overline{DRIVER\ TYPE}$	O	Output low to enable the extra disk drive type port. It's address is 3F1.
32	$\overline{HDC}$	I	Set this input to low, when your system has a hard disk control card. Otherwise, set this input to high.
33	CLOCK IN	I	24 MHz clock input.
34	$\overline{DISKETTE\ CHANGE}$	I	Input from FDD – This input is high when a diskette is present again and a step pulse is issued from FDC.

Pin Description (Continued)

Pin	Symbol	I/O	Description
35	SIDE 1 SELECT	O	Output to FDD – This output is active (high) for the upper head. Otherwise, the lower head is selected.
36	$\overline{\text{READ DATA}}$	I	Input from FDD – Each bit detected provides a 250 ns (4 MHz), 208 ns (4.8 MHz), 125 ns (8 MHz) active (low) pulse on this line.
37	$\overline{\text{WRITE PROTECT}}$	I	Input from FDD – This input is active low when a diskette with a write protect notch is inserted.
38	$\overline{\text{TRACK 00}}$	I	Input from FDD – This signal is low when the upper head is on Track 00 (the outermost track).
39	WRITE GATE	O	Output to FDD – An active high level of this output enables the write current circuits, and the Write Data output controls the writing of information.
40	WRITE DATA	O	Output to FDD – A 125 ns (8 MHz), 208 ns (4.8 MHz), 250 ns (4 MHz) pulse on this output causes a bit to be written on the disk if Write Gate is active.
41	STEP	O	Output to FDD – An active high pulse causes the read/write heads to move in the direction determined by the "direction select" signal. Motion is started each time the signal changes from an active to inactive level (at the trailing edge of the pulse).
42	DIRECTION SELECT	O	Output to FDD – This signal determines the direction the read/write head moves when the step signal is pulsed. A low level indicates away from the center of the diskette (out); a high level indicates toward the center of the diskette (in).
43	MOTOR B ON	O	Output to FDD – The spindle motor B runs when this input is active. The drive requires a 1 sec (high density)/750 ms (double density) delay after "motor on" becomes active before and after the trailing edge of the step pulse.
44	DRIVE A SELECT	O	Output to FDD – When "Drive A Select" is at the active level, drive A is enabled. When it is at the inactive level, all drive A outputs are disabled.
45	DRIVE B SELECT	O	Output to FDD – When "Drive B Select" is at the active level, drive B is enabled. When it is at the inactive level, all drive B outputs are disabled.
46	MOTOR A ON	O	Output to FDD – The spindle motor A runs when this input is active. Drive A requires a 1 sec (high density)/750 ms (double density) delay after "motor on" becomes active before and after the trailing edge of the read or write operation.
47	$\overline{\text{INDEX}}$	I	Input from FDD – A low pulse appears on this line to indicate the beginning of a disk track when the drive senses the index hole in the diskette.
48	REDUCED WRITE	O	Output to FDD – The inactive state low of this signal indicates that high-density media is present, requiring normal write currents, and the active state high indicates low-density media is present, requiring a reduced write current.

Register Description

1. Digital Output Register (IO write 3F2, 372)

The digital output register (DOR) is an output-only register controlling drive motors, drive selection, and feature enable. All bits are cleared by the I/O interface reset line. The bit definitions are as follows.

Bit 7	Reserved
Bit 6	Reserved
Bit 5	Drive B Motor Enable
Bit 4	Drive A Motor Enable
Bit 3	Enable Diskette Interrupts and DMA
Bit 2	Diskette Function Reset – Diskette function reset when this bit is low ('0').
Bit 1	Reserved
Bit 0	Drive Select – A"0"on this bit indicates that drive A is selected.

2. Digital Input Register (IO read 3F7, 377)

The digital input register is an 8-bit, read-only register used for diagnostic purposes. The following are bit definitions for this register.

Bit 7	Diskette Change
Bits 0 ~ 6	Apply to the currently selected fixed disk drive

3. Transfer Rate Register (Diskette Control Register) (IO write 3F7, 377)

The transfer rate register is a 2-bit, output-only register which controls a programmable divider and provides 8M/4.8M/4M Hz clocks for three different data transfer rates. The definition is given as follows:

Bit 0	Bit 1	Transfer Rates	Clock Rates	Reduce write
0	0	500K bps	8 MHz	0
1	0	300K bps	4.8 MHz	1
0	1	250K bps	4 MHz	1
1	1	reserved	reserved	1

4. Main Status Register (IO read 3F4, 374)

Those bits in the main status register are defined as follows:

Bit 7	Request for master (RQM) – The data register is ready to send or receive data to or from the processor.
Bit 6	Data Input/Output (DIO) – The direction of data transfer between the diskette control and the processor.
Bit 5	Non-DMA Mode (NDM) – The diskette controller is in the non-DMA mode.
Bit 4	Diskette Control Busy (CB) – A Read or Write command is being executed.
Bit 3	Reserved
Bit 2	Reserved
Bit 1	Diskette Drive B Busy (DBB) – Diskette drive B is in the seek mode.
Bit 0	Diskette Drive A Busy (DAB) – Diskette drive A is in the seek mode.

5. Diskette Data Register (IO read IO write 3F5 375)

This 8-bit data register actually consists of several registers in a stack and only one register is presented to the data bus at a time when storing data commands, and parameters, or providing diskette-drive status information.

6. Fixed Disk Status Register (IO read 1F7, 177)

The contents of this 8-bit fixed disk status register are checked when system BIOS executes self-test. This register is enabled when PC system has no Hard Disk Control card and bit 7 is of this register is fixed to 1 (high). This register shall be disabled when PC system has a Hard Disk Control card.

Table A-1 The I/O addresses of these five registers mentioned above are given in the following:

Primary	Secondary	Read	Write
3F2	372		Digital output register
3F4	374	Main status register	
3F5	375	Diskette data register	Diskette data register
3F7	377	Digital input register	Transfer rate register
1F7	177	Fixed Disk Status register*	

*: Fixed disk function

Application Notes

A: General Description

The UM8388 can be easily implemented into a FDC card or a main board and only 4 components (UM8388, 7406*2 74LS245*1) are needed in the IBM PC/AT drive system. The address decoder of UM8388 is switchable by setting pin 29 (Drive group select) of UM8388. If pin 29 is set to 1 (high), then the I/O address of the UM8388 is selected in the primary drive group address (3F1 ~ 3F7, 1F7). The contents of the UM8388 Hard Disk Status Register will be checked when system BIOS executes selftest. This register's bit 7 should be high by setting pin 32 to high when the PC system has no Hard Disk Control card, otherwise the register's bit 7 should be low by setting pin 32 to low.

B: PC/AT Application

The UM8388 registers are the same as the PC/AT floppy disk controller's. Therefore, the UM8388 can be directly implemented into the FDC card of the PC/AT to support 1.2M, 720K, 360K 1.44M Bytes FDD and only 4 components (UM8388*1, 7406*2 74LS245) are needed. The application circuit is shown as Figure A-1.

C: PC/XT Application

If the UM8388 is used to support 1.44M, 1.2M, 720K, 360K Byte FDD in the PC/XT an additional FDC program is needed to control the 1.44M, 1.2M Bytes FDD since the PC/XT BIOS doesn't support the 1.2M, 1.44M Byte FDD. During the FDD operation, this additional BIOS reads the contents of the UM8388 Drive Type Register set by pin 31, thus selects the drive to be 1.44M, 1.2M, 360K or 720K.

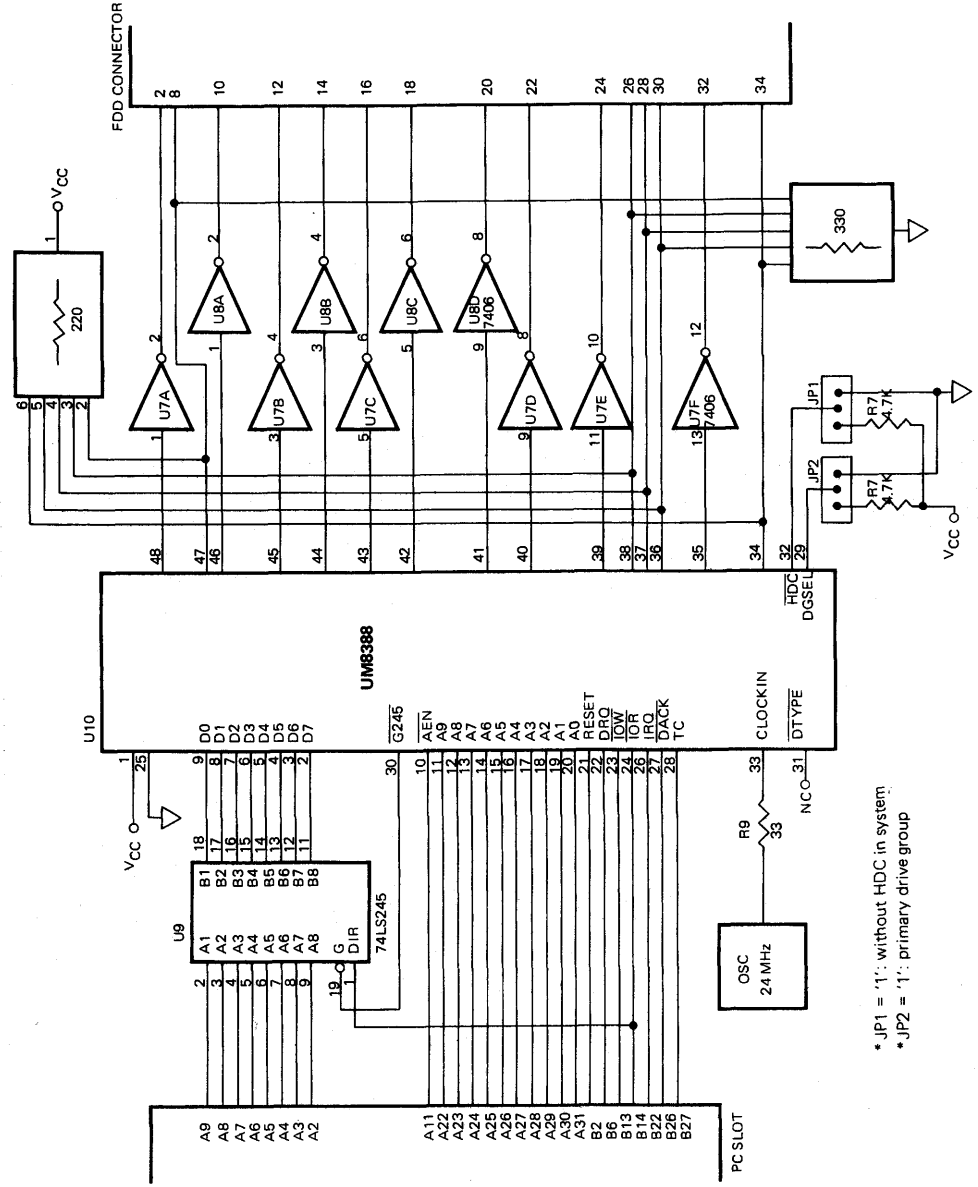


Figure A-1 PC/AT (1.44M, 1.2M, 720K, 360K FDD) Application Circuit

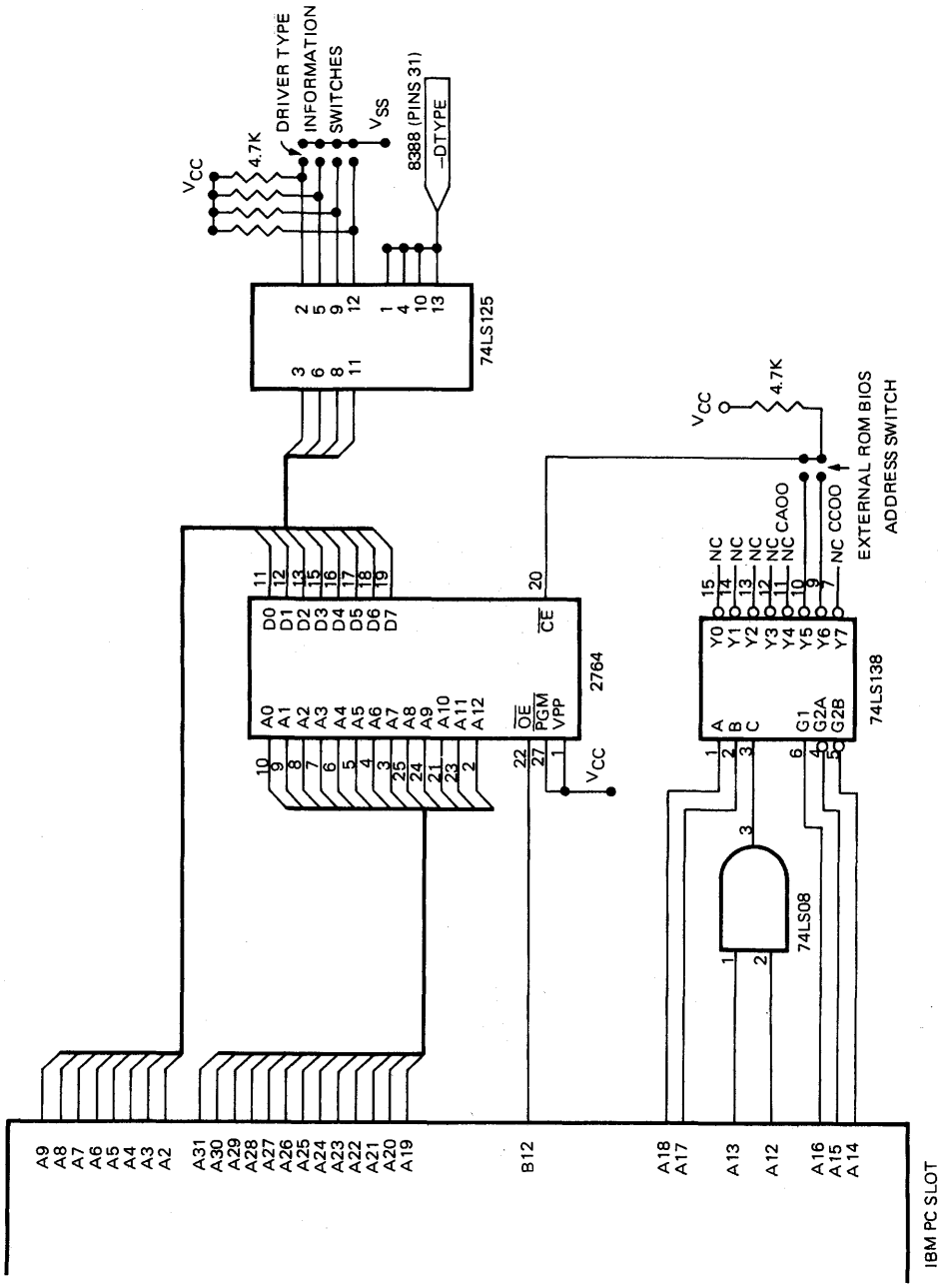


Figure A-2 PC/XT BIOS ROM Circuit

Storage

Ordering Information

Part Number	Operating Current (Max.)	Package Type
UM8388	200 mA	48L DIP
UM8388L-1	200 mA	52L PLCC
UM8388L-2	200 mA	68L PLCC

UMC

UM8397

Single-Chip Floppy Disk Controller

Features

- IBM PC XT drive system compatible
- Supports 2 drives (MS-DOS support)
- 360K/720K format selectable
- IBM PC drive system address decoder
- Only 3 components for the drive
- Internal write precompensation circuit; precompensation values: 250 ns
- Internal data separator circuit
- Supports 8", 5¼", 3½" drives

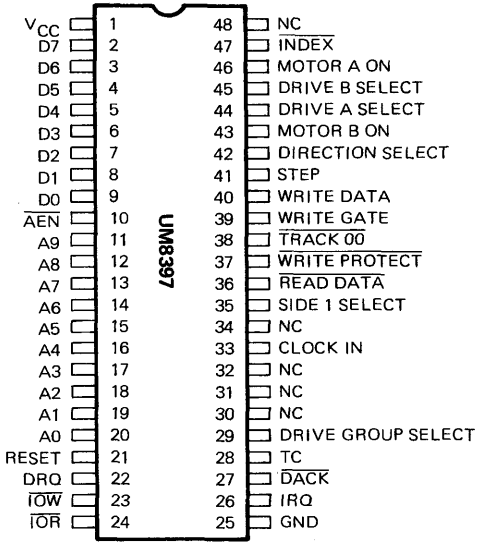
General Description

The UM8397 is a VLSI Floppy Disk Controller (FDC) chip, which contains the circuitry and control functions for interfacing a processor with up to 2 floppy disk drives. It is capable of supporting 360K Bytes (in 5¼" diskette drives) and 720K Bytes (in 3½" diskette drives) and includes FM/MFM-coded, double sided recording. The UM8397 provides the circuitry which includes the internal data separator, write precompensation address decoder, timing control and other control logic. It simplifies design of the diskette drive system and only 3 components are needed in the IBM PC XT drive system.

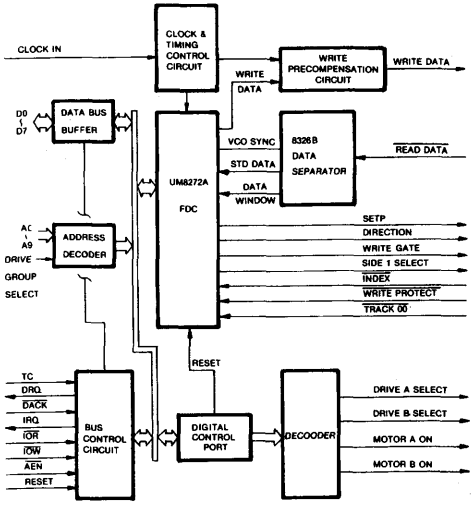
Handshaking signals are provided in the UM8397 which makes DMA operation easy to incorporate with the aid of an external DMA control chip. The FDC will operate in either the DMA or Non-DMA mode. In the Non-DMA mode, the FDC generates interrupts to the processor every time a data byte is available. In the DMA mode, the processor needs only to load the command into the FDC and all data transfers occur under control of the UM8397 and DMA controller.

The diskette drive parameters are programmable and the diskette drive's write-protect feature is supported. An interrupt level is used to indicate when an operation is complete and that a status condition requires microprocessor attention.

Pin Configurations

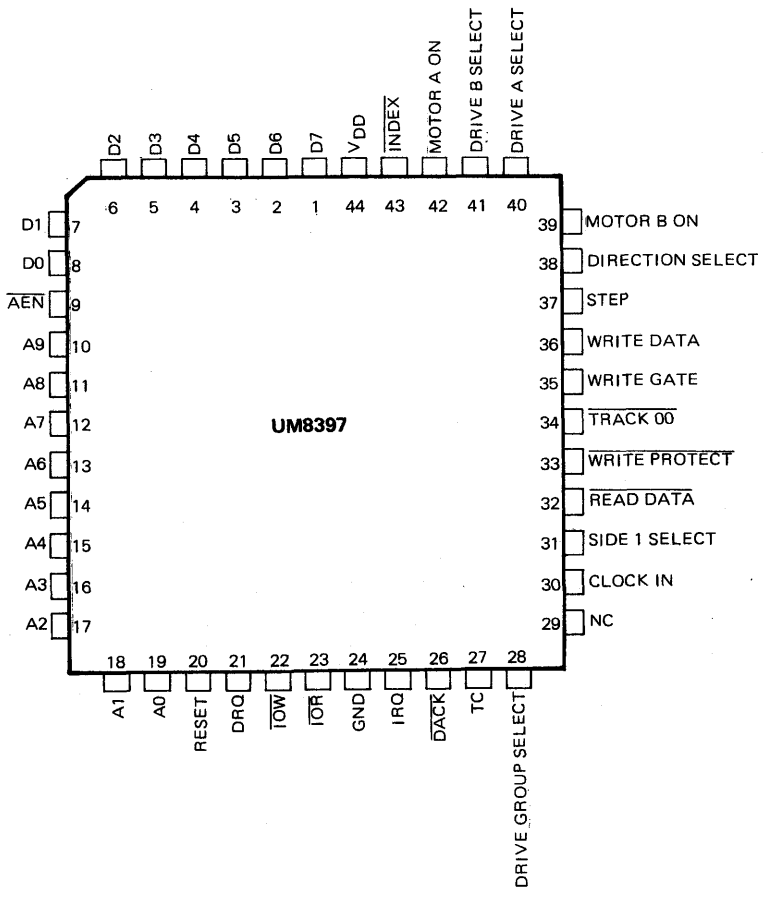


Block Diagram



Pin Configurations

44 PIN PLASTIC LEADED CHIP CARRIER



Absolute Maximum Ratings*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . −55°C to +150°C
All Output Voltages . . . . . −0.5 to +7 Volts
All Input Voltages . . . . . −0.5 to +7 Volts
Supply Voltage V_{CC} . . . . . −0.5 to +7 Volts
Power Dissipation . . . . . 1 Watt

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = 0°C to +70°C, V_{CC} = +5V ± 5%)

Symbol	Parameter	Limits		Unit	Conditions
		Min.	Max.		
V_{IL}	Input low voltage		0.8	V	
V_{IH}	Input high voltage	2.0		V	
V_{OL}	Output low voltage		0.4	V	I_{OL} = 8.0 mA
V_{OH}	Output high voltage	2.4	V_{CC}	V	I_{OH} = 4.0 mA
I_{CC}	V_{CC} supply current		200	mA	
I_{IL}	Input leakage current		10	μA	$0 \leqslant V_O \leqslant V_{CC}$
I_{LOH}	High level output leakage current		10	μA	$V_O = V_{CC}$
I_{OFL}	Output float leakage current		10	μA	$0.4V \leqslant V_O \leqslant V_{CC}$

AC Characteristics (T_A = 0°C to + 70°C, V_{CC} = +5.0V ± 10%)

PROCESSOR WRITE CYCLE

Symbol	Parameter	Min.	Max.
t_{AW}	address setup to $\overline{IOW}$ ↓	10 ns	
t_{WA}	address hold from $\overline{IOW}$ ↑	5 ns	
t_{WW}	$\overline{IOW}$ pulse width	250 ns	
t_{DW}	data setup to $\overline{IOW}$ ↑	150 ns	
t_{WD}	data hold from $\overline{IOW}$ ↑	10 ns	
t_{WI}	IRQ delay from $\overline{IOW}$ ↑		1μs*

PROCESSOR READ CYCLE

Symbol	Parameter	Min.	Max.
t_{AR}	address setup to $\overline{IOR}$ ↓	10 ns	
t_{RA}	address hold from $\overline{IOR}$ ↑	5 ns	
t_{RR}	$\overline{IOR}$ pulse width	250 ns	
t_{RD}	data delay from $\overline{IOR}$ ↓		230 ns
t_{DF}	output floating delay from $\overline{IOR}$ ↑	10 ns	30 ns
t_{RI}	IRQ6 delay from $\overline{IOR}$ ↑		1μs*

Note: *: The values are for 4 MHz clock rate.

Storage

DMA OPERATION*

Symbol	Parameter	Min.	Max.
t_{ROCY}	DRQ cycle period	13 μs	
t_{AKRO}	$\overline{DACK}$ ↓ to DRQ ↓		200 ns
t_{ROR}	DRQ ↑ to $\overline{IOR}$ ↓	800 ns	
t_{ROW}	DRQ ↑ to $\overline{IOW}$ ↓	250 ns	
t_{RORW}	DRQ ↑ to $\overline{IOR}$ ↑ or $\overline{IOW}$ ↑		12 μs

Symbol	Parameter	Min.	Typ.	Max.
t_{IDX}	index pulse width		$10t_{CY}$**	
t_{TC}	terminal count width	$1t_{CY}$		
t_{RST}	reset width	$14t_{CY}$		

FDD INTERFACE

Symbol	Parameter	Min.	Typ.	Max.
t_{WDD}	write data width		250 ns*	
t_{WCY}	write data cycle time		2 μs*	
t_{RDD}	read data active time (low)	40 ns	250 ns*	
t_{RCY}	read data cycle time		2 μs*	

SEEK OPERATION

Symbol	Parameter	Min.	Typ.	Max.
t_{STP}	step active time		10μs*	
t_{SC}	step cycle time	66μs*		
t_{DST}	DIR setup to step ↑	2μs*		
t_{STD}	DIR hold from step ↓	48μs*		

Notes:

* : The values listed for DMA operation are for 4 MHz clock rate.

** : t_{CY} is the clock rate of Drive System.

Pin Description

Pin	Symbol	I/O	Description
1	V_{CC}	I	Power supply, connected to +5V power supply.
2~9	D0 ~ D7	I/O	Bi-directional – 8-bit data bus
10	$\overline{AEN}$	I	Input from DMA – Address Enable. When this line is active (low), the DMA controller has control of the address bus.
11~20	A0 ~ A9	I	Input from processor – 10-bit Address Bus.
21	RESET	I	Input from processor – places FDC in idle state. Reset output lines to FDD to "0" (low). Does not affect SRT, HUT or HLT in Specify command.
22	DRQ	O	Output to DMA – DMA Request is being made by FDC when DRQ = "1".
23	$\overline{IOW}$	I	Input from processor – Control signal for transfer of data to FDC via Data Bus, when "0".
24	$\overline{IOR}$	I	Input from processor – Control signal for transfer of data from FDC to Data Bus, when "0".
25	GND	I	Ground.
26	IRQ	O	Output to processor – Interrupt request generated by FDC.
27	$\overline{DACK}$	I	Input from DMA – DMA cycle is active when "0" (low) and controller is performing DMA transfer.
28	TC	I	Input from DMA – Indicates the termination of a DMA transfer when "1" (high). It terminates data transfer during Read/Write/Scan command in DMA or interrupt mode.
29	DRIVE GROUP SELECT	I	The primary address will be applied when this signal is active high (3FX). The secondary address will be applied when this signal is low (37X).
30~32 34, 48	NC		Not connected.
33	CLOCK IN	I	4 MHz clock input.
35	SIDE 1 SELECT	O	Output to FDD – This output is active (high) to the upper head. Otherwise, the lower head is selected.
36	$\overline{READ\ DATA}$	I	Input from FDD – Each bit detected provides a 250 ns (4 MHz) active (low) pulse on this line.
37	$\overline{WRITE\ PROTECT}$	I	Input from FDD – This input is active low when a diskette with a write protect notch is inserted.
38	$\overline{TRACK\ 00}$	I	Input from FDD – This signal is low when the upper head is on Track 00 (the outermost track).
39	WRITE GATE	O	Output to FDD – An active level of this input enables the write current circuits, and the Write Data input controls the writing of information.

Pin Description (Continued)

Pin	Symbol	I/O	Description
40	WRITE DATA	O	Output to FDD – A 250 ns (4 MHz) pulse on this output causes a bit to be written on the disk if Write Gate is active.
41	STEP	O	Output to FDD – An active pulse causes the read/write heads to move in the direction determined by the "direction select" signal. Motion is started each time the signal changes from an active to inactive level (at the trailing edge of the pulse).
42	DIRECTION SELECT	O	Output to FDD – This signal determines the direction the read/write head moves when the step signal is pulsed. A low level indicates away from the center of the diskette (out); a high level indicates toward the center of the diskette (in).
43	MOTOR B ON	O	Output to FDD – The spindle motor B runs when this input is active. The drive requires a 1 sec (high density)/750 ms (double density) delay after "motor on" becomes active before and after the trailing edge of the step pulse.
44	DRIVE A SELECT	O	Output to FDD – When "Drive A Select" is at the active level, drive A is enabled. When it is at the inactive level, all drive A outputs are disabled.
45	DRIVE B SELECT	O	Output to FDD – When "Drive B Select" is at the active level, drive B is enabled. When it is at the inactive level, all drive B outputs are disabled.
46	MOTOR A ON	O	Output to FDD – The spindle motor A runs when this input is active. Drive A requires a 1 sec (high density)/750 ms (double density) delay after "motor on" becomes active before and after the trailing edge of the read or write operation.
47	$\overline{\text{INDEX}}$	I	Input from FDD – A pulse appears on this line to indicate the beginning of a disk track when the drive senses the index hole in the diskette.

Register Description

1. Digital Output Register (IO Write 3F2, 372)

The digital output register (DOR) is an output-only register used to control drive motors, drive selection, and feature enable. All bits are cleared by the I/O interface reset line. The bit definitions are as follows.

Bit 7	Reserved
Bit 6	Reserved
Bit 5	Drive B Motor Enable
Bit 4	Drive A Motor Enable
Bit 3	Enable Diskette Interrupts and DMA
Bit 2	Diskette Function Reset – Diskette function reset when this bit is low ('0').
Bit 1	Reserved
Bit 0	Drive Select – A."0" on this bit indicates that drive A is selected.

2. Digital Input Register (IO Read 3F7, 377)

The digital input register is an 8-bit, read-only register used for diagnostic purposes. The following are bit definitions for this register.

Bit 7	Diskette Change
Bit 0~6	Apply to the currently selected fixed disk drive

3. Main Status Register (IO Read 3F4, 374)

The bits in the main status register are defined as follows:

Bit 7	Request for master (RQM) – The data register is ready to send or receive data to or from the processor.
Bit 6	Data Input/Output (DIO) – The direction of data transfer between the diskette control and the processor.
Bit 5	Non-DMA Mode (NDM) – The diskette controller is in the non-DMA mode.
Bit 4	Diskette Control Busy (CB) – A Read or Write command is being executed.
Bit 3	Reserved
Bit 2	Reserved
Bit 1	Diskette Drive B Busy (DBB) – Diskette drive B is in the seek mode.
Bit 0	Diskette Drive A Busy (DAB) – Diskette drive A is in the seek mode.

4. Data Register (IO read/write 3F5, 375)

The 8-bit data register which actually consists of several registers in a stack with only one register presented to the data bus at a time stores data, commands, and parameters, and provides diskette-drive status information.

Table A-1 The I/O addresses of the UM8397 registers

Primary	Secondary	Read	Write
3F2	372		Digital output register
3F4	374	Main status register	
3F5	375	Diskette data register	Diskette data register
3F7	377	Digital input register	
1F7	177	Fixed Disk Status register*	

*: Fixed disk function

Command Descriptions

There are 15 separate commands which the UM8397 will execute. Each of these commands requires multiple 8-bit bytes to fully specify the operation which the processor wishes the FDC to perform. The following commands are available:

READ DATA
FORMAT A TRACK
SCAN EQUAL
SCAN LOW OR EQUAL
SCAN HIGH OR EQUAL
RECALIBRATE
READ ID
INVALID
SENSE INTERRUPT STATUS
SPECIFY
SENSE DRIVE STATUS
SEEK
READ DELETED DATA
WRITE DELETED DATA
READ A TRACK

The format of these commands is the same as UM8272A. The UM8397 also has two registers to which the main system processor has access: a status register and a data register just the same as the UM8272A. The track stepping rate, head load time, and head unload time may be programmed by the user. The UM8397 offers many additional features such as multiple sector transfers in both read and write with a single command, and full IBM PC XT compatibility in both double and high density models.

Command Symbol Description

Symbol	Name	Description
A0	Address Line 0	A0 controls selection of Main Status Register (A0 = 0) or Data Register (A0 = 1).
C	Cylinder Number	C stands for the current/selected Cylinder (track) number 0 through 76 of the medium.
D	Data	D stands for the data pattern which is going to be written into a sector.
D7-D0	Data Bus	8-bit Data Bus, where D7 stands for the most significant bit, and D0 stands for the least significant bit.
DTL	Data Length	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the Sector.
EOT	End of Track	EOT stands for the final Sector number on a Cylinder. During Read or Write operation FDC will stop data transfer after a sector # equal to EOT.
GPL	Gap Length	GPL stands for the length of Gap 3. During Read/Write commands this value determines the number of bytes that VCOs will stay low after two CRC bytes. During Format command it determines the size of Gap 3.
H	Head Address	H stands for head number 0 or 1, as specified in ID field.
HD	Head	HD stands for a selected head number 0 or 1 and controls the polarity of pin 27. (H = HD in all command words.)
HLT	Head Load Time	HLT stands for the head load time in the FDD (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time	HUT stands for the head unload time after a read or write operation has occurred (16 to 240 ms in 16 ms increments).
MF	FM or MFM Mode	If MF is low, FM mode is selected, and if it is high, MFM mode is selected.
MT	Multi-Track	If MT is high, a multi-track operation is to be performed. If MT = 1 after finishing Read/Write operation on side 0 FDC will automatically start searching for sector 1 on side 1.
N	Number	N stands for the number of data bytes written in Sector.
NCN	New Cylinder Number	NCN stands for a new Cylinder number, which is going to be reached as a result of the Seek operation. Desired position of Head.
ND	Non-DMA Mode	ND stands for operation in the Non-DMA Mode.
PCN	Present Cylinder Number	PCN stands for the Cylinder number at the completion of SENSE INTERRUPT STATUS Command. Position of Head at present time.
R	Record	R stands for the Sector number, which will be read or written.
R/W	Read/Write	R/W stands for either Read (R) or Write (W) signal.
SC	Sector	SC indicates the number of Sectors per Cylinder.
SK	Skip	SK stands for Skip Deleted Data Address Mark.
SRT	Step Rate Time	SRT stands for the Stepping Rate for the FDD. (1 to 16 ms in 1 ms increments.) Stepping Rate applies to all drives, (F = 1 ms, E = 2 ms, etc.)
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	ST 0-3 stand for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by A0 = 0); ST 0-3 may be read only after a command has been executed and contains information relevant to that particular command.
STP		During a Scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); and if STP = 2, then alternate sectors are read and compared.
US0, US1	Unit Select	US stands for a selected drive number 0 or 1.

Table 1. UM8397 Command Set

Phase	R/W	Databus D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Remarks
READ DATA			
Command	W	MT MF SK 0 0 1 1 0	Command Codes
	W	X X X X X HD US1 US0	
	W	C	Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H	
	W	R	
	W	N	
	W	EOT	
	W	GPL	
	W	DTL	
Execution			Data-transfer between the FDD and mainsystem.
Result	R	ST 0	Status information after Command execution.
	R	ST 1	
	R	ST 2	
	R	C	Sector ID information after Command execution.
	R	H	
	R	R	
	R	N	
READ DELETED DATA			
Command	W	MT MF SK 0 1 1 0 0	Command Codes
	W	X X X X X HD US1 US0	
	W	C	Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H	
	W	R	
	W	N	
	W	EOT	
	W	GPL	
	W	DTL	
Execution			Data-transfer between the FDD and mainsystem.
Result	R	ST 0	Status information after Command execution.
	R	ST 1	
	R	ST 2	
	R	C	Sector ID information after Command execution.
	R	H	
	R	R	
	R	N	
WRITE DATA			
Command	W	MT MF 0 0 0 1 0 1	Command Codes
	W	X X X X X HD US1 US0	
	W	C	Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H	
	W	R	
	W	N	
	W	EOT	
	W	GPL	
	W	DTL	
Execution			Data-transfer between the FDD and mainsystem.
Result	R	ST 0	Status information after Command execution.
	R	ST 1	
	R	ST 2	
	R	C	Sector ID information after Command execution.
	R	H	
	R	R	
	R	N	
WRITE DELETED DATA			
Command	W	MT MF 0 0 1 0 0 1	Command Codes
	W	X X X X X HD US1 US0	
	W	C	Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H	
	W	R	
	W	N	
	W	EOT	
	W	GPL	
	W	DTL	
Execution			Data-transfer between the FDD and mainsystem.
Result	R	ST 0	Status information after Command execution.
	R	ST 1	
	R	ST 2	
	R	C	Sector ID information after Command execution.
	R	H	
	R	R	
	R	N	

Phase	R/W	Databus D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Remarks
READ A TRACK			
Command	W	0 MF SK 0 0 0 1 0	Command Codes
	W	X X X X X HD US1 US0	
	W	C	Sector ID information prior to Command execution.
	W	H	
	W	R	
	W	N	
	W	EOT	
	W	GPL	
	W	DTL	
Execution			Data-transfer between the FDD and mainsystem. FDC reads all data fields from index hole to EOT.
Result	R	ST 0	Status information after Command execution
	R	ST 1	
	R	ST 2	
	R	C	Sector ID information after Command execution.
	R	H	
	R	R	
	R	N	
READ ID			
Command	W	0 MF 0 0 1 0 1 0	Command Codes
	W	X X X X X HD US1 US0	
Execution			The first correct ID information on the Cylinder is stored in Data Register.
Result	R	ST 0	Status information after Command execution.
	R	ST 1	
	R	ST 2	
	R	C	Sector ID information read during Execution Phase from Floppy Disk.
	R	H	
	R	R	
	R	N	
FORMAT A TRACK			
Command	W	0 MF 0 0 1 1 0 1	Command Codes
	W	X X X X X HD US1 US0	
	W	N	Bytes/Sector
	W	SC	Sectors/Track
	W	GPL	Gap 3
	W	D	Filer Byte
Execution			FDC formats an entire track
Result	R	ST 0	Status information after Command execution
	R	ST 1	
	R	ST 2	
	R	C	In this case, the ID information has no meaning.
	R	H	
	R	R	
	R	N	
SCAN EQUAL			
Command	W	MT MF SK 1 0 0 0 1	Command Codes
	W	X X X X X HD US1 US0	
	W	C	Sector ID information Prior to Command execution.
	W	H	
	W	R	
	W	N	
	W	EOT	
	W	GPL	
	W	STP	
Execution			Data-compared between the FDD and main-system.
Result	R	ST 0	Status information after Command execution.
	R	ST 1	
	R	ST 2	
	R	C	Sector ID information after Command execution
	R	H	
	R	R	
	R	N	

Note: 1 A_0 should equal binary 1 for all operations.
2 X = Don't care, usually made to equal binary 0.

Storage

Table 1. UM8397 Command Set (Continued)

Phase	R/W	Databus D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Remarks
SCAN LOW OR EQUAL			
Command	W	MT MF SK 1 1 0 0 1	Command Codes
	W	X X X X X HD US1 US0	
	W	C	Sector ID information prior Command execution.
	W	H	
	W	R	
	W	N	
	W	EOT	
	W	GPL	
	W	STP	
Execution			Data-compared between the FDD and main-system.
Result	R	ST 0	Status information after Command execution.
	R	ST 1	
	R	ST 2	
	R	C	Sector ID information after Command execution.
	R	H	
	R	R	
	R	N	
SCAN HIGH OR EQUAL			
Command	W	MT MF SK 1 1 0 1	Command Codes
	W	X X X X X HD US1 US0	
	W	C	Sector ID information prior Command execution.
	W	H	
	W	R	
	W	N	
	W	EOT	
	W	GPL	
	W	STP	
Execution			Data-compared between the FDD and main-system.
Result	R	ST 0	Status information after Command execution.
	R	ST 1	
	R	ST 2	
	R	C	Sector ID information after Command execution.
	R	H	
	R	R	
	R	N	

Phase	R/W	Databus D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Remarks
RECALIBRATE			
Command	W	0 0 0 0 0 1 1 1	Command Codes
Execution	W	X X X X X HD US1 US0	Head retracted to Track 0
SENSE INTERRUPT STATUS			
Command	W	0 0 0 0 1 0 0 0	Command Codes
Result	R	ST 0	Status information at the end of seek-operation about the FDC.
	R	PCN	
SPECIFY			
Command	W	0 0 0 0 0 0 1 1	Command Codes
	W	SRT HUT	
	W	HLT ND	
SENSE DRIVE STATUS			
Command	W	0 0 0 0 0 1 0 0	Command Codes
	W	X X X X X HD US1 US0	
Result	R	ST 3	Status information about FDD
SEEK			
Command	W	0 0 0 0 1 1 1 1	Command Codes
	W	X X X X X HD US1 US0	
	W	NCN	
Execution			Head is positioned over proper Cylinder on Diskette
INVALID			
Command	W	Invalid Codes	Invalid Command Codes (NoOP – FDC goes into Standby State)
Result	R	ST 0	ST 0 = 80 (16)

Read Data

A set of nine (9) byte words is required to place the FDC into the Read Data Mode. After the Read Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head setting time (defined in the Specify Command), and begins reading ID address Marks and ID fields. When the current sector number ("R") stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC outputs data (from the Data field) byte-by-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and outputted to the data bus. This continuous read function is called a "Multi-Sector Read Operation." The Read Data Command must be terminated by the receipt of a Terminal Count signal. Upon receipt of this signal, the FDC stops outputting data to the processor, while continuing to read data from the current sector checking CRC (Cyclic Redundancy Count) bytes. At the end of the sector terminate the Read Data Command.

The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track), MFM (MFM/FM), and N (Number of Bytes/Sector). Table 2 shows the Transfer Capacity. The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1. Side 0 and completing at Sector L. Side 1 (Sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, then DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a Sector, the data beyond DTL in the Sector is not sent to the Data Bus. The FDC reads (internally) the complete Sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read Operation. When N is non-zero, then DTL has no meaning and should be set to 0FFH.

At the completion of the Read Data Command, the head is not unloaded until after Head Unload Time Interval (specified in the Specify Command) has elapsed. If the processor issues another command before the head unloads then the head setting time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another. If the FDC detects the Index Hole twice without finding the right sector, (indicated in "R"), then the FDC sets the Status Register 1's ND (No Data) flag to 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the Status

Register 1's DE (Data Error) flag to 1 (high), and if a CRC error occurs in the Data Field the FDC also sets the Status Register 2's DD (Data Error in Data Field) flag to 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

If the FDC reads a Deleted Data Address Mark off the diskette, and the SK bit (bit D5 in the first Command Word) is not set (SK = 0), then the FDC sets the Status Register 2's CM (Control Mark) flag to 1 (high), and terminates the Read Data Command, after reading all the data in the Sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be served by the processor every 27 μs in the FM Mode, and every 13 μs in the MFM Mode, or the FDC sets the Status Register 1's OR (Over Run) flag to 1 (high), and terminates the Read Data Command.

If the processor terminates a read (or write) operation in the FDC, then the ID Information in the Result Phase is dependent upon the state of the MT bit and EOT byte. Table 3 shows the values for C, H, R, and N, when the processor terminates the Command.

Table 2. Transfer Capacity

Multi-Track MT	MFM/FM MF	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskette
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	or 26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	or 15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	or 8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

Table 3. ID Information When Processor Terminates Command

MT	EOT	Final Sector Transferred to Processor	ID Information at Result Phase			
			C	H	R	N
0	1A	Sector 1 to 25 at Side 0	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 0				
	08	Sector 1 to 7 at Side 0				
	1A	Sector 26 at Side 0	C + 1	NC	R = 01	NC
	0F	Sector 15 at Side 0				
	08	Sector 8 at Side 0				
	1A	Sector 1 to 25 at Side 1	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 1				
	08	Sector 1 to 7 at Side 1				
	1A	Sector 26 at Side 1	C + 1	NC	R = 01	NC
	0F	Sector 15 at Side 1				
	08	Sector 8 at Side 1				
1	1A	Sector 1 to 25 at Side 0	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 0				
	08	Sector 1 to 7 at Side 0				
	1A	Sector 26 at Side 0	NC	LSB	R = 01	NC
	0F	Sector 15 at Side 0				
	08	Sector 8 at Side 0				
	1A	Sector 1 to 25 at Side 1	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 1				
	08	Sector 1 to 7 at Side 1				
	1A	Sector 26 at Side 1	C + 1	LSB	R = 01	NC
	0F	Sector 15 at Side 1				
	08	Sector 8 at Side 1				

Note: 1. NC (No Change): The same value as the one at the beginning of command execution.
2. LSB (Least Significant Bit): The least significant bit of H is complemented.

Write Data

A set of nine (9) bytes is required to set the FDC into the Write Data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified, head setting time (defined in the Specify Command), and begins reading ID Fields. When the current sector number ("R"), stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC takes data from the processor byte-by-byte via the data bus, and outputs it to the FDD. After writing data into the current sector, the Sector Number stored in "R" is incremented by one, and the next data field is written into. The FDC continues this "Multi-Sector Write Operation" until the issuance of a Terminal Count-signal. If a Terminal Count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written then the remainder of the data field is filled with 00 (zeros).

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (Incorrect CRC) in one of the ID Fields, it sets the Status Register 1's DE (Data Error) flag to 1 (high), and terminates the Write Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

The Write Command operates in much the same manner as the Read Command. The Following items are the same; refer to the Read Data Command for details.

- Transfer Capacity
- EN (End of Cylinder) Flag
- ND (No Data) Flag
- Head Unload Time Interval
- ID Information when the processor terminates command.
- Definition of DTL when N = 0 and when N ≠ 0

In the Write Data mode, data transfers between the processor and FDC must occur every 31 μs in the FM mode, and every 15 μs in the MFM mode. If the time interval between data transfers is longer than this then the FDC sets the Status Register 1's OR (Over Run) flag to 1 (high), and terminates the Write Data Command.

For Mini-floppies, multiple track writes are usually not permitted. This is because of the turn-off time of the erase head coils – the head switches tracks before the erase head turns off. Therefore the system should typically wait 1.3 ms before attempting to step or change sides.

Write Deleted Data

This command is the same as the Write Data Command except a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark.

Read Deleted Data

This command is the same as the Read Data Command except that when the FDC detects a Data Address Mark at the beginning of a Data Field and SK = 0 (low), it will read all the data in the sector and set the Status Register 2's CM flag to 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the Data Address Mark and reads the next sector.

Read A Track

This command is similar to READ DATA Command except that the entire data field is read continuously from each of the sectors of a track. Immediately after encountering the INDEX HOLE the FDC starts reading all data fields on the track as continuous blocks of data. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR, and sets the Status Register 1's ND flag to 1 (high). If there is no comparison. (unloaded state), waits the specified, head setting time in the ID Register. (IDR) compares with the sector.

This command terminates when EOT number of sectors have been read. If the FDC does not find an ID Address Mark on the diskette after it encounters the INDEX HOLE for the second time, then it sets the Status Register 1's MA (missing address mark) flag to 1 (high), and terminates the command. (Status Register 0 has bits 7 and 6 set to 0 and 1 respectively.)

Read ID

The READ ID Command is used to give the present position of the recording head. The FDC stores the values from the first ID Field it is able to read. If no proper ID Address Mark is found on the diskette, before the INDEX HOLE is encountered for the second time then the Status Register 1's MA (Missing Address Mark) flag is set to 1 (high), and if no data is found then the Status Register 1's ND (No Data) flag is also set to 1 (high), and the command is terminated.

Format A Track

The Format Command allows an entire track to be formatted. After the INDEX HOLE is detected, Data is written on the Diskette: Gaps, Address Marks, ID Fields and Data Fields, all per the IBM System 34 (Double Density) or System 3740 (Single Density) format are recorded. The particular format which will be written is controlled by the values programmed into N (number of bytes/sector), SC (sectors/cylinder), GPL (Gap Length), and D (Data Pattern) which are supplied by the processor during the Command Phase. The Data Field is filled with the Byte of data stored in D. The ID Field for each sector is supplied by the processor, that is, four data requests per sector are made by the FDC for C (Cylinder Number), H (Head Number), R (Sector Number) and N (Number of Bytes/Sector). This allows the diskette to be formatted with nonsequential sector numbers, if desired.

After formatting each sector, the processor must send new values for C, H, R, and N to the UM8397 for each sector on the track. The content of the R Register is incremented by one after each sector is formatted, thus, the R register contains a value of R + 1 when it is read during the Result Phase. This incrementing and formatting continues for the whole track until the FDC encounters the INDEX HOLE for the second time, whereupon it terminates the command.

If a FAULT signal is received from the FDD at the end of a write operation, then the FDC sets the Status Register 0's EC flag to 1 (high), and terminates the command after setting bits 7 and 6 of Status Register 0 to 0 and 1 respectively. Also the loss of a READY signal at the beginning of a command execution phase causes command termination.

Table 4 shows the relationship between N, SC, and GPL for various sector sizes:

Table 4. Sector Size Relationships

Format	Sector Size	N	SC	GPL[1]	GPL[2,3]
8" Standard Floppy					
FM Mode	128 bytes/sector	00	1A	07	1B
	256	01	0F	0E	2A
	512	02	08	1B	3A
	1024	03	04	47	8A
	2048	04	02	C8	FF
	4096	05	01	C8	FF
MFM Mode[4]	256	01	1A	0E	36
	512	02	0F	1B	54
	1024	03	08	35	74
	2048	04	04	99	FF
	4096	05	02	C8	FF
	8192	06	01	C8	FF
5¼" Minifloppy					
FM Mode	128 bytes/sector	00	12	07	09
	128	00	10	10	19
	256	01	08	18	30
	512	02	04	46	87
	1024	03	02	C8	FF
	2048	04	01	C8	FF
MFM Mode[4]	256	01	12	0A	0C
	256	01	10	20	32
	512	02	08	2A	50
	1024	03	04	80	F0
	2048	04	02	C8	FF
	4096	05	01	C8	FF
3½" Sony Micro Floppydisk"					
FM Mode	128 bytes/sector	0	0F	07	1B
	256	1	09	0E	2A
	512	2	05	1B	3A
MFM Mode[4]	256	1	0F	0E	36
	512	2	09	1B	54
	1024	3	05	35	74

Notes:
1. Suggested values of GPL in Read or Write commands to avoid splice point between data field are ID field of contiguous sections.
2. Suggested values of GPL in format command.
3. All values except sector size are hexidecimal.
4. In MFM mode FDC cannot perform a Read/Write/format operation with 128 bytes/sector. (N = 00).

During the Command Phase of the Seek operation the FDC is in the FDC BUSY state, but during the Execution Phase it is in the NON BUSY state. While the FDC is in the NON BUSY state, another Seek Command may be issued, and in this manner parallel Seek operations may be done on up to 2 Drives at once.

If an FDD is in a NOT READY state at the beginning of the command execution phase or during the Seek operation, then the Status Register 0's NR (NOT READY) flag is set to 1 (high), and the command is terminated.

Note that the UM8397 Read and Write Commands do not have implied Seeks. Any R/W command should be preceded by: 1) Seek Command; 2) Sense Interrupt Status, and 3) Read ID.

Recalibrate

This command causes the read/write head within the FDD to retract to the Track 0 position. The FDC clears the contents of the PCN counter, and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is low, the Direction signal remains 1 (high) and Step Pulses are issued. When the Track 0 signal goes high, the Status Register 0's SE (SEEK END) flag is set to 1 (high) and the command is terminated. If the Track 0 signal is still low after 77 Step Pulses have been issued, the FDC sets the SE (SEEK END) and EC (EQUIPMENT CHECK) flags of Status Register 0 to both 1s (highs), and terminates the command.

The ability to overlap RECALIBRATE Commands to multiple FDDs, and the loss of the READY signal, as described in the SEEK Command, also applies to the RECALIBRATE Command.

Sense Interrupt Status

An Interrupt signal is generated by the FDC for one of the following reasons:

1. Upon entering the Result Phase of:
   a. Read Data Command
   b. Read a Track Command
   c. Read ID Command
   d. Read Deleted Data Command
   e. Write Data Command
   f. Format a Cylinder Command
   g. Write Deleted Data Command
   h. Scan Commands
2. Ready Line of FDD changes state
3. End of Seek or Recalibrate Command
4. During Execution Phase in the NON-DMA Mode

Interrupts caused by reasons 1 and 4 above occur during

normal command operations and are easily discernible by the processor. However, interrupts caused by reasons 2 and 3 may be uniquely identified with the aid of the Sense Interrupt Status Command. This command when issued resets the interrupt signal and via bits 5, 6, and 7 of Status Register 0 identifies the cause of the interrupt.

Neither the Seek nor Recalibrate Command have a Result Phase. Therefore, it is mandatory to use the Sense interrupt Status Command after these commands to effectively terminate them and to provide verification of the head position (PCN).

Table 5. Seek, Interrupt Codes

Seek End Bit 5	Interrupt Code		Cause
	Bit 6	Bit 7	
0	1	1	Ready Line changed state, either polarity
1	0	0	Normal Termination of Seek or Recalibrate Command
1	1	0	Abnormal Termination of Seek or Recalibrate Command

Specify

The Specify Command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution Phase of one of the Read/Write Commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (01 = 16 ms, 02 = 32 ms . . . 0F = 240 ms). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and when the Read/Write operation starts. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms . . . FE = 254 ms).

The step rate should be programmed 1 ms longer than the minimum time required by the drive.

The time intervals mentioned above are a direct function of the clock. Times indicated above are for an 8 MHz clock, if the clock was reduced to 4 MHz then all time intervals are increased by a factor of 2.

The choice of DMA or NON-DMA operation is made by the ND (NON-DMA) bit. When this bit is high (ND = 1) the NON-DMA mode is selected, and when ND = 0 the DMA mode is selected.

Sense Drive Status

This command may be used by the processor whenever it wishes to obtain the status of the FDDs. Status Register 3 contains the Drive Status information.

Invalid

If an invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command. No interrupt is generated by the UM8397 during this condition. Bit 6 and bit 7 (DIO and RQM) in the Main Status Register are both high ("1") indicating to the processor that the UM8397 is in the Result Phase and the contents of Status Register 0 (ST0) must be read. When the processor reads Status Register 0 it will find an 80H Indicating an invalid command was received.

A Sense interrupt Status Command must be sent after a Seek or Recalibrate interrupt, otherwise the FDC will consider the next command to be an invalid Command.

In some applications the user may wish to use this command as a No-Op command, to place the FDC in a standby or no operation state.

Table 6. Status Registers

Bit No.	Bit Name	Bit Symbol	Description
STATUS REGISTER 0			
D_7	Interrupt Code	IC	D_7 = 0 and D_6 = 0 Normal Termination of Command, (NT). Command was completed and properly executed.
D_6			D_7 = 0 and D_6 = 1 Abnormal Termination of Command, (AT). Execution of Command was started, but was not successfully completed.
D_6			D_7 = 1 and D_6 = 0 Invalid Command issue, (IC). Command which was issued was never started.
			D_7 = 1 and D_6 = 1 Abnormal Termination because during command execution the ready signal from FDD changed state.

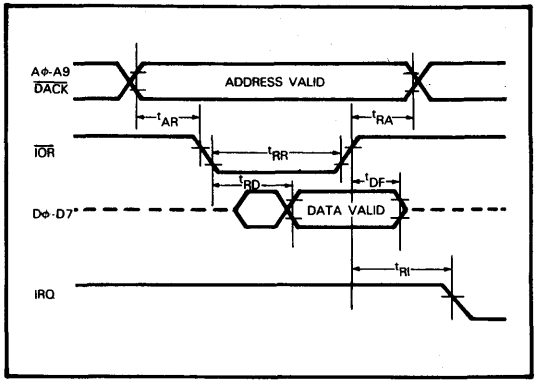
Table 6. Status Registers (Continued)

Bit No.	Bit Name	Bit Symbol	Description
STATUS REGISTER 0 (CONT.)			
D_5	Seek End	SE	When the FDC completes the SEEK Command, this flag is set to 1 (high).
D_4	Equipment Check	EC	If a fault Signal is received from the FDD, or if the Track 0 Signal fails to occur after 77 Step Pulses (Recalibrate Command) then this flag is set.
D_3	Not Ready	NR	When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to Side 1 of a single sided drive, then this flag is set.
D_2	Head Address	HD	This flag is used to indicate the state of the head at Interrupt.
D_1	Unit Select 1	US 1	These flags are used to indicate a Drive Unit Number at Interrupt
D_0	Unit Select 0	US 0	
STATUS REGISTER 1			
D_7	End of Cylinder	EN	When the FDC tries to access a Sector beyond the final Sector of a Cylinder, this flag is set.
D_6			Not used. This bit is always 0 (low).
D_5	Data Error	DE	When the FDC detects a CRC error in either the ID field or the data field, this flag is set.
D_4	Over Run	OR	If the FDC is not serviced by the main-systems during data transfers, within a certain time interval, this flag is set.
D_3			Not used. This bit always 0 (low).
D_2	No Data	ND	During execution of READ DATA, WRITE DELETED DATA or SCAN Command, if the FDC cannot find the Sector specified in the IDR Register, this flag is set.
			During executing the READ ID Command, if the FDC cannot read the ID field without an error, then this flag is set.
			During the execution of the READ A Cylinder Command, if the starting sector cannot be found, then this flag is set.
D_1	Not Writable	NW	During execution of WRITE DATA WRITE DELETED DATA or Format A Cylinder Command, if the FDC detects a write protect signal from the FDD, then this flag is set.
D_0	Missing Address Mark	MA	If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set.

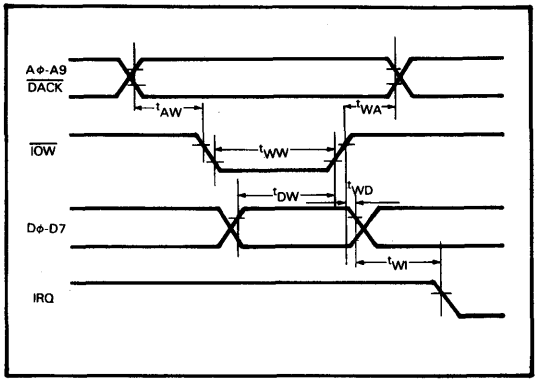
Bit No.	Bit Name	Bit Symbol	Description
STATUS REGISTER 1 (CONT.)			
D_0	Missing Address Mark	MA	If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. Also at the same time, the MD (Missing Address Mark in Data Field) of Status Register 2 is set.
STATUS REGISTER 2			
D_7			Not used. This bit is always 0 (low.)
D_6	Control Mark	CM	During executing the READ DATA or SCAN Command, if the FDC encounters a Sector which contains a Deleted Data Address Mark, this flag is set.
D_5	Data Error in Data Field	DD	If the FDC detect a CRC error in the data field then this flag is set.
D_4	Wrong Cylinder	WC	This bit is related with the ND bit. and when the content of C on the medium are different from that stored in the IDR, this flag is set.
D_3	Scan Equal Hit	SH	During executing the SCAN Command, if the condition of "equal" is satisfied, this flag is set.
D_2	Scan Not Satisfied	SN	During executing the SCAN Command, if the FDC cannot find a Sector on the cylinder which meets the condition, then this flag is set.
D_1	Bad Cylinder	BC	This bit is related with the ND bit, and when the content of C on the medium is different from that stored in the IDR and the content of C is FF, then this flag is set.
D_0	Missing Address Mark in Data Field	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.
STATUS REGISTER 3			
D_7	Fault	FT	This bit is used to indicate the status of the Fault signal from the FDD.
D_6	Write Protected	WP	This bit is used to indicate the status of the Write Protected signal from the FDD.
D_5	Ready	RDY	This bit is used to indicate the status of the Ready signal from the FDD.
D_4	Track 0	T0	This bit is used to indicate the status of the Track 0 signal from the FDD.
D_3	Two Side	TS	This bit is used to indicate the status of the Two Side signal from the FDD.
D_2	Head Address	HD	This bit is used to indicate the status of Side Select signal to the FDD.
D_1	Unit Select 1	US 1	This bit is used to indicate the status of the Unit Select 1 signal to the FDD
D_0	Unit Select 0	US 0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD

Timing Waveforms

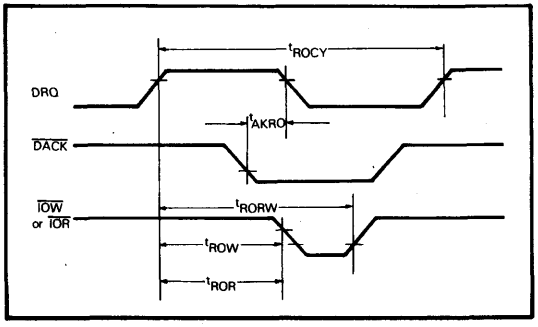
Processor Read Operation



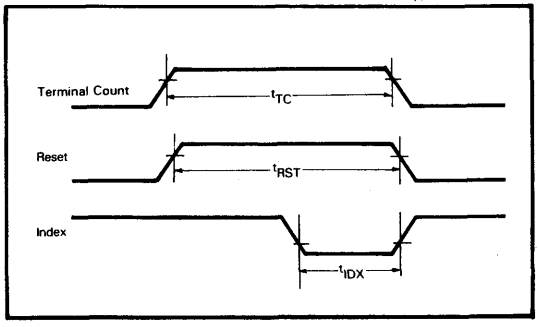
Processor Write Operation



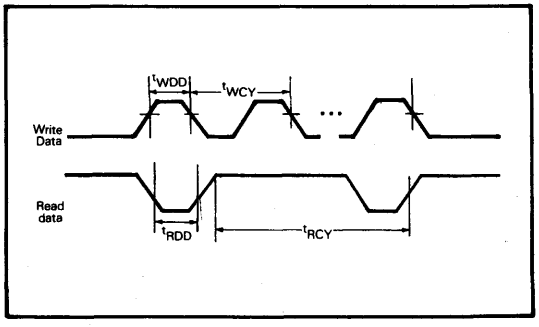
DMA Operation



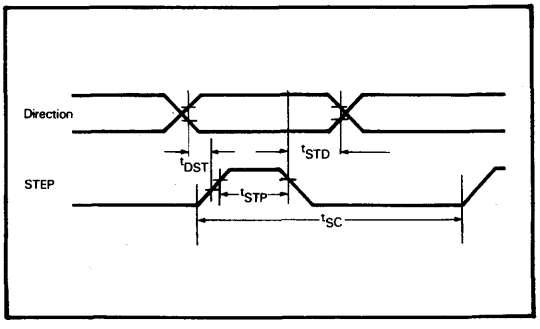
Terminal Count, Reset, Index



FDD Write/Read Operation



Seek Operation



Application Notes

A: General Description

The address decoder built-in UM8397 is switchable by setting pin 29 of UM8397. If pin 29 is set to 1 (high), then the I/O address of the UM8397 is selected in the primary drive group addresses (3F1 ~ 3F7, 1F7) as described in Table A-1.

B: PC/XT Application

The UM8397 provides circuitry which includes the UM8272A, internal data separator (UM8326B), write precompensation circuit, address decoder, clock & timing control circuit, and other control logic. Therefore, it is very easy to implement into the FDC card or main board. Only 3 components (UM8397*1, 7406*2) are needed in the IBM PC XT drive system. The application circuit is shown in Figure A-2.

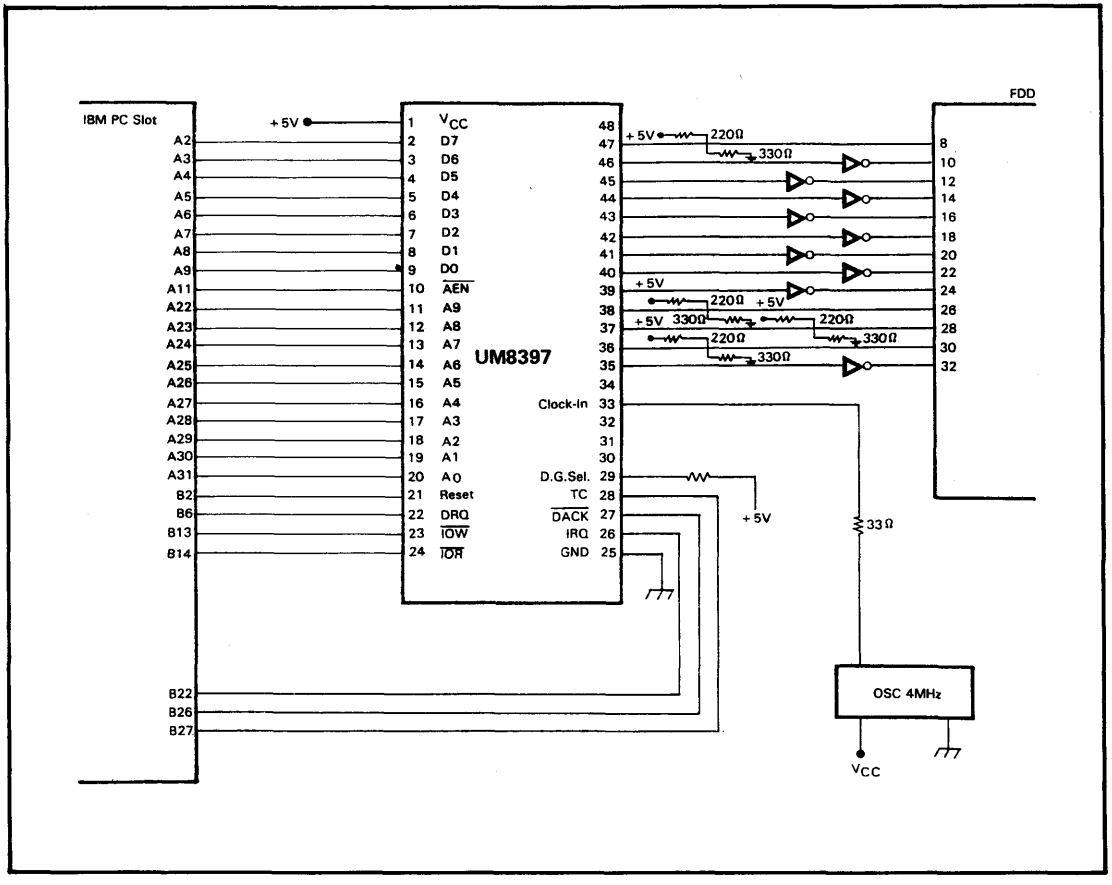


Figure A-2 PC/XT (360K, 720K FDD) Application Circuit

Ordering Information

Part Number	Operating Current (Max.)	Package Type
UM8397	200 mA	48 pin DIP
UM8397L	200 mA	44 pin PLCC

UMC

UMC

UM8398

Single-Chip Floppy Disk Controller

Features

- IBM PC XT/AT drive system compatible
- Supports 2 drives (MS-DOS support)
- 1.2M/360K/720K format selectable
- IBM PC drive system address decoder
- Only 3 components for the drive
- Internal write precompensation circuit; precompensation values: 250-125 ns
- Internal data separator circuit
- Supports to control 8", 5¼", 3½" drives

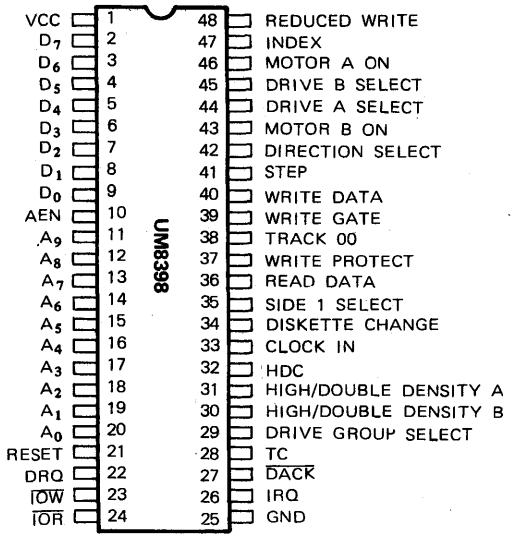
General Description

The UM8398 is a VLSI Floppy Disk Controller (FDC) chip, which contains the circuitry and control functions for interfacing a processor with up to 2 floppy disk drives. It is capable of supporting 360K Bytes, 1.2M Bytes (in 5¼" diskette drives), 720K Bytes, and 1.44M Bytes, (in 3½" diskette drives) FDDs using FM/MFM-coded, and double sided recording. UM8398 includes an internal data separator, write precompensation, circuit address decoder, timing control and other control logics. It simplifies design of a diskette drive system since only 3 components are needed in the IBM PC XT/AT drive system.

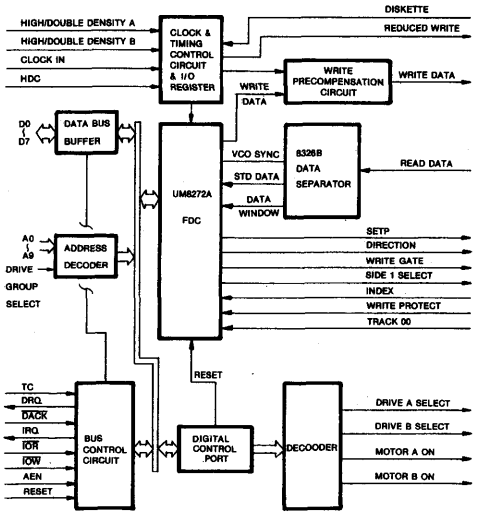
Handshaking signals are provided in UM8398 which makes DMA operation easy to incorporate with the aid of an external DMA control chip. The FDC will operate in either the DMA or Non-DMA mode. In the Non-DMA mode, the FDC generates interrupts to the processor every time a data byte is available. In the DMA mode, the processor needs only to load the command into the FDC and all data transfers occur under control of the UM8398 and DMA controller.

Many diskette drive parameters are programmable and write-protection feature is supported. One interrupt level is used to indicate when an operation is completed, or a status condition requires microprocessor's attention.

Pin Configurations

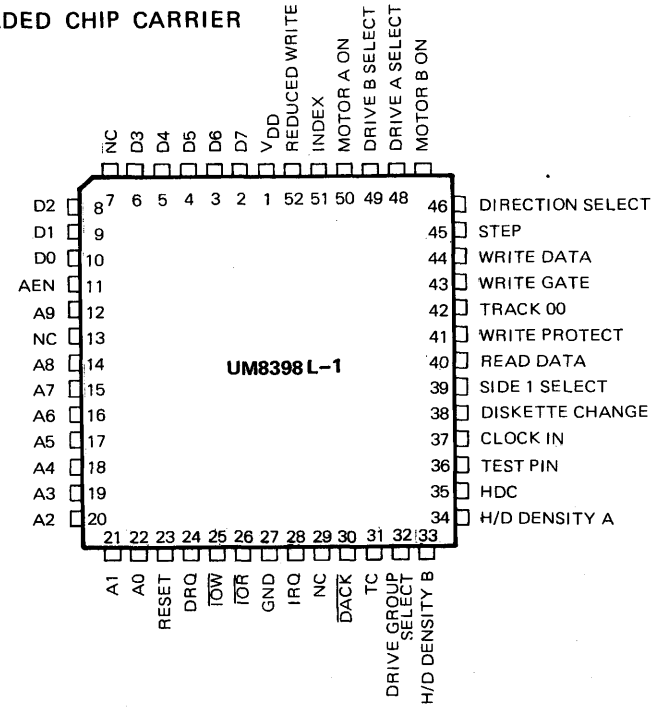


Block Diagram

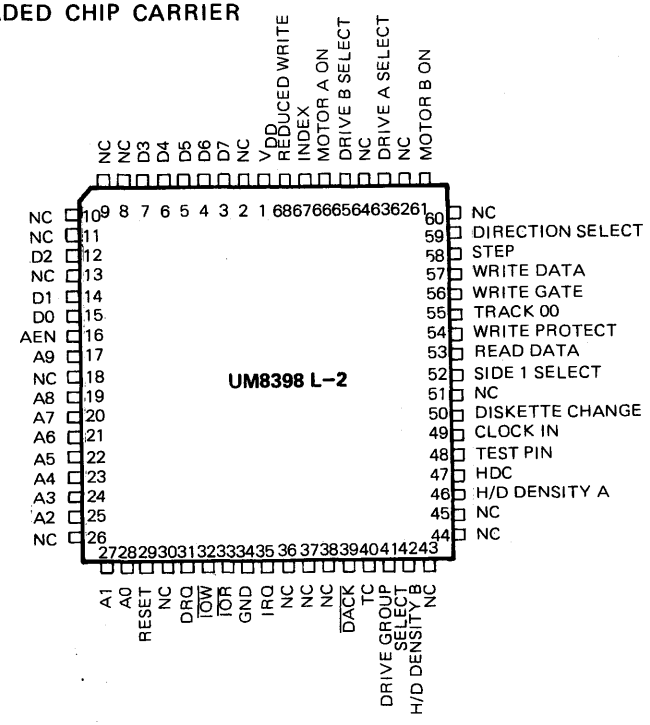


Pin Configurations (Continued)

52 PIN PLASTIC LEADED CHIP CARRIER



68 PIN PLASTIC LEADED CHIP CARRIER



Storage

Absolute Maximum Ratings*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . −55°C to +150°C
All Output Voltages . . . . . −0.5 to +7 Volts
All Input Voltages . . . . . −0.5 to +7 Volts
Supply Voltage V_{CC} . . . . . −0.5 to +7 Volts
Power Dissipation . . . . . 1 Watt

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = 0°C to +70°C, V_{CC} = +5V ± 5%)

Symbol	Parameter	Limits		Unit	Conditions
		Min.	Max.		
V_{IL}	Input low voltage		0.8	V	
V_{IH}	Input high voltage	2.0		V	
V_{OL}	Output low voltage		0.4	V	I_{OL} = 2.0mA
V_{OH}	Output high voltage	2.4	V_{CC}	V	I_{OH} = 400μA
I_{CC}	V_{CC} supply current		200	mA	
I_{IL}	Input leakage current		10	μA	$0 \leqslant V_O \leqslant V_{CC}$
I_{LOH}	High level output leakage current		10	μA	$V_O = V_{CC}$
I_{OFL}	Output float leakage current		10	μA	$0.4V \leqslant V_O \leqslant V_{CC}$

AC Characteristics (T_A = 0°C to + 70°C, V_{CC} = +5.0V ± 10%)

PROCESSOR WRITE CYCLE

Symbol	Parameter	Min.	Max.
t_{AW}	address setup to $\overline{IOW}$ ↓	0 ns	
t_{WA}	address hold from $\overline{IOW}$ ↑	0 ns	
t_{WW}	$\overline{IOW}$ pulse width	250 ns	
t_{DW}	data setup to $\overline{IOW}$ ↑	150 ns	
t_{WD}	data hold from $\overline{IOW}$ ↑	10 ns	
t_{WI}	IRQ delay from $\overline{IOW}$ ↑		500 ns*

PROCESSOR READ CYCLE

Symbol	Parameter	Min.	Max.
t_{AR}	address setup to $\overline{IOR}$ ↓	0 ns	
t_{RA}	address hold from $\overline{IOR}$ ↑	0 ns	
t_{RR}	$\overline{IOR}$ pulse width	250 ns	
t_{RD}	data delay from $\overline{IOR}$ ↓		230 ns
t_{DF}	output floating delay from $\overline{IOR}$ ↑	10 ns	30 ns
t_{RI}	IRQ6 delay from $\overline{IOR}$ ↑		500 ns*

Note: *: The values are for 8 MHz clock rate, multiply timings by 2/1.67 when using 4/4.8 MHz clock rates.

DMA OPERATION*

Symbol	Parameter	Min.	Max.
t_{ROCY}	DRQ cycle period	13 μs	
t_{AKRO}	$\overline{DACK}$ ↓ to DRQ ↓		200 ns
t_{ROR}	DRQ ↑ to $\overline{IOR}$ ↓	800 ns	
t_{ROW}	DRQ ↑ to $\overline{IOW}$ ↓	250 ns	
t_{RORW}	DRQ ↑ to $\overline{IOR}$ ↑ or $\overline{IOW}$ ↑		12 μs

Symbol	Parameter	Min.	Typ.	Max.
t_{IDX}	index pulse width		$10t_{CY}$**	
t_{TC}	terminal count width	$1t_{CY}$		
t_{RST}	reset width	$14t_{CY}$		

Notes:
* : The values listed for DMA operation are for 8 MHz clock rate, multiply timings by 2/1.67 when using 4/4.8 MHz clock rates.
**: t_{CY} is the clock rate of Drive System.

FDD INTERFACE

Symbol	Parameter	Min.	Typ.	Max.
t_{WGD}	write gate active before the first significant data bit	4 μs		8 μs
t_{WDG}	write gate inactive after the last significant data bit	4 μs		8 μs
t_{WDD}	write data width	t_{WCH}–50ns**	125/208/250 ns*	
t_{WCY}	write data cycle time		1/1.67/2 μs*	
t_{RDD}	read data active time (high)	40 ns	125/208/250 ns*	
t_{RCY}	read data cycle time		1/1.67/2 μs*	

SEEK OPERATION***

Symbol	Parameter	Min.	Typ.	Max.
t_{DU}	$US_{A,B}$ hold from DIR	45 μs		
t_{UD}	$US_{A,B}$ setup to DIR	24 μs		
t_{STP}	step active time		5 μs	
t_{SC}	step cycle time	33 μs		
t_{DST}	DIR setup to step ↑	1 μs		
t_{STD}	DIR hold from step ↓	24 μs		

Notes:
* : The specified values are for 8/4.8/4 MHz respectively.
** : t_{WCH} – write clock high time.
***: The values listed for seek operation are for 8 MHz clock period, multiply timings by 2/1.67 when using 4/4.8 MHz clock rates.

Storage

Pin Description

Pin	Symbol	I/O	Description
1	V_{CC}	I	Power supply. Connected to +5V power supply.
2~9	$D_7 \sim D_0$	I/O	Bi-directional 8-bit data bus
10	AEN	I	Input from DMA — Address Enable. When this line is active, the DMA controller has control of the address bus.
11~20	$A_9 \sim A_0$	I	Input from processor — 10-bit Address Bus.
21	RESET	I	Input from processor — places FDC in idle state. Reset output lines to FDD to "0" (low). Does not affect SRT, HUT or HLT in Specify command. If RDY pin is held high during Reset, FDC will generate interrupt 1.024 ms later. To clear this interrupt, use Sense Interrupt Status command.
22	DRQ	O	Output to DMA — DMA Request is being made by FDC when DRQ 2 = "1".
23	$\overline{IOW}$	I	Input from processor — Control signal for transfer of data to FDC via Data Bus, when "0".
24	$\overline{IOR}$	I	Input from processor — Control signal for transfer of data from FDC to Data Bus, when "0".
25	GND	I	Ground. Normally connected to +0V ground
26	IRQ	O	Output to processor — Interrupt request generated by FDC.
27	$\overline{DACK}$	I	Input from DMA — DMA cycle is active when "0" (low) and controller is performing DMA transfer.
28	TC	I	Input from DMA — Indicates the termination of a DMA transfer when "1" (high). It terminates data transfer during Read/Write/Scan command in DMA or interrupt mode.
29	DRIVE GROUP SELECT	I	The primary address will be applied when this signal is active high.
30	HIGH/DOUBLE DENSITY B	I	Drive B high or double density diskette drive selection. When drive B is high density, set this input to high.
31	HIGH/DOUBLE DENSITY A	I	Drive A high or double density diskette drive format selection. When drive A is high density, set this input to high.
32	HDC	I	Set this input to low, when your system has hard disk control card. Otherwise, set this input to high.
33	CLOCK IN	I	24 MHz clock input.
34	DISKETTE CHANGE	I	Input from FDD — This input is high when a diskette is present and a step pulse is received when the drive is selected.

Pin Description (Continued)

Pin	Symbol	I/O	Description
35	SIDE 1 SELECT	O	Output to FDD – This output is active (high) for the upper head. Otherwise, the lower head is selected.
36	READ DATA	I	Input from FDD – Each bit detected provides a 250 ns (4 MHz), 208 ns (4.8 MHz), 150 ns (8 MHz) active (low) pulse on this line.
37	WRITE PROTECT	I	Input from FDD – This input is active low when a diskette with a write protect notch is inserted.
38	TRACK 00	I	Input from FDD – This signal is low when the upper head is on Track 00 (the outermost track).
39	WRITE GATE	O	Output to FDD – An active level of this input enables the write current circuits, and the Write Data input controls the writing of information.
40	WRITE DATA	O	Output to FDD – A 150 ns (8 MHz), 208 ns (4.8 MHz), 250 ns (4 MHz) pulse on this output causes a bit to be written on the disk if Write Gate is active. When Write Gate is inactive, pulses do not appear on this output.
41	STEP	O	Output to FDD – An active pulse causes the read/write heads to move in the direction determined by the "direction select" signal. Motion is started each time the signal changes from an active to inactive level (at the trailing edge of the pulse).
42	DIRECTION SELECT	O	Output to FDD – This signal determines the direction the read/write head moves when the step signal is pulsed. An active level indicates away from the center of the diskette (out); an inactive level indicates toward the center of the diskette (in).
43	MOTOR B ON	O	Output to FDD – The spindle motor B runs when this input is active. The drive requires a 1 sec (high density)/750 ms (double density) delay after "motor on" becomes active before and after the trailing edge of the step pulse.
44	DRIVE A SELECT	O	Output to FDD – When "Drive A Select" is at the active level, drive A is enabled. When it is at the inactive level, all drive A outputs are disabled.
45	DRIVE B SELECT	O	Output to FDD – When "Drive B Select" is at the active level, drive B is enabled. When it is at the inactive level, all drive B outputs are disabled.
46	MOTOR A ON	O	Output to FDD – The spindle motor A runs when this input is active. Drive A requires a 1 sec (high density)/750 ms (double density) delay after "motor on" becomes active before and after the trailing edge of the read or write operation.
47	INDEX	I	Input from FDD – A pulse appears on this line to indicate the beginning of a disk track when the drive senses the index hole in the diskette.
48	REDUCED WRITE	O	Output to FDD – The inactive state of this signal indicates that high-density media is present, requiring normal write currents, and the active state indicates low-density media is present, requiring a reduced write current.

Register Description

1. Digital Output Register

The digital output register (DOR) is an output-only register controlling drive motors, drive selection, and feature enable. All bits are cleared by the I/O interface reset line. The bit definitions are as follows.

Bit 7	Reserved
Bit 6	Reserved
Bit 5	Drive B Motor Enable
Bit 4	Drive A Motor Enable
Bit 3	Enable Diskette Interrupts and DMA
Bit 2	Diskette Function Reset – Diskette function reset when this bit is low ('0').
Bit 1	Reserved
Bit 0	Drive Select – A "0" on this bit indicates that drive A is selected.

2. Digital Input Register

The digital input register is an 8-bit, read-only register used for diagnostic purposes. The following are bit definitions for this register.

Bit 7	Diskette Change
Bit 0~6	Apply to the currently selected fixed disk drive

3. Transfer Rate Register (Diskette Control Register)

The transfer rate register is a 2-bit, output-only register which controls a programmable divider and provides 8M/4.8M/4M Hz clocks for three different data transfer rates. The definition is given as follows:

Bit 0	Bit 1	Transfer Rates	Clock Rates
0	0	500K bps	8 MHz
1	0	300K bps	4.8 MHz
0	1	250K bps	4 MHz
1	1	reserved	reserved

4. Main Status Register

Those bits in the main status register are defined as follows:

Bit 7	Request for master (RQM) – The data register is ready to send or receive data to or from the processor.
Bit 6	Data Input/Output (DIO) – The direction of data transfer between the diskette control and the processor.
Bit 5	Non-DMA Mode (NDM) – The diskette controller is in the non-DMA mode.
Bit 4	Diskette Control Busy (CB) – A Read or Write command is being executed.
Bit 3	Reserved
Bit 2	Reserved
Bit 1	Diskette Drive B Busy (DBB) – Diskette drive B is in the seek mode.
Bit 0	Diskette Drive A Busy (DAB) – Diskette drive A is in the seek mode.

5. Diskette Data Register

This 8-bit data register actually consists of several registers in a stack and only one register is presented to the data bus at a time when storing data commands, and parameters, or providing diskette-drive status information.

6. Drive Type Register

The drive type register is a 4-bit read-only register for drive type settings. This register is used only when FDC control ROM is at ON condition. The bit definitions are given in the following:

Bit 0	Drive A Type – Drive A is double density when this bit is '0' and high density when this bit is '1'.
Bit 1	Drive B Type – Drive B is double density when this bit is '0' and high density when this bit is '1'.
Bit 2	Ground 0 (Low)
Bit 3	Ground 0 (Low)

7. Fixed Disk Status Register

The content of this 8-bit fixed disk status register is checked when system BIOS executes self-test. This register is enabled when PC system has no Hard Disk Control card and bit 7 is of this register is fixed to 1 (high). This register shall be disabled when PC system has a Hard Disk Control card.

The I/O addresses of these seven registers mentioned above are given in the following:

Primary	Secondary	Read	Write
3F1	371	Drive type register	
3F2	372		Digital output register
3F4	374	Main status register	Main status register
3F5	375	Diskette data register	Diskette data register
3F7	377	Digital input register	Transfer rate register
1F7	177	Fixed Disk Status register*	

*: Fixed disk function

Command Descriptions

There are 15 separate commands which the UM8398 will execute. Each of these commands requires multiple 8-bit bytes to fully specify the operation which the processor wishes the FDC to perform. The following commands are available:

READ DATA
FORMAT A TRACK
SCAN EQUAL
SCAN LOW OR EQUAL
SCAN HIGH OR EQUAL
RECALIBRATE
READ ID
INVALID
SENSE INTERRUPT STATUS
SPECIFY
SENSE DRIVE STATUS
SEEK
READ DELETED DATA
WRITE DELETED DATA
READ A TRACK

The format of these commands is the same as UM8272A. The UM8398 also has two registers to which the main system processor has access: a status register and a data register just the same as UM8272A. The track stepping rate, head load time, and head unload time may be programmed by the user. The UM8398 offers many additional features such as multiple sector transfers in both read and write with a single command, and full IBM PC XT/AT compatibility in both double and high density models.

Command Symbol Description

Symbol	Name	Description
A_0	Address Line 0	A_0 controls selection of Main Status Register (A_0 = 0) or Data Register (A_0 = 1).
C	Cylinder Number	C stands for the current/selected Cylinder (track) number 0 through 76 of the medium.
D	Data	D stands for the data pattern which is going to be written into a sector.
D_7-D_0	Data Bus	8-bit Data Bus, where D_7 stands for the most significant bit, and D_0 stands for the least significant bit.
DTL	Data Length	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the Sector.
EOT	End of Track	EOT stands for the final Sector number on a Cylinder. During Read or Write operation FDC will stop data transfer after a sector # equal to EOT.
GPL	Gap Length	GPL stands for the length of Gap 3. During Read/Write commands this value determines the number of bytes that VCOs will stay low after two CRC bytes. During Format command it determines the size of Gap 3.
H	Head Address	H stands for head number 0 or 1, as specified in ID field.
HD	Head	HD stands for a selected head number 0 or 1 and controls the polarity of pin 27. (H = HD in all command words.)
HLT	Head Load Time	HLT stands for the head load time in the FDD (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time	HUT stands for the head unload time after a read or write operation has occurred (16 to 240 ms in 16 ms increments).
MF	FM or MFM Mode	If MF is low, FM mode is selected, and if it is high, MFM mode is selected.
MT	Multi-Track	If MT is high, a multi-track operation is to be performed. If MT = 1 after finishing Read/Write operation on side 0 FDC will automatically start searching for sector 1 on side 1.
N	Number	N stands for the number of data bytes written in Sector.
NCN	New Cylinder Number	NCN stands for a new Cylinder number, which is going to be reached as a result of the Seek operation. Desired position of Head.
ND	Non-DMA Mode	ND stands for operation in the Non-DMA Mode.
PCN	Present Cylinder Number	PCN stands for the Cylinder number at the completion of SENSE INTERRUPT STATUS Command. Position of Head at present time.
R	Record	R stands for the Sector number, which will be read or written.
R/W	Read/Write	R/W stands for either Read (R) or Write (W) signal.
SC	Sector	SC indicates the number of Sectors per Cylinder.
SK	Skip	SK stands for Skip Deleted Data Address Mark.
SRT	Step Rate Time	SRT stands for the Stepping Rate for the FDD. (1 to 16 ms in 1 ms increments.) Stepping Rate applies to all drives, (F = 1 ms, E = 2 ms, etc.)
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	ST 0-3 stands for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by A_0 = 0); ST 0-3 may be read only after a command has been executed and contains information relevant to that particular command.
STP		During a Scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); and if STP = 2, then alternate sectors are read and compared.
US0, US1	Unit Select	US stands for a selected drive number 0 or 1.

Table 1. UM8398 Command Set

Phase	R/W	Databus D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Remarks
READ DATA			
Command	W	MT MF SK 0 0 1 1 0	Command Codes
	W	X X X X X HD US1 US0	
	W	C	Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H	
	W	R	
	W	N	
	W	EOT	
	W	GPL	
	W	DTL	
Execution			Data-transfer between the FDD and main system.
Result	R	ST 0	Status information after Command execution.
	R	ST 1	
	R	ST 2	
	R	C	Sector ID information after Command execution.
	R	H	
	R	R	
	R	N	
READ DELETED DATA			
Command	W	MT MF SK 0 1 1 0 0	Command Codes
	W	X X X X X HD US1 US0	
	W	C	Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H	
	W	R	
	W	N	
	W	EOT	
	W	GPL	
	W	DTL	
Execution			Data-transfer between the FDD and main system.
Result	R	ST 0	Status information after Command execution.
	R	ST 1	
	R	ST 2	
	R	C	Sector ID information after Command execution.
	R	H	
	R	R	
	R	N	
WRITE DATA			
Command	W	MT MF 0 0 0 1 0 1	Command Codes
	W	X X X X X HD US1 US0	
	W	C	Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H	
	W	R	
	W	N	
	W	EOT	
	W	GPL	
	W	DTL	
Execution			Data-transfer between the FDD and main system.
Result	R	ST 0	Status information after Command execution.
	R	ST 1	
	R	ST 2	
	R	C	Sector ID information after Command execution.
	R	H	
	R	R	
	R	N	
WRITE DELETED DATA			
Command	W	MT MF 0 0 1 0 0 1	Command Codes
	W	X X X X X HD US1 US0	
	W	C	Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H	
	W	R	
	W	N	
	W	EOT	
	W	GPL	
	W	DTL	
Execution			Data-transfer between the FDD and main system.
Result	R	ST 0	Status information after Command execution.
	R	ST 1	
	R	ST 2	
	R	C	Sector ID information after Command execution.
	R	H	
	R	R	
	R	N	

Phase	R/W	Databus D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Remarks
READ A TRACK			
Command	W	0 MF SK 0 0 0 1 0	Command Codes
	W	X X X X X HD US1 US0	
	W	C	Sector ID information prior to Command execution.
	W	H	
	W	R	
	W	N	
	W	EOT	
	W	GPL	
	W	DTL	
Execution			Data-transfer between the FDD and mainsystem. FDC reads all data fields from index hole to EOT.
Result	R	ST 0	Status information after Command execution
	R	ST 1	
	R	ST 2	
	R	C	Sector ID information after Command execution.
	R	H	
	R	R	
	R	N	
READ ID			
Command	W	0 MF 0 0 1 0 1 0	Command Codes
	W	X X X X X HD US1 US0	
Execution			The first correct ID information on the Cylinder is stored in Data Register.
Result	R	ST 0	Status information after Command execution.
	R	ST 1	
	R	ST 2	
	R	C	Sector ID information read during Execution Phase from Floppy Disk.
	R	H	
	R	R	
	R	N	
FORMAT A TRACK			
Command	W	0 MF 0 0 1 1 0 1	Command Codes
	W	X X X X X HD US1 US0	
	W	N	Bytes/Sector
	W	SC	Sectors/Track
	W	GPL	Gap 3
	W	D	Filer Byte
Execution			FDC formats an entire track
Result	R	ST 0	Status information after Command execution
	R	ST 1	
	R	ST 2	
	R	C	In this case, the ID information has no meaning.
	R	H	
	R	R	
	R	N	
SCAN EQUAL			
Command	W	MT MF SK 1 0 0 0 1	Command Codes
	W	X X X X X HD US1 US0	
	W	C	Sector ID information Prior to Command execution.
	W	H	
	W	R	
	W	N	
	W	EOT	
	W	GPL	
	W	STP	
Execution			Data-compared between the FDD and main-system.
Result	R	ST 0	Status information after Command execution.
	R	ST 1	
	R	ST 2	
	R	C	Sector ID information after Command execution.
	R	H	
	R	R	
	R	N	

Note: 1 A_0 should equal binary 1 for all operations.
2 X = Don't care, usually made to equal binary 0.

Storage

Table 1. UM8398 Command Set (Continued)

Phase	R/W	Databus D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Remarks
SCAN LOW OR EQUAL			
Command	W	MT MF SK 1 1 0 0 1	Command Codes
	W	X X X X X HD US1 US0	
	W	C	Sector ID information prior Command execution.
	W	H	
	W	R	
	W	N	
	W	EOT	
	W	GPL	
	W	STP	
Execution			Data-compared between the FDD and main-system.
Result	R	ST 0	Status information after Command execution.
	R	ST 1	
	R	ST 2	
	R	C	Sector ID information after Command execution.
	R	H	
	R	R	
	R	N	
SCAN HIGH OR EQUAL			
Command	W	MT MF SK 1 1 1 0 1	Command Codes
	W	X X X X X HD US1 US0	
	W	C	Sector ID information prior Command execution.
	W	H	
	W	R	
	W	N	
	W	EOT	
	W	GPL	
	W	STP	
Execution			Data-compared between the FDD and main-system.
Result	R	ST 0	Status information after Command execution.
	R	ST 1	
	R	ST 2	
	R	C	Sector ID information after Command execution.
	R	H	
	R	R	
	R	N	

Phase	R/W	Databus D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Remarks
RECALIBRATE			
Command	W	0 0 0 0 0 1 1 1	Command Codes
Execution	W	X X X X X HD US1 US0	Head retracted to Track 0
SENSE INTERRUPT STATUS			
Command	W	0 0 0 0 1 0 0 0	Command Codes
Result	R	ST 0	Status information at the end of seek-operation about the FDC.
	R	PCN	
SPECIFY			
Command	W	0 0 0 0 0 0 1 1	Command Codes
	W	SRT HUT	
	W	HLT ND	
SENSE DRIVE STATUS			
Command	W	0 0 0 0 0 1 0 0	Command Codes
	W	X X X X X HD US1 US0	
Result	R	ST 3	Status information about FDD
SEEK			
Command	W	0 0 0 0 1 1 1 1	Command Codes
	W	X X X X X HD US1 US0	
Execution	W	NCN	Head is positioned over proper Cylinder on Diskette
INVALID			
Command	W	Invalid Codes	Invalid Command Codes (NoOP – FDC goes into Standby State)
Result	R	ST 0	ST 0 = 80 (16)

Read Data

A set of nine (9) byte words is required to place the FDC into the Read Data Mode. After the Read Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head setting time (defined in the Specify Command), and begins reading ID address Marks and ID fields. When the current sector number ("R") stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC outputs data (from the Data field) byte-by-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a "Multi-Sector Read Operation." The Read Data Command must be terminated by the receipt of a Terminal Count signal. Upon receipt of this signal, the FDC stops outputting data to the processor, while continuing to read data from the current sector, checking CRC (Cyclic Redundancy Count) bytes, and then at the end of the sector. It will terminate the Read Data Command.

The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track), MFM (MFM/FM), and N (Number of Bytes/Sector). Table 2 on the next page shows the Transfer Capacity. The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing at Sector L, Side 1 (Sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, then DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a Sector, the data beyond DTL in the Sector is not sent to the Data Bus. The FDC reads (internally) the complete Sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read Operation. When N is non-zero, then DTL has no meaning and should be set to 0FFH.

At the completion of the Read Data Command, the head is not unloaded until after Head Unload Time Interval (specified in the Specify Command) has elapsed. If the processor issues another command before the head unloads then the head setting time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another. If the FDC detects the Index Hole twice without finding the right sector, (indicated in "R"), then the FDC sets the Status Register 1's ND (No Data) flag to 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the Status

Register 1's DE (Data Error) flag to 1 (high), and if a CRC error occurs in the Data Field the FDC also sets the Status Register 2's DD (Data Error in Data Field) flag to 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

If the FDC reads a Deleted Data Address Mark off the diskette, and the SK bit (bit D5 in the first Command Word) is not set (SK = 0), then the FDC sets the Status Register 2's CM (Control Mark) flag to 1 (high), and terminates the Read Data Command, after reading all the data in the Sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be served by the processor every 27 μs in the FM Mode, and every 13 μs in the MFM Mode, or the FDC sets the Status Register 1's OR (Over Run) flag to 1 (high), and terminates the Read Data Command.

If the processor terminates a read (or write) operation in the FDC, then the ID Information in the Result Phase is dependent upon the state of the MT bit and EOT byte. Table 3 shows the values for C, H, R, and N, when the processor terminates the Command.

Table 2. Transfer Capacity

Multi-Track MT	MFM/FM MF	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskette
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	or 26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	or 15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	or 8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

Table 3. ID Information When Processor Terminates Command

MT	EOT	Final Sector Transferred to Processor	ID Information at Result Phase			
			C	H	R	N
0	1A	Sector 1 to 25 at Side 0	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 0				
	08	Sector 1 to 7 at Side 0				
	1A	Sector 26 at Side 0	C + 1	NC	R = 01	NC
	0F	Sector 15 at Side 0				
	08	Sector 8 at Side 0				
	1A	Sector 1 to 25 at Side 1	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 1				
	08	Sector 1 to 7 at Side 1				
	1A	Sector 26 at Side 1	C + 1	NC	R = 01	NC
	0F	Sector 15 at Side 1				
	08	Sector 8 at Side 1				
1	1A	Sector 1 to 25 at Side 0	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 0				
	08	Sector 1 to 7 at Side 0				
	1A	Sector 26 at Side 0	NC	LSB	R = 01	NC
	0F	Sector 15 at Side 0				
	08	Sector 8 at Side 0				
	1A	Sector 1 to 25 at Side 1	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 1				
	08	Sector 1 to 7 at Side 1				
	1A	Sector 26 at Side 1	C + 1	LSB	R = 01	NC
	0F	Sector 15 at Side 1				
	08	Sector 8 at Side 1				

Note: 1. NC (No Change): The same value as the [illegible]
2. LSB (Least [illegible]

Storage

Write Data

A set of nine (9) bytes is required to set the FDC into the Write Data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified, head settling time (defined in the Specify Command), and begins reading ID Fields. When the current sector number ("R"), stored in the ID Register. (IDR) compares with the sector number read off the diskette, then the FDC takes data from the processor byte-by-byte via the data bus, and outputs it to the FDD. After writing data into the current sector, the Sector Number stored in "R" is incremented by one, and the next data field is written into. The FDC continues this "Multi-Sector Write Operation" until the issuance of a Terminal Count-signal. If a Terminal Count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written then the remainder of the data field is filled with 00 (zeros).

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (Incorrect CRC) in one of the ID Fields, it sets the Status Register 1's DE (Data Error) flag to 1 (high), and terminates the Write Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

The Write Command operates in much the same manner as the Read Command. The Following items are the same; refer to the Read Data Command for details.

- Transfer Capacity
- EN (End of Cylinder) Flag
- ND (No Data) Flag
- Head Unload Time Interval
- ID Information when the processor terminates command.
- Definition of DTL when N = 0 and when N ≠ 0

In the Write Data mode, data transfers between the processor and FDC must occur every 31 μs in the FM mode, and every 15 μs in the MFM mode. If the time interval between data transfers is longer than this then the FDC sets the Status Register 1's OR (Over Run) flag to 1 (high), and terminates the Write Data Command.

For Mini-floppies, multiple track writes are usually not permitted. This is because of the turn-off time of the erase head coils – the head switches tracks before the erase head turns off. Therefore the system should typically wait 1.3 ms before attempting to step or change sides.

Write Deleted Data

This command is the same as the Write Data Command except a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark.

Read Deleted Data

This command is the same as the Read Data Command except that when the FDC detects a Data Address Mark at the beginning of a Data Field and SK = 0 (low), it will read all the data in the sector and set the Status Register 2's CM flag to 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the Data Address Mark and reads the next sector.

Read A Track

This command is similar to READ DATA Command except that the entire data field is read continuously from each of the sectors of a track. Immediately after encountering the INDEX HOLE the FDC starts reading all data fields on the track as continuous blocks of data. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR, and sets the Status Register 1's ND flag to 1 (high) if there is no comparison. unloaded state), waits the specified, head, setting time in the ID Register. (IDR) compares with the sector.

This command terminates when EOT number of sectors have been read. If the FDC does not find an ID Address Mark on the diskette after it encounters the INDEX HOLE for the second time, then it sets the Status Register 1's MA (missing address mark) flag to 1 (high), and terminates the command. (Status Register 0 has bits 7 and 6 set to 0 and 1 respectively.)

Read ID

The READ ID Command is used to give the present position of the recording head. The FDC stores the values from the first ID Field it is able to read. If no proper ID Address Mark is found on the diskette, before the INDEX HOLE is encountered for the second time then the Status Register 1's MA (Missing Address Mark) flag is set to 1 (high), and if no data is found then the Status Register 1's ND (No Data) flag is also set to 1 (high), and the command is terminated.

Format A Track

The Format Command allows an entire track to be formatted. After the INDEX HOLE is detected, Data is written on the Diskette: Gaps, Address Marks, ID Fields and Data Fields, all as per the IBM System 34 (Double Density), or System 3740 (Single Density). The Format is recorded. The particular format which will be written is controlled by the values programmed into N (number of bytes/sector), SC (sectors/cylinder), GPL (Gap Length), and D (Data Pattern) which are supplied by the processor during the Command Phase. The Data Field is filled with the Byte of data stored in D. The ID Field for each sector is supplied by the processor, thus is, four data requests per sector are made by the FDC for C (Cylinder Number), H (Head Number), R (Sector Number) and N (Number of Bytes/Sector). This allows the diskette to be formatted with nonsequential sector numbers, if desired.

After formatting each sector, the processor must send new values for C, H, R, and N to the UM8398 for each sector on the track. The content of the R Register is incremented by one after each sector is formatted, thus, the R register contains a value of R + 1 when it is read during the Result Phase. This incrementing and formatting continues for the whole track until the FDC encounters the INDEX HOLE for the second time, whereupon it terminates the command.

If a FAULT signal is received from the FDD at the end of a write operation, then the FDC sets the Status Register 0's EC flag to 1 (high), and terminates the command after setting bits 7 and 6 of Status Register 0 to 0 and 1 respectively. Also the loss of a READY signal at the beginning of a command execution phase causes command termination.

Table 4 shows the relationship between N, SC, and GPL for various sector sizes:

Table 4. Sector Size Relationships

Format	Sector Size	N	SC	GPL[1]	GPL[2,3]
8" Standard Floppy					
FM Mode	128 bytes/sector	00	1A	07	1B
	256	01	0F	0E	2A
	512	02	08	1B	3A
	1024	03	04	47	8A
	2048	04	02	C8	FF
	4096	05	01	C8	FF
MFM Mode[4]	256	01	1A	0E	36
	512	02	0F	1B	54
	1024	03	08	35	74
	2048	04	04	99	FF
	4096	05	02	C8	FF
	8192	06	01	C8	FF
5¼" Minifloppy					
FM Mode	128 bytes/sector	00	12	07	09
	128	00	10	10	19
	256	01	08	18	30
	512	02	04	46	87
	1024	03	02	C8	FF
	2048	04	01	C8	FF
MFM Mode[4]	256	01	12	0A	0C
	256	01	10	20	32
	512	02	08	2A	50
	1024	03	04	80	F0
	2048	04	02	C8	FF
	4096	05	01	C8	FF
3½" Sony Micro Floppydisk"					
FM Mode	128 bytes/sector	0	0F	07	1B
	256	1	09	0E	2A
	512	2	05	1B	3A
MFM Mode[4]	256	1	0F	0E	36
	512	2	09	1B	54
	1024	3	05	35	74

Notes:
1. Suggested values of GPL in Read or Write commands to avoid splice point between data field and ID field of contiguous sections.
2. Suggested values of GPL in format command.
3. All values except sector size are hexidecimal.
4. In MFM mode FDC cannot perform a Read/Write/format operation with 128 bytes/sector. (N = 00).

During the Command Phase of the Seek operation the FDC is in the FDC BUSY state, but during the Execution Phase it is in the NON BUSY state. While the FDC is in the NON BUSY state, another Seek Command may be issued, and in this manner parallel Seek operations may be done on up to 2 Drives at once.

If an FDD is in a NOT READY state at the beginning of the command execution phase or during the Seek operation, then the Status Register 0's NR (NOT READY) flag is set to 1 (high), and the command is terminated.

Note that the UM8398 Read and Write Commands do not have implied Seeks. Any R/W command should be preceded by: 1) Seek Command; 2) Sense Interrupt Status, and 3) Read ID.

Recalibrate

This command causes the read/write head within the FDD to retract to the Track 0 position. The FDC clears the contents of the PCN counter, and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is low, the Direction signal remains 1 (high) and Step Pulses are issued. When the Track 0 signal goes high, the Status Register 0's SE (SEEK END) flag is set to 1 (high) and the command is terminated. If the Track 0 signal is still low after 77 Step Pulses have been issued, the FDC sets the SE (SEEK END) and EC (EQUIPMENT CHECK) flags of Status Register 0 to both 1s (highs), and terminates the command.

The ability to overlap RECALIBRATE Commands to multiple FDDs, and the loss of the READY signal, as described in the SEEK Command, also applies to the RECALIBRATE Command.

Sense Interrupt Status

An Interrupt signal is generated by the FDC for one of the following reasons:

1. Upon entering the Result Phase of:
   a. Read Data Command
   b. Read a Track Command
   c. Read ID Command
   d. Read Deleted Data Command
   e. Write Data Command
   f. Format a Cylinder Command
   g. Write Deleted Data Command
   h. Scan Commands
2. Ready Line of FDD changes state
3. End of Seek or Recalibrate Command
4. During Execution Phase in the NON-DMA Mode

Interrupts caused by reasons 1 and 4 above occur during

normal command operations and are easily discernbile by the processor. However, interrupts caused by reasons 2 and 3 may be uniquely identified with the aid of the Sense Interrupt Status Command. This command when issued, resets the interrupt signal and via bits 5, 6, and 7 of Status Register 0 identifies the cause of the interrupt.

Neither the Seek nor Recalibrate Command have a Result Phase. Therefore, it is mandatory to use the Sense interrupt Status Command after these commands to effectively terminate them and to provide verification of the head position (PCN).

Table 5. Seek, Interrupt Codes

Seek End Bit 5	Interrupt Code		Cause
	Bit 6	Bit 7	
0	1	1	Ready Line changed state, either polarity
1	0	0	Normal Termination of Seek or Recalibrate Command
1	1	0	Abnormal Termination of Seek or Recalibrate Command

Specify

The Specify Command sets the intial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution Phase of one of the Read/Write Commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (01 = 16 ms, 02 = 32 ms . . . 0F = 240 ms). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and when the Read/Write operation starts. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms . . . FE = 254 ms).

The step rate should be programmed 1 ms longer than the minimum time required by the drive.

The time intervals mentioned above are a direct function of the clock. Times indicated above are for an 8 MHz clock, if the clock was reduced to 4 MHz then all time intervals are increased by a factor of 2.

The choice of DMA or NON-DMA operation is made by the ND (NON-DMA) bit. When this bit is high (ND = 1) the NON-DMA mode is selected, and when ND = 0 the DMA mode is selected.

Sense Drive Status

This command may be used by the processor whenever it wishes to obtain the status of the FDDs. Status Register 3 contains the Drive Status information.

Invalid

If an invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command. No interrupt is generated by the UM8398 during this condition. Bit 6 and bit 7 (DIO and RQM) in the Main Status Register are both high ("1") indicating to the processor that the UM8398 is in the Result Phase and the contents of Status Register 0 (ST0) must be read. When the processor reads Status Register 0 it will find an 80H Indicating an invalid command was received.

A Sense interrupt Status Command must be sent after a Seek or Recalibrate interrupt, otherwise the FDC will consider the next command to be an invalid Command.

In some applications the user may wish to use this command as a No-Op command, to place the FDC in a standby or no operation state.

Table 6. Status Register

Bit No.	Bit Name	Bit Symbol	Description
STATUS REGISTER 0			
D_7	Interrupt Code	IC	D_7 = 0 and D_6 = 0 Normal Termination of Command, (NT). Command was completed and properly executed.
D_6			D_7 = 0 and D_6 = 1 Abnormal Termination of Command, (AT). Execution of Command was started, but was not successfully completed.
D_6			D_7 = 1 and D_6 = 0 Invalid Command issue, (IC). Command which was issued was never started.
			D_7 = 1 and D_6 = 1 Abnormal Termination because during command execution the ready signal from FDD changed state.

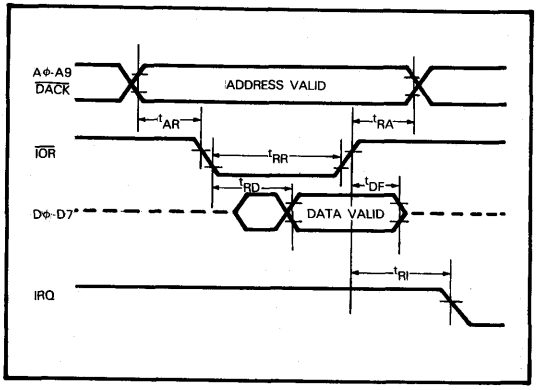
Table 6. Status Registers (Continued)

Bit No.	Name	Symbol	Description
STATUS REGISTER 0 (CONT.)			
D_6	Seek End	SE	When the FDC completes the SEEK Command, this flag is set to 1 (high).
D_4	Equipment Check	EC	If a fault Signal is received from the FDD, or if the Track 0 Signal fails to occur after 77 Step Pulses (Recalibrate Command) then this flag is set.
D_3	Not Ready	NR	When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to Side 1 of a single sided drive, then this flag is set.
D_2	Head Address	HD	This flag is used to indicate the state of the head at Interrupt.
D_1	Unit Select 1	US 1	These flags are used to indicate a Drive Unit Number at Interrupt
D_0	Unit Select 0	US 0	
STATUS REGISTER 1			
D_7	End of Cylinder	EN	When the FDC tries to access a Sector beyond the final Sector of a Cylinder, this flag is set.
D_6			Not used. This bit is always 0 (low).
D_5	Data Error	DE	When the FDC detects a CRC error in either the ID field or the data field, this flag is set.
D_4	Over Run	OR	If the FDC is not serviced by the main-systems during data transfers, within a certain time interval, this flag is set.
D_3			Not used. This bit always 0 (low).
D_2	No Data	ND	During execution of READ DATA, WRITE DELETED DATA or SCAN Command, if the FDC cannot find the Sector specified in the IDR Register, this flag is set.
			During executing the READ ID Command, if the FDC cannot read the ID field without an error, then this flag is set.
			During the execution of the READ A Cylinder Command, if the starting sector cannot be found, then this flag is set.
D_1	Not Writable	NW	During execution of WRITE DATA WRITE DELETED DATA or Format A Cylinder Command, if the FDC detects a write protect signal from the FDD, then this flag is set.
D_0	Missing Address Mark	MA	If the FDC cannot detect the ID Address Mark after encountering the Index hole twice, then this flag is set.

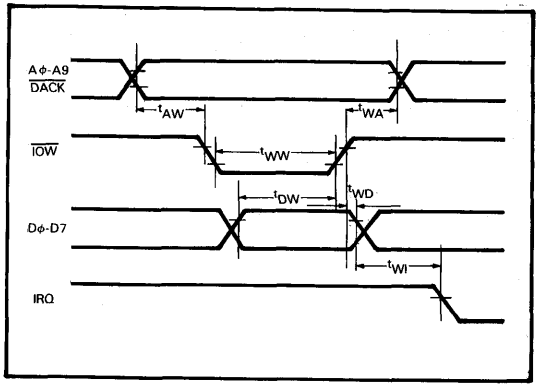
Bit No.	Name	Symbol	Description
STATUS REGISTER 1 (CONT.)			
D_0	Missing Address Mark	MA	If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. Also at the same time, the MD (Missing Address Mark in Data Field) of Status Register 2 is set.
STATUS REGISTER 2			
D_7			Not used. This bit is always 0 (low.)
D_6	Control Mark	CM	During executing the READ DATA or SCAN Command, if the FDC encounters a Sector which contains a Deleted Data Address Mark, this flag is set.
D_5	Data Error in Data Field	DD	If the FDC detect a CRC error in the data field then this flag is set.
D_4	Wrong Cylinder	WC	This bit is related with the ND bit. and when the contents of C on the medium is different from that stored in the IDR, this flag is set.
D_3	Scan Equal Hit	SH	During executing the SCAN Command, if the condition of "equal" is satisfied, this flag is set.
D_2	Scan Not Satisfied	SN	During executing the SCAN Command, if the FDC cannot find a Sector on the cylinder which meets the condition, then this flag is set.
D_1	Bad Cylinder	BC	This bit is related with the ND bit, and when the content of C on the medium is different from that stored in the IDR and the content of C is FF, then this flag is set.
D_0	Missing Address Mark in Data Field	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.
STATUS REGISTER 3			
D_7	Fault	FT	This bit is used to indicate the status of the Fault signal from the FDD.
D_6	Write Protected	WP	This bit is used to indicate the status of the Write Protected signal from the FDD.
D_5	Ready	RDY	This bit is used to indicate the status of the Ready signal from the FDD.
D_4	Track 0	T0	This bit is used to indicate the status of the Track 0 signal from the FDD.
D_3	Two Side	TS	This bit is used to indicate the status of the Two Side signal from the FDD.
D_2	Head Address	HD	This bit is used to indicate the status of Side Select signal to the FDD.
D_1	Unit Select 1	US 1	This bit is used to indicate the status of the Unit Select 1 signal to the FDD
D_0	Unit Select 0	US 0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD

Timing Waveforms

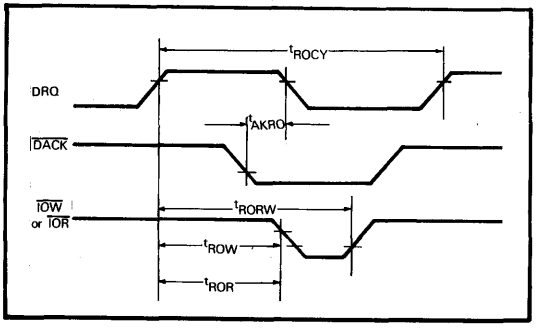
Processor Read Operation



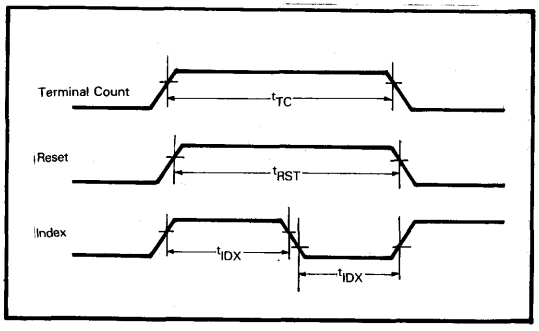
Processor Write Operation



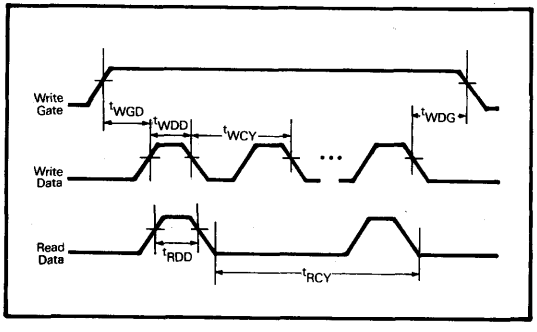
DMA Operation



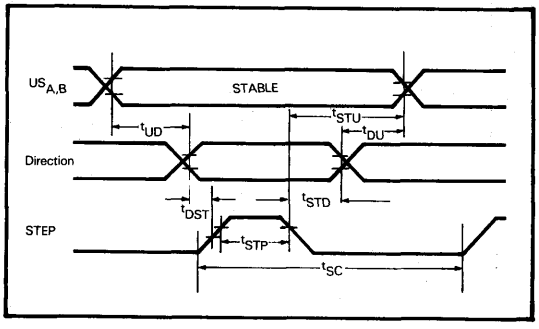
Terminal Count, Reset, Index



FDD Write/Read Operation



Seek Operation



Application Notes

A: General Description

The UM8398 is a VLSI Floppy Disk Controller (FDC) chip, which contains the circuitry and control functions for interfacing a processor up to 2 Floppy Disk Drives. It is capable of supporting 360K Bytes, 1.2M Bytes (in 5¼" diskette drives), 720K Bytes, and 1.44M Bytes (in 3½" diskette drives) FDDs using FM/MFM-coded, double sided recording. The UM8398 provides all the functions of the UM8272A, internal data separator (UM8326B), write precompensation circuit, address decoder, clock & timing control circuit, and other control logic. Therefore, it is very easy to implement into a FDC card or main board since only 3 components (UM8398*1, 7406*2) are needed in the IBM PC XT/AT drive system.

The address decoder of UM8398 is switchable by setting pin 29 of UM8398. If pin 29 is set to 1 (high), then the I/O address of the UM8398 is selected in the primary drive group address (3F1~3F7, 1F7) described in Table A-1.

Table A-1 I/O addresses of the UM8398 registers

Primary	Secondary	Read	Write
3F1	371	Drive type register	
3F2	372		Digital output register
3F4	374	Main status register	Main status register
3F5	375	Diskette data register	Diskette data register
3F7	377	Digital input register	Transter rate register
1F7	177	Status register*	

* Fixed disk function

B: PC/AT Application

The UM8398's registers described in Table A-1 are the same as the PC/AT floppy disk controller's. Therefore, the UM8398 can be directly implemented into the FDC card of the PC/AT to support 1.2M, 720K, 360K Bytes FDD with only 3 components (UM8398*1, 7406*2) needed. The application circuit is shown in Figure A-1.

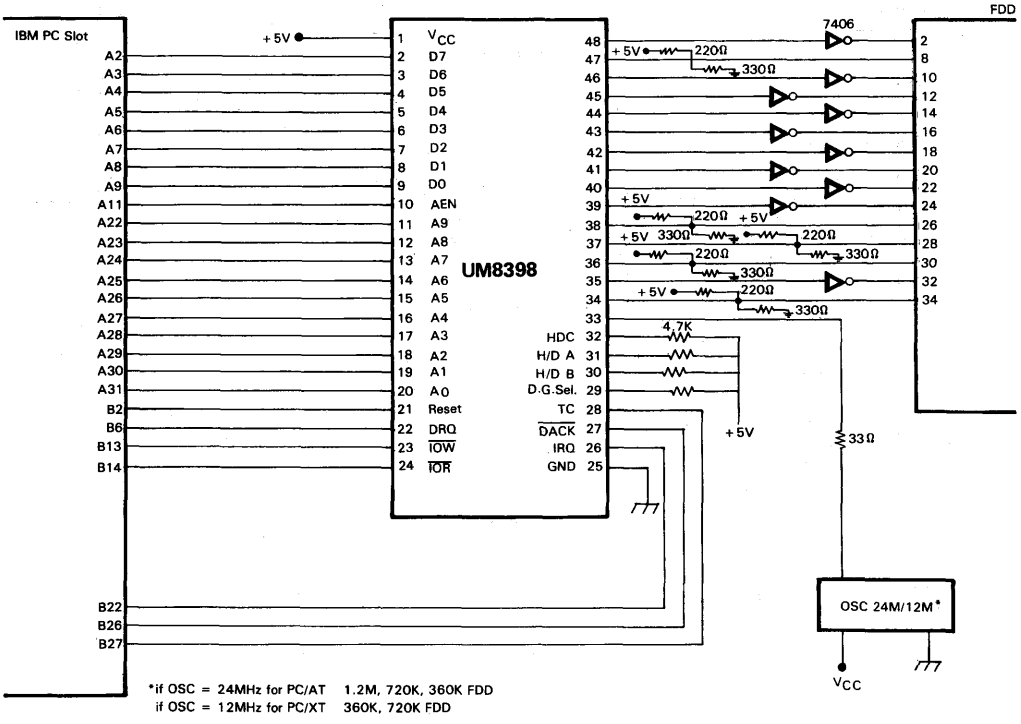


Figure A-1 PC/AT (1.2M, 720K, 360K FDD) and PC/XT (360K, 720K FDD) Application Circuit

C: PC/XT Application

If the UM8398 is implemented into the FDC card of the PC/XT to support 360K Byte and 720K Byte FDD, the application circuit is the same as the PC/AT's of the UM8398 except that the frequency of the oscillation circuit has to be 12 MHz.

If the UM8398 is used to support 1.2M, 720K, 360K Byte FDD in the PC/XT, then an additional FDC program is needed to control the 1.2M Byte FDD since the PC/XT BIOS doesn't support the 1.2M Byte FDD. During the FDD operation, this additional BIOS reads the contents of the UM8398's Drive Type Register set by pin 30 and pin 31, thus selects the drive to be 1.2M or 360K Byte FDD.

The contents of the UM8398's Hard Disk Status Register will be checked when system BIOS executes self-test. This register's bit 7 should be high by setting pin 32 to high when the PC system has no Hard Disk Control card, otherwise the register's bit 7 should be low by setting pin 32 to low.

Table A-2 Shows the definition of pins 30, 31, and 32.

Table A-2

H/D A (Pin 31)	H/D B(Pin 30)	HDC (Pin 32)
"1" High density	High density	Without HDC in system
"0" Double density	Double density	With HDC in system

PC/XT 1.2M, 720K, 360K FDD Application Circuits

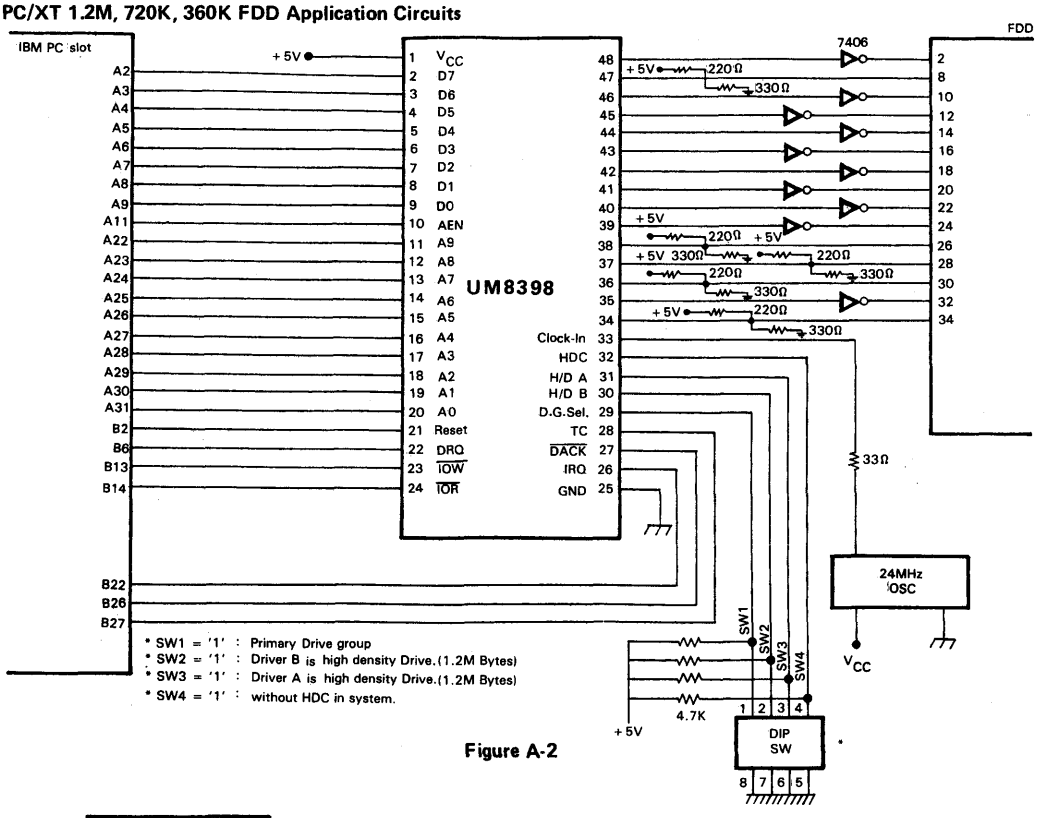


Figure A-2

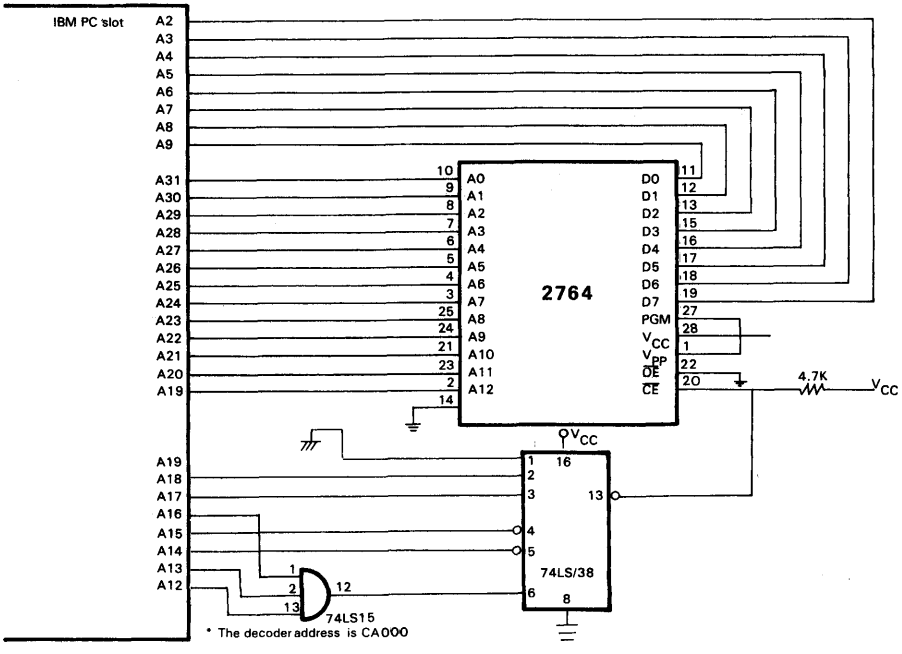


Figure A-3 PC/XT BIOS ROM circuit

Ordering Information

Part Number	Operating Current (Max.)	Package Type
UM8398	200 mA	48L DIP
UM8398L-1	200 mA	52 PLCC
UM8398L-2	200 mA	68 PLCC

I/O and Peripherals

Part No.	Description	Page
UM2661	Enhanced Programmable Communications Interface (EPCI)	5-3
UM6522/A	Versatile Interface Adapter (VIA)	5-18
UM6532/A	RAM, I/O, Timer Array	5-35
UM6551	Asynchronous Communication Interface Adapter (ACIA)	5-42
UM82C01	Capacitance Keyboard Encoder (CKE)	5-51
UM82C11-C	Printer Adapter Interface (PAI)	5-62
UM82C450	Asynchronous Communication Element (ACE)	5-71
UM82C451	Parallel/Asynchronous Communication Element	5-86
UM82C452	Single Chip Multi-I/O	5-111
UM82C550	Asynchronous Communications Element with FIFOs	5-135
UM82C8167	Real-Time Clock (RTC)	5-158
UM82C852	Multi I/O For XT	5-165
UM82450	Asynchronous Communication Element (ACE)	5-188
UM8250A	Asynchronous Communication Element (ACE)	5-204
UM8250B	Asynchronous Communication Element (ACE)	5-219

UMC

UM2661

Enhanced Programmable Communications Interface (EPCI)

Features

Synchronous Operation

- 5 to 8-bit characters plus parity
- Single or double SYN operation
- Internal or external character synchronization
- Transparent or non-transparent mode
- Transparent mode DLE stuffing (Tx) and detection (Rx)
- Automatic SYN or DLE-SYN insertion
- SYN, DLE and DLE-SYN stripping
- Odd, even, or no parity
- Local or remote maintenance loop back mode
- Baud rate: DC to 1M bps (1X clock)

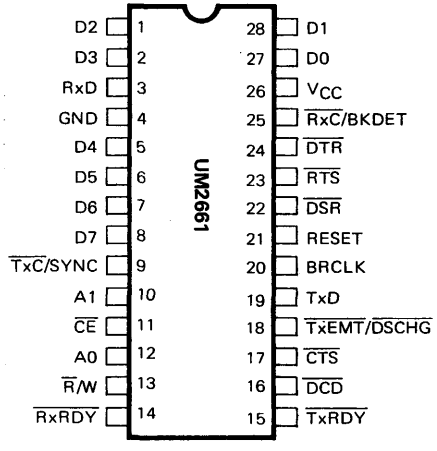
Asynchronous Operation

- 5 to 8-bit characters plus parity
- 1, 1½ or 2 stop bits transmitted
- Odd, even, or no parity
- Parity, overrun and framing error detection
- Line break detection and generation
- False start bit detection
- Automatic serial echo mode (echoplex)
- Local or remote maintenance loop back mode
- Baud rate: DC to 1M bps (1X clock)
  - DC to 62.5K bps (16X clock)
  - DC to 15.625K bps (64X clock)

Other Features

- Internal or external baud rate clock
- 3 baud rate sets UM2661–1, –2, –3
- 16 internal rates for each set
- Double buffered transmitter and receiver
- Dynamic character length switching
- Full or half duplex operation
- TTL compatible inputs and outputs
- RxC and TxC pins are short circuit protected
- 3 open drain MOS outputs can be wire-ORed
- Single 5V power supply
- No system clock required

Pin Configuration



Block Diagram

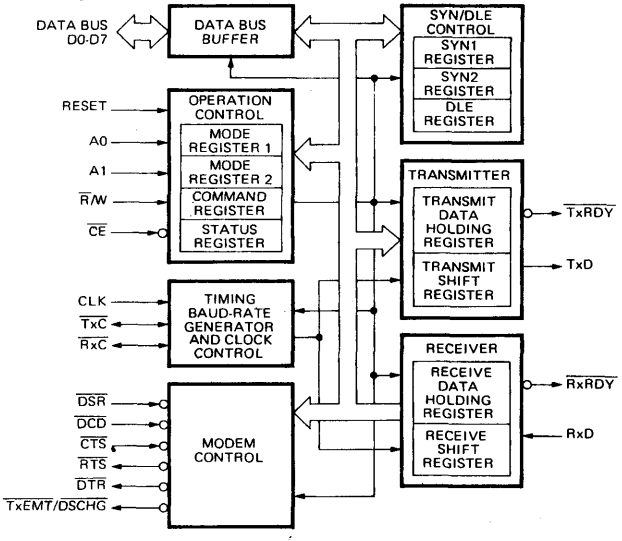


Figure 1. Internal Block Diagram

Absolute Maximum Ratings *

Supply Voltage V_{CC} . . . . . −0.3V to +7.0V
Input/Output Voltage V_{IN} . . . . . −0.3V to +7.0V
Operating Temperature T_{OP} . . . . . 0°C to 70°C
Storage Temperature T_{STG} . . . . . −55°C to 150°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

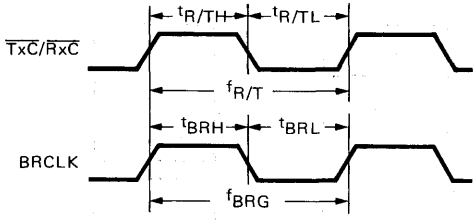
DC Characteristics

(V_{CC} = 5.0V ± 5%, T_A = 0-70°C, unless otherwise noted)

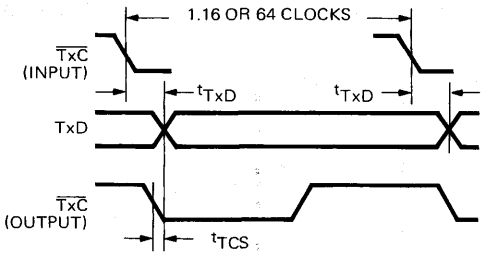
Parameter	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	2.0		V_{CC}	V
Input Low Voltage	V_{IL}			0.8	V
Input Leakage Current V_{IN} = 0 to 5.5V	I_{IN}			10	μA
Input Leakage Current for High Impedance State	I_{TSI}			10	μA
Output High Voltage: I_{LOAD} = −400μA	V_{OH}	2.4			V
Output Low Voltage: I_{LOAD} = 2.2 mA	V_{OL}			0.4	V
Input Capacitance: f_c = 1 MHz	C_{IN}			20	pF
Output Capacitance	C_{OUT}			20	pF
Power Dissipation (V_{CC} = 5.25V)	P_D			650	mW

Receiver/Transmitter Signal Timing

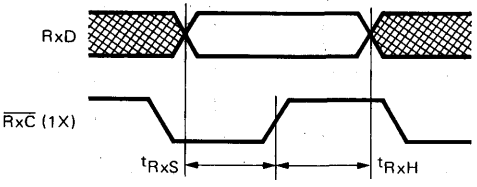
CLOCKS



TRANSMIT TIMING



RECEIVER TIMING

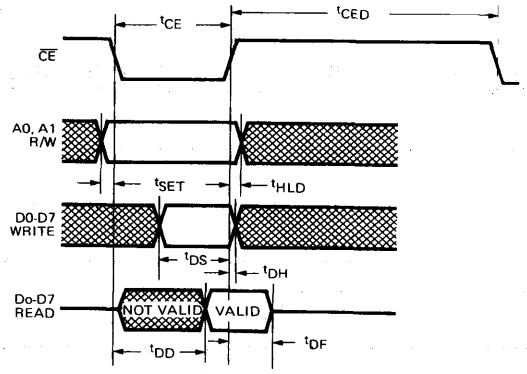


Symbol	Characteristics	Min.	Typ.	Max.	Unit
$t_{R/TH}$	TxC or RxC HIGH	500			ns
$t_{R/TL}$	TxC or RxC LOW	500		1.0	ns
$f_{R/T}$	TxC or RxC freq.	DC		1.0	MHz
t_{BRH}	BRCLK HIGH	70			ns
t_{BRL}	BRCLK LOW	70			ns
f_{BRG}	BRCLK freq. (1)		4.9152		MHz
t_{RxS}	RxD SETUP	300			ns
t_{RxH}	RxD HOLD	350			ns
t_{TxD}	TxD DELAY FROM TxC C_L = 150 pF			650	ns
t_{TCS}	SKEW TxD vs TxC C_L = 150 pF		0		ns

Note: f_{BRG} = 4.9152 applicable for -1 and -2, f_{BRG} = 5.0688 for -3.

Read/Write Timing Characteristics

(V_{CC} = 5.0V ± 5%, T_A = 0-70°C, unless otherwise noted)



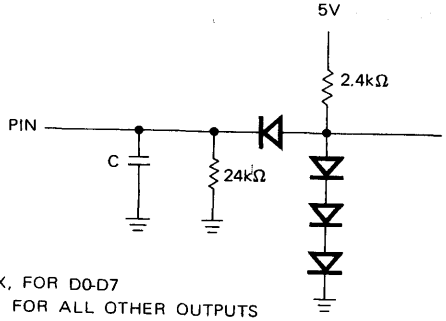
Symbol	Characteristics	Min.	Max.	Unit
t_{CE}	$\overline{CE}$ Pulse Width	250		ns
t_{CED}	$\overline{CE}$ to $\overline{CE}$ Delay	600		ns
t_{SET}	Address and R/W Set Up	10		ns
t_{HLD}	Address and $\overline{R}$/W Hold	10		ns
t_{DS}	Write Data Set Up	150		ns
t_{DH}	Write Data Hold	0		ns
t_{DD}	Read Data Delay C_L = 150 pF		200	ns
t_{DF}	READ DATA HOLD C_L = 150 pF	10	100	ns

Table 1. Effect of MR17 and MR16 on Character Fill and Character Stripping (Synchronous Mode)

MR17	MR16	Mode	Synchronizing Sequence	Character Fill	Character(s) Stripped CR7=0, CR6=1
0	0	Double SYN Normal	SYN1-SYN2	SYN1-SYN2	SYN1 SYN1-SYN2(1)
1	0	Single SYN Normal	SYN1	SYN1	SYN1(1)
0	1	Double SYN Transparent	SYN1-SYN2	DLE-SYN1	DLE-SYN1(1) SYN1-SYN2(1) (Only Initial Synchronizing Sequence) DLE (also Sets SR3 it is Parity Disabled and not Following a DLE or SYN1) In a DLE-DLE Sequence Only the First DLE is Stripped
1	1	Single SYN Transparent	SYN1	DLE-SYN1	DLE-SYN1(1) SYN1 (only Initial Synchronizing Sequence) DLE and DLE-DLE same as Double SYN Transparent

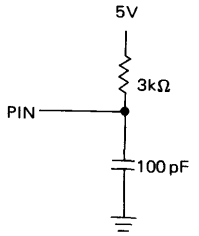
Note: Symbol indicates SYN DET status set upon detection of initial synchronizing characters and after SYNC has been achieved by detection of DLE-SYN1 pair.

Test Load



C = 130 pF MAX, FOR D0-D7
C = 30 pF MAX. FOR ALL OTHER OUTPUTS

OPEN COLLECTOR OUTPUT TEST LOAD



I/O And Peripherals

Timing Waveforms

SYNCHRONOUS MODE 7-BIT CHARACTER, NO PARITY

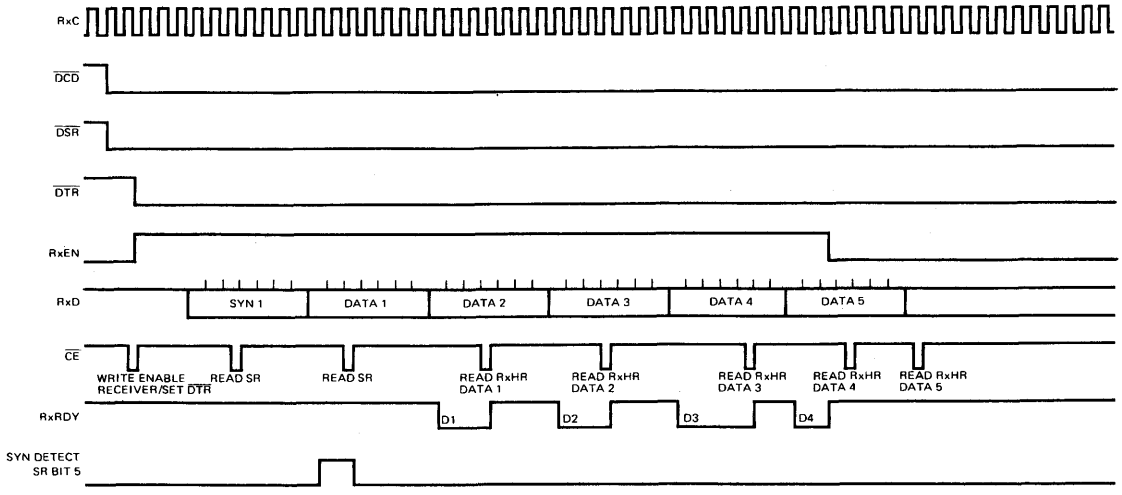


Figure 2. Receiver Operation Timing Diagram

ASYNCHRONOUS MODE 7-BIT CHARACTER, NO PARITY, 1 STOP BIT

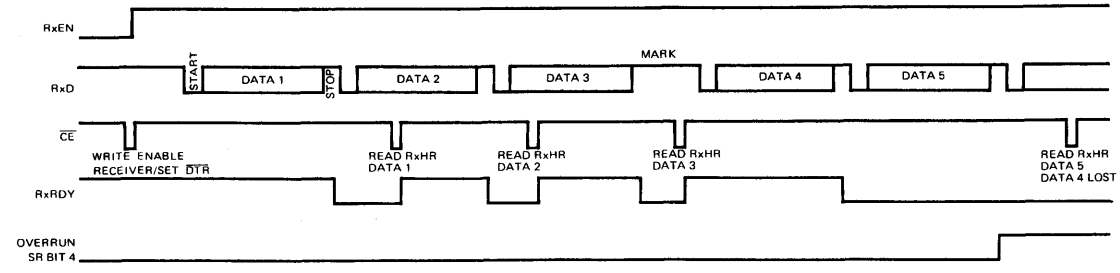


Figure 3. Receiver Operation Timing Diagram

Timing Waveforms (Continued)

SYNCHRONOUS MODE 7-BIT CHARACTER, NO PARITY

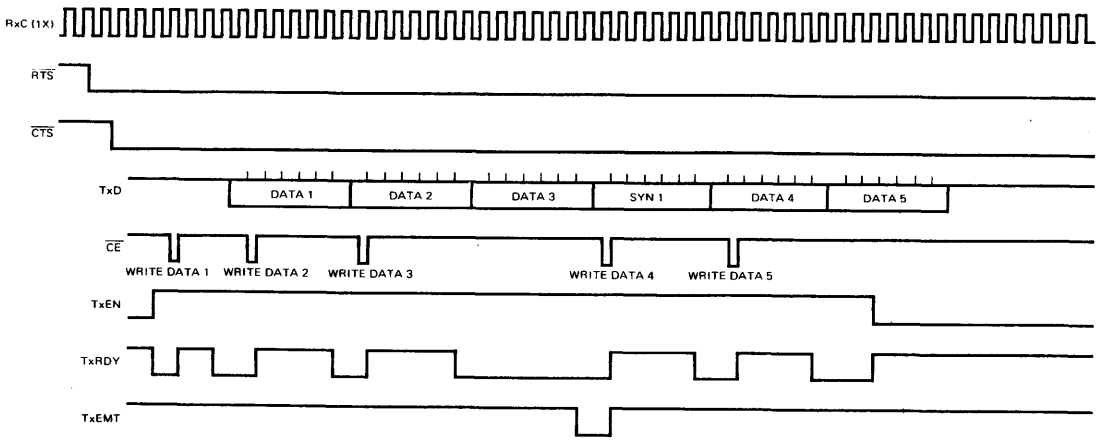


Figure 4. Transmitter Operation Timing Diagram

ASYNCHRONOUS MODE 7-BIT CHARACTER, NO PARITY, 1 STOP BIT

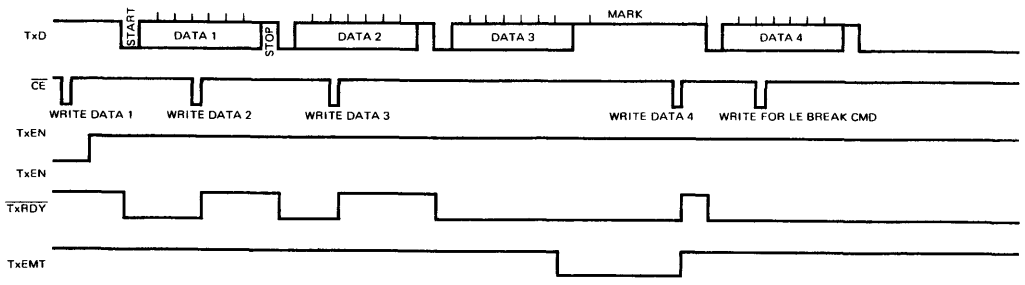


Figure 5. Transmitter Operation Timing Diagram

I/O And Peripherals

Timing Waveforms (Continued)

ASYNCHRONOUS RECEIVER OPERATION

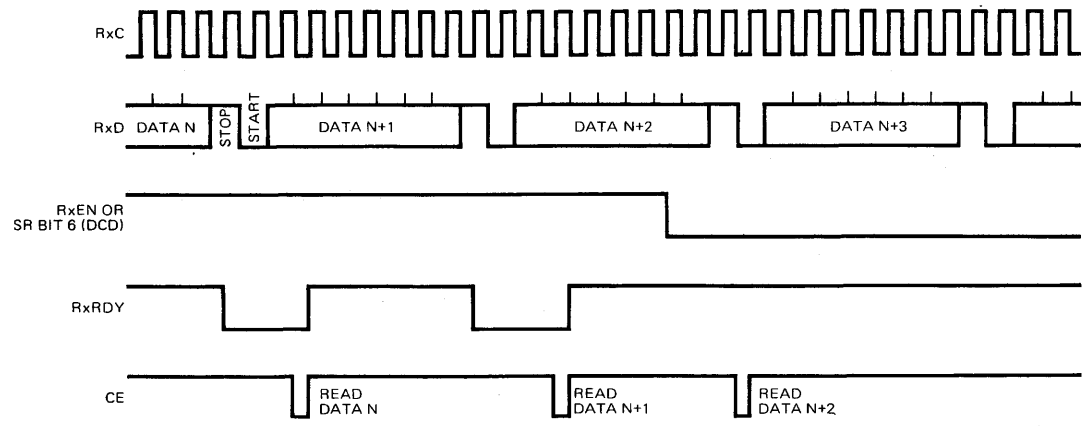


Figure 6. With Loss of $\overline{DCD}$ or Disabling RxEN

ASYNCHRONOUS RECEIVER OPERATION

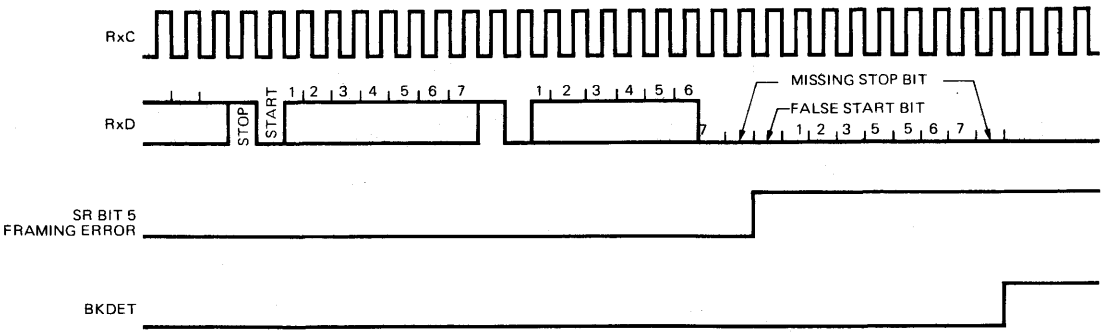


Figure 7. Framing Error and Break Detection Timing

Table 2. Baud Rate Generator Characteristics

UM2661-1 (BRCLK = 4.9152 MHz)

MR 2				Baud Rate	Actual Frequency 16X Clock (KHz)	Percent Error	Divisor
3	2	1	0				
0	0	0	0	50	0.8	–	6144
0	0	0	1	75	1.2	–	4096
0	0	1	0	110	1.7598	–0.01	2793
0	0	1	1	134.5	2.152	–	2284
0	1	0	0	150	2.4	–	2048
0	1	0	1	200	3.2	–	1536
0	1	1	0	300	4.8	–	1024
0	1	1	1	600	9.6	–	512
1	0	0	0	1050	16.8329	0.196	292
1	0	0	1	1200	19.2	–	256
1	0	1	0	1800	28.7438	–0.19	171
1	0	1	1	2000	31.9168	–0.26	154
1	1	0	0	2400	38.4	–	128
1	1	0	1	4800	76.8	–	64
1	1	1	0	9600	153.6	–	32
1	1	1	1	19200	307.2	–	16

UM2661-2 (BRCLK = 4.9152 MHz)

MR 2				Baud Rate	Actual Frequency 16X Clock (KHz)	Percent Error	Divisor
3	2	1	0				
0	0	0	0	45.5	0.7279	0.005	6752
0	0	0	1	50	0.8	–	6144
0	0	1	0	75	1.2	–	4096
0	0	1	1	110	1.7598	–0.01	2793
0	1	0	0	134.5	2.152	–	2284
0	1	0	1	150	2.4	–	2048
0	1	1	0	300	4.8	–	1024
0	1	1	1	600	9.6	–	512
1	0	0	0	1200	19.2	–	256
1	0	0	1	1800	28.7438	–0.19	171
1	0	1	0	2000	31.9168	–0.26	154
1	0	1	1	2400	38.4	–	128
1	1	0	0	4800	76.8	–	64
1	1	0	1	9600	153.6	–	32
1	1	1	0	19200	307.2	–	16
1	1	1	1	38400	614.4	–	8

UM2661-3 (BRCLK = 5.0688 MHz)

MR 2				Baud Rate	Actual Frequency 16X Clock (KHz)	Percent Error	Divisor
3	2	1	0				
0	0	0	0	50	0.8	–	6336
0	0	0	1	75	1.2	–	4224
0	0	1	0	110	1.76	–	2880
0	0	1	1	134.5	2.1523	0.016	2355
0	1	0	0	150	2.4	–	2112
0	1	0	1	300	4.8	–	1056
0	1	1	0	600	9.6	–	528
0	1	1	1	1200	19.2	–	264
1	0	0	0	1800	28.8	–	176
1	0	0	1	2000	32.081	0.253	158
1	0	1	0	2400	38.4	–	132
1	0	1	1	3600	57.6	–	88
1	1	0	0	4800	76.8	–	66
1	1	0	1	7200	115.2	–	44
1	1	1	0	9600	153.6	–	33
1	1	1	1	19200	316.8	3.126	16

Note: 16X CLK is used in asynchronous mode. In synchronous mode, clock multiplier is 1X and BRG can be used only for T x C

Signal Descriptions

CPU Interface

Reset (Reset)
A high on this input performs a master reset on the UM2661. This signal asynchronously terminates any device activity and clears the mode, command and status registers. The device assumes the idle state and remains there until initialized with the appropriate control words.

A0, A1 (Address 0, 1)
Address lines used to select the internal registers.

$\overline{R}$/W (Read/Write)
The direction of data transfers between the EPCI and the CPU is controlled by the R/W input. When CE and $\overline{R}$/W are both low the contents of the selected registers will be transferred to the data bus. With CE low and $\overline{R}$/W high a write to the selected register is performed.

$\overline{CE}$ (Chip Enable)
When low, the selected register will be accessed. When high the D0-D7 lines will be placed in the high impedance state.

D0-D7 (Data Bus)
An 8-bit three-state positive true data bus used to transfer commands, data and status between the EPCI and the CPU.

$\overline{TxRDY}$ (Transmitter Ready)
This output is the complement of status register bit SR0. When low, it indicates that the transmit data holding register (TxHR) is ready to accept a data character from the CPU. It goes high when the data character is loaded. This output is valid only when the transmitter is enabled. It is an open drain output which can be "wire-ORed" to the CPU interrupt.

$\overline{RxRDY}$ (Receiver Ready)
This output is the complement of status register bit SR1. When low, it indicates that the receive data holding register (RxHR) has a character ready for input to the CPU. It goes high when the RxHR is read by the CPU and also when the receiver is disabled. It is an open drain output which can be "wire-ORed" to the CPU interrupt line.

$\overline{TxEMT/DSCHG}$
This output is the complement of status register bit SR2. When low, it indicates that the transmitter has completed serialization of the last character loaded by the CPU, or that a change of state of the DSR or DCD inputs has occurred. This output goes high when the status register is read by the CPU if the TxEMT condition does not exist. Otherwise, the TxHR must be loaded by the CPU for this line to go high. It is an open drain output which can be "wire OR-ed" to the CPU interrupt line.

Transmitter/Receiver Signals

BRCLK (Baud Rate Clock)
Clock input to the internal baud rate generator. This is not required when external receiver and transmitter clocks are used.

$\overline{RxC}$/BKDET (Receiver Clock, Break Detect)
When the EPCI is programmed for External Receiver Clock, this pin will act as an input and control the rate at which a character is received. The frequency is programmed in Mode Register 1 and may be 1X, 16X or 64X the baud rate. Data are sampled on the rising edge. If internal Receiver Clock is programmed this pin will provide an output, either a 1X/16X clock or Break Detect signal determined by programming Mode Register 2.

$\overline{TxC}$/XSYNC (Transmitter Clock/External SYNC)
When the EPCI is programmed for External Transmitter clock, this pin will act as an input and control the rate at which the character is transmitted. The frequency is programmed in Mode Register 1 and may be 1X, 16X or 64X the baud rate. Data changes on the falling edge of this clock. If the UPCI is programmed for Internal Transmitter clock, this pin can be either an output providing a 1X/16X clock or an input for External Synchronization determined by Mode Register 2 programming.

RxD (Receive Data)
RxD is the serial data input to the receiver.

TxD (Transmit Data)
TxD is the serial data output from the transmitter. When the transmitter is disabled the output will be in the high, "Mark", state.

$\overline{DSR}$ (Data Set Ready)
$\overline{DSR}$ is an input that can be used to indicate to the UPCI Data Set Ready or Ring Indicator. Its complement appears in the Status Register as bit SR7. A change of state on $\overline{DSR}$ will cause $\overline{TxEMT/DSCHG}$ to go low if either CR0 or CR2=1.

$\overline{DCD}$ (Data Carrier Detect)
The $\overline{DCD}$ input must be low for the receiver to operate. If DCD goes high while receiving, the RxC is internally inhibited. The complement of $\overline{DCD}$ appears in the Status Register as bit SR6. A change of state in $\overline{DCD}$ will cause $\overline{TxEMT/DSCHG}$ to go low if either CR0 or CR2=1.

$\overline{CTS}$ (Clear To Send)
The $\overline{CTS}$ input must be low for the transmitter to operate. If $\overline{CTS}$ goes high while transmitting, the character currently in the Transmit Shift Register will be transmitted before termination, TxD will then go to the high level (Mark).

$\overline{\text{DTR}}$ (Data Terminal Ready)
The $\overline{\text{DTR}}$ output is the complement of CR1. It is normally used to indicate Data Terminal Ready.

$\overline{\text{RTS}}$ (Request To Send)
The $\overline{\text{RTS}}$ output is the complement of CR5. If the Transmit Shift Register is not empty when CR5 is reset, $\overline{\text{RTS}}$ will not go high until one TxC after the last serial bit is transmitted.

Functional Description

The internal organization of the EPCI consists of six major blocks, (see Fig. 1). These are the Transmitter, Receiver, Clock Control, Operation Control, Modem Control and SYN/DLE Control. These blocks internally communicate over common data and control buses. The data bus is also linked to the CPU via a bi-directional three-state interface. Briefly, these blocks perform the following functions:

Transmitter
The Transmitter receives parallel data from the CPU and converts it to a serial bit stream, inserting Start, Stop, and Parity bits, as selected by the user, and outputs a composite serial data stream.

Receiver
The Receiver accepts serial data from the sending device, converts it to parallel format checking for appropriate Start, Stop and Parity bits and Control Characters, as selected by the user, and sends the assembled character to the CPU.

Timing Control
The Timing Control block contains a programmable Baud Rate Generator (BRG) which is able to accept external Transmit ($\overline{\text{TxC}}$) or Receiver ($\overline{\text{RxC}}$) clocks or to divide external clock (BRCLK) for controlling data transfers. The BRCLK input allows the user to program one of 16 commonly used baud rates.

Operating Control
The Operation Control block contains four registers; Mode Registers 1 and 2, (MR1, MR2) the Command Register (CR) and Status Register (SR). These registers are used to store configuration and operation commands from the CPU. They generate the necessary internal control signals for proper device operation, and maintain status information for the CPU.

Modem Control
The modem control section provides interfacing for three input signals and three output signals used for "handshaking" and status indication between the CPU and a modem.

SYN/DLE Control
This section contains control circuitry and three 8-bit registers storing the SYN1, SYN2, and DLE characters provided by the CPU. These registers are used in the synchronous mode of operation to provide the characters required for synchronization, idle fill and data transparency.

Operational Description

The EPCI's operation is determined by programming the Mode and Command Registers. Baud rate, asynchronous or synchronous communication, and SYN characters are determined before enabling the transmitter or receiver.

Asynchronous Receiver Operation
After the Mode Registers are configured the receiver is enabled when the RxEN bit in the Command Register (CR2) is set to a 1 and $\overline{\text{DCD}}$ is low. The EPCI then monitors the RxD input waiting for a high to low transition. If a transition is detected, the RxD input is again sampled one-half bit time later. If RxD is now high, a search for a valid start bit is begun again. If RxD is still low a valid start bit is assumed and the receiver continues to sample the RxD input at one bit time intervals until the correct number of data bits, parity bit and one stop bit have been assembled. The character is then transferred to the Receive Data Holding Register (RxHR); RxRDY in the status Register is set (SR1); the $\overline{\text{RxRDY}}$ output goes low. If the character length is less than 8 bits, the high order unused bits in the holding register are set to zero. The parity error, framing error, and overrun error status bits are strobed into the status register on the positive going edge of $\overline{\text{RxC}}$ corresponding to the received character boundry. See Figures 3 and 6.

If the stop bit is present, the receiver will immediately begin its search for the next start bit. If the stop bit is absent (framing error), the receiver will interpret a space bit if it persists into the next bit time interval. If a break condition is detected (RxD is low for the entire character as well as the stop bit) only one character consisting of all zeros (with the FE status bit set) will be transferred to the holding register. The RxD input must return to a high condition before a search for the next start bit begins. See Figure 7.

Pin 25 can be programmed as a Break Detect (BKDET) output by setting both bits 4 and 7 of Mode Register 2 (MR2). When these bits are set and a break is detected, the BKDET output will go high. If RxD returns high for at least one RxD time. BKDET will return low.

Synchronous Receiver Operation
When the EPCI is programmed for synchronous operation, the receiver will remain idle until the receiver enable bit

(CR2) is set. At this time the EPCI enters the hunt mode. Data are shifted into the receive data shift register (RxSR) one bit at a time. The contents of RxSR are then compared to the contents of the SYN1 register. If the two are not equal, the next bit is shifted in and the comparison is repeated. When the two registers match, the hunt mode is terminated and character assembly mode begins. If single SYN operation is programmed, the SYN DETECT status bit is set. If double SYN operation is programmed, the first character assembled after SYN1 must be SYN2 in order for the SYN DETECT bit to be set. Otherwise the EPCI returns to the hunt mode. (Note that the sequence SYN1-SYN1-SYN2 will not achieve synchronization). See Figure 2.

When synchronization has been achieved, the EPCI continues to assemble characters and transfer them to the holding register, setting the $\overline{\text{RxRDY}}$ status bit and asserting the $\overline{\text{RxRDY}}$ output each time a character is transferred. The PE and OE status bits are set as appropriate. Further receipt of the appropriate SYN sequence sets the SYN DETECT status bit. If the SYN stripping mode is commanded, SYN characters are not transferred to the holding register. Note: the SYN characters used to establish initial synchronization are not transferred to the holding register in any case.

By setting MR24 (MR2 bit 4) and MR27=1 pin 9 ($\overline{\text{RxC}}$/SYNC) will be programmed as an external synchronization input. When XSYNC is selected internal SYN1, SYN1-SYN2 and DLE-SYN1 detection is disabled. Each positive going signal on XSYNC will cause the receiver to establish synchronization on the rising edge of the next RxC pulse. Character assembly will start with the RxD input at this edge. XSYNC must be lowered prior to the next rising edge of RxC. This external synchronization will cause the SYN DETECT status bit to be set until the status register is read. Refer to XSYNC timing diagram.

Asynchronous Transmitter Operation

When the EPCI is programmed to transmit, the transmitter will remain idle until $\overline{\text{CTS}}$ is low and the TxEN bit (CR0) is set. The EPCI will respond by setting status register (SR) bit 0 and asserting the $\overline{\text{TxRDY}}$ output. When the CPU writes a character into the transmit data holding register (TxHR), SR0 is reset and $\overline{\text{TxRDY}}$ returns high. The character is then transferred to the transmit shift register (TxSR) when it is idle or has completed transmission of the previous character. SR0 is again set, and $\overline{\text{TxRDY}}$ goes low. See Figure 5.

In the asynchronous mode, the transmitter automatically sends a start bit followed by the programmed number of data bits, the least significant bit being sent first. It then appends an optional odd or even parity bit and the programmed number of stop bits. If, following transmission of the data bits, a new character is not available in the transmit holding register, the TxD output remains in the marking (high) condition and the TxEMT/DSCHG output and its corresponding status bit are asserted. Transmission resumes when the CPU loads a new character into the holding register. The transmitter can be forced to output a continuous low (BREAK) condition by setting CR3.

Synchronous Transmitter Operation

When the ECPI is initially programmed for synchronous transmission it will remain in the idle state (RxD high) until TxEN is set. At this point TxD remains high, $\overline{\text{TxRDY}}$ will go low and both will stay in this state until the first character (usually a SYN character) is written into the TxHR. This starts transmission, with $\overline{\text{TxRDY}}$ going low each time a character is shifted from the TxHR to the TxSR. If $\overline{\text{TxRDY}}$ is not serviced before the previous character is shifted out of the TxSR, the $\overline{\text{TxEMT}}$ output will go low and the EPCI will automatically fill the pending gap with SYN1, SYN1, SYN2 doublets, or DLE-SYN1 doublets, depending on the state of MR6 and MR17. Transmission will be continuous until TxFN is reset to 0. See Figure 4.

If the send DLE bit (CR3) is set, the DLE character is automatically transmitted prior to the transmission of any character stored in the TxHR. Since this is a one time command, CR3 does not have to be reset.

EPCI Programming

Before data communications can be started the EPCI must be programmed by writing to its mode and command registers. Additionally, if synchronous communication has been selected the appropriate SYN1, SYN2 and DLE registers must be loaded. Reference the Register Addressing Table and Initialization Flow Chart for address requirements and programming procedure.

The Register Addressing Table shows MR1 and MR2 at the same address. The EPCI has an internal pointer that initially directs that first read or write to MR1, then on the next access at the same address the pointer directs the operation to MR2. A similar sequence occurs for the SYN and DLE registers; first SYN1 then SYN2 then DLE. If more than the required number of accesses are made the internal pointer resets to the first register. The pointer is also reset to MR1 and SYN1 by a RESET input or a read of the Command Register, but unaffected by any other read or write operation.

Register Formats

The register formats are summarized in Figures 8 through11 MR1 and MR2 define the general operating characteristics. The Command Register controls the basic operation defined by MR1 and MR2. The Status Register indicates the EPCI operating status and the condition of external

inputs. These registers are cleared by a RESET input (SR6 and SR7 excepted).

Mode Register 1 (MR1)

MR11 and MR10 select the communication mode and baud rate multiplier. Note: the multiplier in asynchronous mode applies only if the external input option is selected by MR24 and RM25.

MR13 and MR12 select Character length. Character length does not include the parity bit, when selected, and does not include the start and stop bits in asynchronous operation.

MR14, when set, selects parity. A parity bit will be transmitted with each character, and a parity check will be performed on each character received.

MR15 selects either odd or even parity.

In the asynchronous mode MR16 and MR17 select the number of stop bits; 1, 1.5 or 2, If 1X baud rate is programmed 1.5 stop bits defaults to 1 on transmit.

In the synchronous mode MR17 controls the number of SYN characters used to establish synchronization, and the number of fill characters to be transmitted when $\overline{\text{TxRDY}}$ and $\overline{\text{TxEMT}}$ are 0.

MR16 controls selection of the transparent mode. When MR16 is set (transparent selected) DLE-SYN1 is used for character fill and SYN detect (SR 5), but the normal synchronization sequence is used to establish character sync. When transmitting in the synchronous transparent mode, a DLE character in the TxHR will cause a second DLE character to be transmitted. Note: If the send DLE command (CR3) is active when a DLE character is in the TxHR, only one additional DLE will be transmitted.

The bits in the mode register affecting character assembly and disassembly (MR12–MR16) can be changed dynamically (during active receive/transmit operation). The character mode register affects both the transmitter and receiver; therefore in synchronous mode, changes should be made only in half duplex mode (RxEN=1 or TxEN=1, but not both simultaneously=1). In asynchronous mode, character changes should be made when RxEN and TxEN=0,or when TxEN=1 and the transmitter is marking in half duplex mode (RxEN=0).

To effect assembly/disassembly of the next received/transmitted character, MR12--15 must be changed within n bit times of the active going state of $\overline{\text{RxDRY}}/\overline{\text{TxRDY}}$. Transparent and non-transparent mode changes (MR16) must occur within n-1 bit times of the character to be affected when the receiver or transmitter is active. (n = the smaller of the new and old character lengths.)

Mode Register 2 (MR2)

MR20 through MR23 select the internal Baud Rate Generator (BRG). There are sixteen selectable rates for each version as outlined in Table 2.

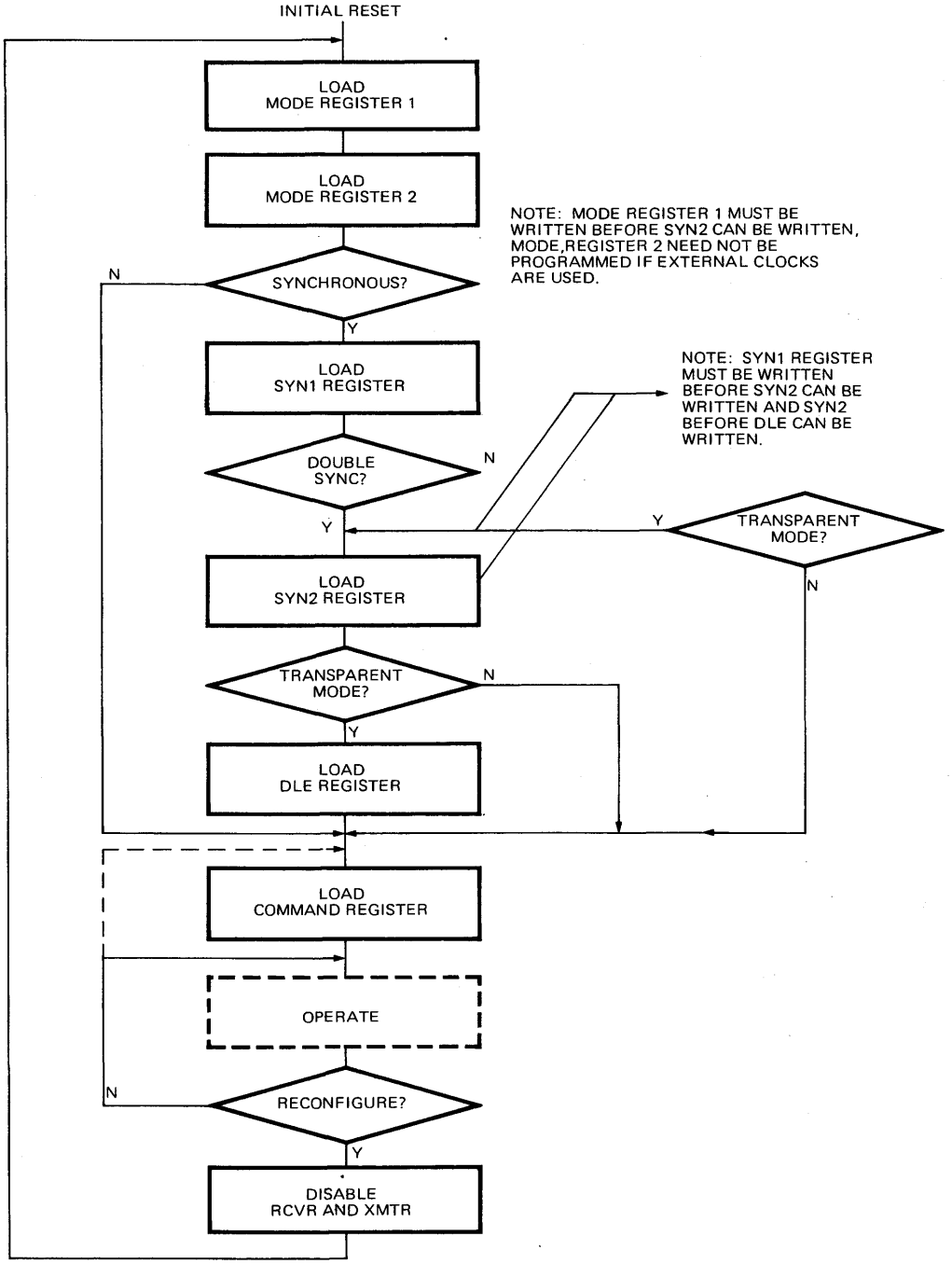
MR24 through MR27 define the receive and transmit clock source and the function of pins 9 and 25. Reference Figure 9.

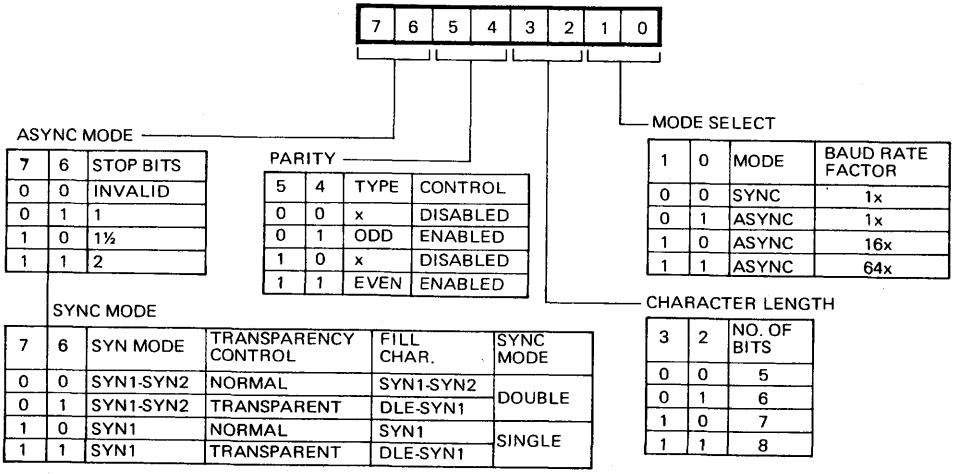
I/O And Peripherals

Table 3. UM2661 Register Addressing

CE	A_1	A_0	$\overline{R/W}$	Function
1	X	X	X	Three-state Data Bus
0	0	0	0	Read Receive Holding Register (RxHR)
0	0	0	1	Write Transmit Holding Register (TxHR)
0	0	1	0	Read Status Register (SR)
0	0	1	1	Write SYN1/SYN2/DLE Registers
0	1	0	0	Read Mode Registers (MR1, MR1/MR2)
0	1	0	1	Write Mode Registers (MR1, MR1/MR2)
0	1	1	0	Read Command Register
0	1	1	1	Write Command Register

EPCI Initialization Flow Chart





7	6	STOP BITS
0	0	INVALID
0	1	1
1	0	1½
1	1	2

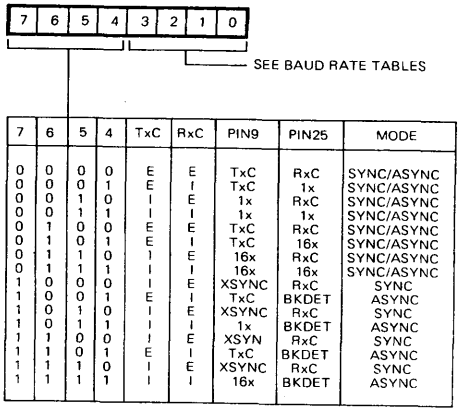
5	4	TYPE	CONTROL
0	0	x	DISABLED
0	1	ODD	ENABLED
1	0	x	DISABLED
1	1	EVEN	ENABLED

1	0	MODE	BAUD RATE FACTOR
0	0	SYNC	1x
0	1	ASYNC	1x
1	0	ASYNC	16x
1	1	ASYNC	64x

3	2	NO. OF BITS
0	0	5
0	1	6
1	0	7
1	1	8

7	6	SYN MODE	TRANSPARENCY CONTROL	FILL CHAR.	SYNC MODE
0	0	SYN1-SYN2	NORMAL	SYN1-SYN2	DOUBLE
0	1	SYN1-SYN2	TRANSPARENT	DLE-SYN1	
1	0	SYN1	NORMAL	SYN1	SINGLE
1	1	SYN1	TRANSPARENT	DLE-SYN1	

Figure 8. Mode Register 1



7	6	5	4	TxC	RxC	PIN9	PIN25	MODE
0	0	0	0	E	E	TxC	RxC	SYNC/ASYNC
0	0	0	1	E	I	TxC	1x	SYNC/ASYNC
0	0	1	0	I	E	1x	RxC	SYNC/ASYNC
0	0	1	1	I	I	1x	1x	SYNC/ASYNC
0	1	0	0	E	E	TxC	RxC	SYNC/ASYNC
0	1	0	1	E	I	TxC	16x	SYNC/ASYNC
0	1	1	0	I	E	16x	RxC	SYNC/ASYNC
0	1	1	1	I	I	16x	16x	SYNC/ASYNC
1	0	0	0	I	E	XSYNC	RxC	SYNC
1	0	0	1	E	I	TxC	BKDET	ASYNC
1	0	1	0	I	E	XSYNC	RxC	SYNC
1	0	1	1	I	I	1x	BKDET	ASYNC
1	1	0	0	I	E	XSYN	RxC	SYNC
1	1	0	1	E	I	TxC	BKDET	ASYNC
1	1	1	0	I	E	XSYNC	RxC	SYNC
1	1	1	1	I	I	16x	BKDET	ASYNC

Figure 9. Function of Pin 9 and Pin 25

Command Register (CR)

CR0 (TxEN) will enable or disable the transmitter. When TxEN=0, TxD, $\overline{\text{TxRDY}}$ and $\overline{\text{TxEMT}}$ are all high, the transmitter is disabled. When TxEN goes active, $\overline{\text{TxRDY}}$ will go low requesting the first character to be written to the TxHR, and the TxD output will be enabled to transmit. When TxEN goes inactive, the UPCI will complete transmission of any character still in the TxSR. TxD will then go to the marking state and $\overline{\text{TxRDY}}$ and $\overline{\text{TxEMT}}$ will go high. Refer to Transmit timing diagram.

CR1 controls the $\overline{\text{DTR}}$ output. The $\overline{\text{DTR}}$ output is a logical complement of CR1.

CR2 (RxEN) will enable or disable the receiver. When RxEN=0, the receiver is in an idle mode with $\overline{\text{RxRDY}}$ high. A 0 to 1 transition of RxEN will initiate a start bit search in asynchronous mode or initiate the hunt mode in synchronous transmission. A 1 to 0 transition of RxEN immediately terminates receiver operation.

In the asynchronous mode setting CR3 will force the TxD output low (break condition) at the end of the current transmitted character. TxD will then remain low until CR3 is cleared; at that time TxD will go high for a minimum 1 bit time before resuming normal transmission.

In the synchronous mode setting CR3 will force the transmission of the DLE character prior to sending the character in the TxHR. Because this is a one-time command, bit 3 will automatically reset.

CR5 controls the state of the $\overline{\text{RTS}}$ output. When CR5=1, $\overline{\text{RTS}}$ will go low and the transmit logic will be enabled. A 1 to 0 transition of CR5 will cause $\overline{\text{RTS}}$ to go high one TxC time after the last serial bit is transmitted, (if the TxSR was not already empty).

CR7 and CR6 provide four alternate modes of operation in both synchronous and asynchronous operation. When both bits are 0 normal operation is selected.

In the asynchronous mode, when only CR6 is set automatic echo mode is selected Clocked, regenerated received data are automatically directed to the TxD line while normal receiver operation continues. The receiver must be enabled (CR2=1), but the transmitter need not be enabled. CPU to receiver communications continue normally, but the CPU to transmitter link is disabled. Only the first character of a break condition is echoed. The TxD output will go high until the next valid start is detected. The following conditions are true while in automatic echo mode:

1. Data assembled by the receiver is automatically placed in the transmit holding register and re-transmitted by the transmitter on the TxD output.
2. Transmit clock = receive clock.
3. $\overline{\text{TxRDY}}$ output = 1.
4. The $\overline{\text{TxEMT/DSCHG}}$ pin will reflect only the data set change condition.
5. The TxEN command (CR0) is ignored.

In the synchronous mode, when only the CR6 is set automatic SYN/DLE stripping is performed. The state of MR17 and MR16 controls which characters are stripped. Reference Figure 10 for a detailed example of the characters stripped.

Note: automatic stripping does not affect setting of the SYN and DLE detect status bits.

Two diagnostic modes are achievable in both synchronous and asynchronous operation; local loopback with CR7=1 and CR6=0, and remote loopback with both bits=1.

Local Loop Back

1. The transmitter output is connected to the receiver input.
2. $\overline{\text{DTR}}$ is connected to $\overline{\text{DCD}}$ and $\overline{\text{RTS}}$ is connected to $\overline{\text{CTS}}$.
3. Transmit clock is connected to the receive clock.
4. The $\overline{\text{DTR}}$, $\overline{\text{RTS}}$ and $\overline{\text{TxD}}$ outputs are held high.
5. The $\overline{\text{CTS}}$, $\overline{\text{DCD}}$, $\overline{\text{DSR}}$ and $\overline{\text{RxD}}$ inputs are ignored.

Note: CR bits 0, 1 and 5 must be set, CR2 is a don't care.

Remote Loop Back

1. Data assembled by the receiver are automatically placed in the transmit holding register and re-transmitted by the transmitter on the TxD output.
2. Receive clock is connected to the transmit clock.
3. No data are sent to the local CPU, but the error status conditions (PE, OE, FE) are set.
4. The $\overline{\text{RxRDY}}$, $\overline{\text{TxRDY}}$, and $\overline{\text{TxEMT/DSCHG}}$ outputs are held high.
5. CR1 (TxEN) is ignored.
6. All other signals operate normally.

Status Register

SRD is the transmitter ready ($\overline{\text{TxRDY}}$) status, it is the logical complement of the $\overline{\text{TxRDY}}$ output. This bit indicates the state of the TxHR when the transmitter is enabled (TxEN=1). A 0 indicates TxHR is full, a 1 indicates TxHR is empty and requires servicing by the CPU. This bit is cleared by writing to TxHR or by disabling the transmitter (TxEN=0). Note: SRO is not set in either the auto echo or remote loop back modes.

SR1 is the receiver ready (RxRDY) status. It is the logical complement of the $\overline{\text{RxRDY}}$ output. This bit indicates the state of the RxHR when the receiver is enabled (RxEN=1). A 0 indicates the RxHR is empty, a 1 indicates the RxHR is full and requires servicing by the CPU. This bit is cleared by writing to the TxHR or by disabling the receiver. (RxEN=0).

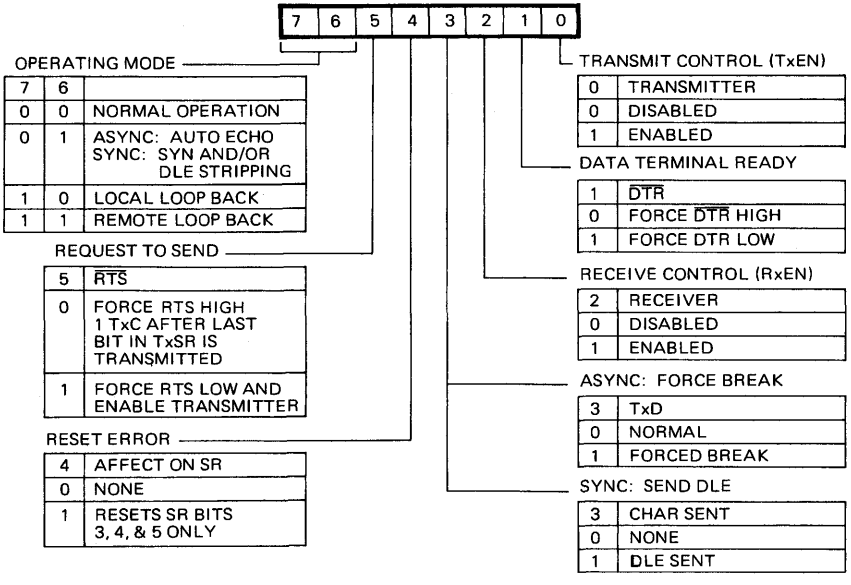


Figure 10. Command Register

SR2 indicates a change of state of either $\overline{DSR}$ or $\overline{DCD}$ or that the TxSR is empty. This bit is the logical complement of the $\overline{TxEMT/DSCHG}$ output. A reading of the status register will clear bit 2 if a state change on DSR or $\overline{DCD}$ has occurred. If a second successive read of the status register indicates bit 2=0, then $\overline{DCD}$ or $\overline{DSR}$ changes. If bit 2 is still set, then the TxSR is empty. Because the transmitter does not start until the first character has been written to the TxHR, $\overline{TxEMT}$ status will not be reflected until transmission of the first character is complete, $\overline{TxEMT}$ status is cleared by writing to the TxHR or disabling the transmitter. Note: $\overline{TxEMT}$ status will be set in synchronous mode even though "fill" characters are being transmitted.

SR3 when set reflects a parity error when parity checking is enabled in both the synchronous and asynchronous modes. In the synchronous transparent mode, (MR16=1) and the parity enable bit (MR14) is 0, SR3 will then indicate DLE detect when set. This indicates that a character matching DLE register was received and the present character is neither SYN1 nor DLE. This bit is cleared when the next character following the above sequence is loaded into the RxHR, when the receiver is disabled or by a reset error command.

SR4 indicates an overrun error when set. An overrun condition exists when the CPU does not read the RxHR before the next received character is transferred to it. (The previous character is lost.) SR4 is cleared by the reset error command and when the receiver is disabled.

In the asynchronous mode SR5 indicates that the received character was not framed by a stop bit. If the RxHR is all 0's when bit 5 is set, a break condition was present. In synchronous non-transparent mode, it indicates receipt of the SYN1 character in single SYN mode or the SYN1-SYN2 pair in double SYN mode. In synchronous transparent mode this bit is set upon detection of the initial synchronizing characters (SYN1 or SYN1-SYN2) and after synchronization has been achieved, when a DLE-SYN1 pair is received. The bit is reset when the receiver is disabled, when the reset error command is given in asynchronous mode, and when the status register is read by the CPU in the synchronous mode.

SR6 and SR7 reflect the condition of the $\overline{DCD}$ and $\overline{DSR}$ inputs respectively. Their state is the logical complement of their respective inputs.

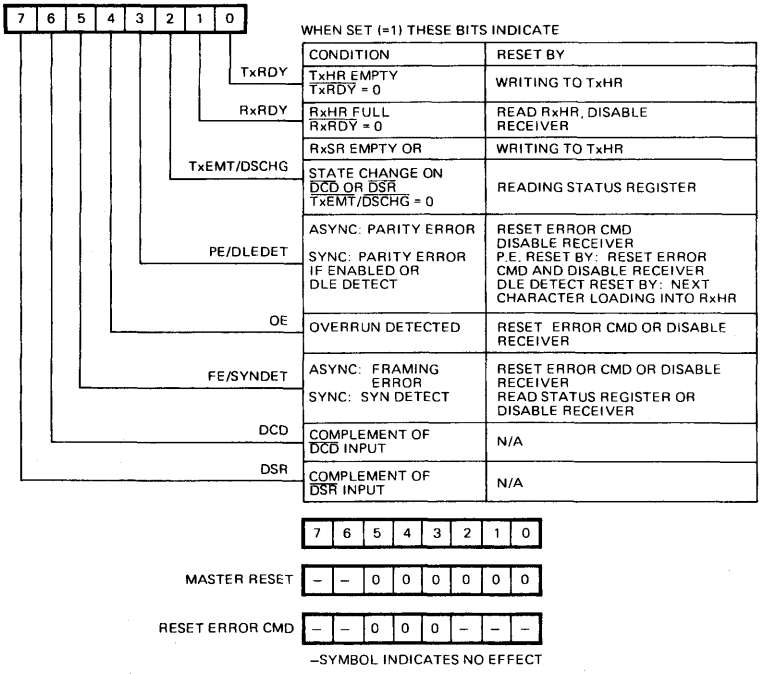


Figure 11. Status Register

Ordering Information

Part Number	BRCLK	Baud Rate
UM2661-1	4.9152 MHz	50 ~19200
UM2661-2	4.9152 MHz	45.5~38400
UM2661-3	5.0688 MHz	50 ~19200

UMC

UMC

UM6522/A

Versatile Interface Adapter(VIA)

Features

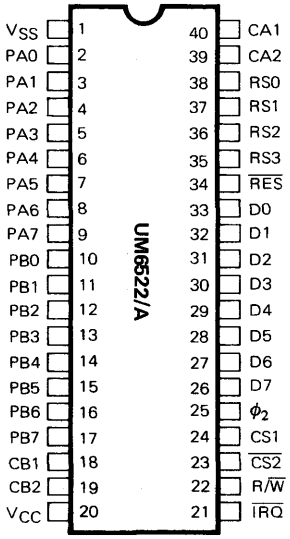
- Two 8-bit bi-directional I/O ports
- Two 16-bit programmable timer/counters
- Serial data port
- Single +5V power supply
- TTL compatible except Port A
- CMOS compatible peripheral Port A lines
- Expanded "handshake" capability allows positive control of data transfers between processor and peripheral devices
- Latched input and output registers
- 1 MHz and 2 MHz operation

General Description

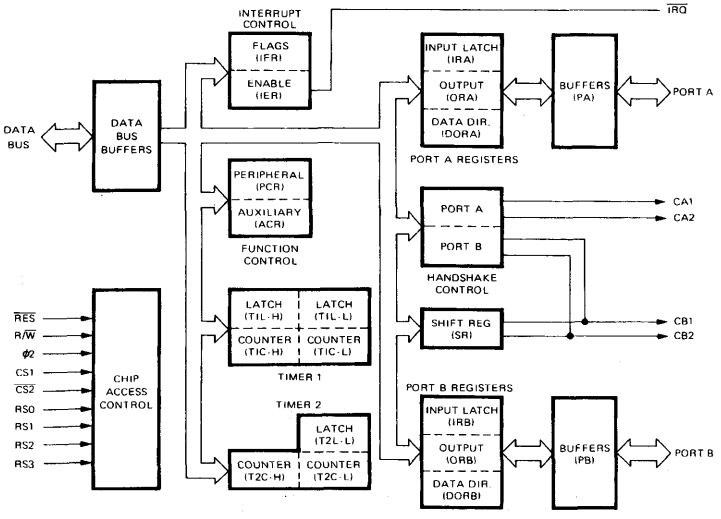
The UM6522/A Versatile Interface Adapter (VIA) is a very flexible I/O control device. In addition, this device contains a pair of very powerful 16-bit interval timers, a serial-to-parallel/parallel-to-serial shift register and input data latching on the peripheral ports. Expanded handshaking capability allows control of bi-directional data transfers between VIA's in multiple processor systems.

Control of peripheral devices is handled primarily through two 8-bit bi-directional ports. Each line can be programmed as either an input or an output. Several peripheral I/O lines can be controlled directly from the interval timers for generating programmable frequency square waves or for counting externally generated pulses. To facilitate control of the many powerful features of this chip, an interrupt flag register, an interrupt enable register and a pair of function control registers are provided.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Supply Voltage . . . . . +8.0 VOLTS
Operating Voltage Range . . . . . +4V to +7V
Input Voltage Applied . . . . . GND–2.0V to 6.5V
I/O Pin Voltage Applied . . . . . GND–0.5V to V_{CC} +0.5V
Storage Temperature Range . . . . . –65°C to +150°C
Operating Temperature Range . . . . . 0°C to +70°C
Maximum Power Dissipation . . . . . 1 Watt

*Comments

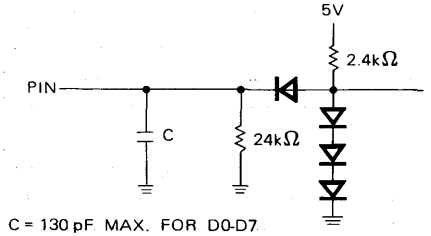
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

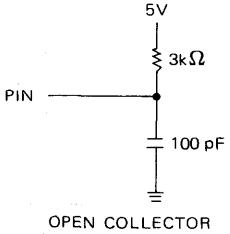
(V_{CC} = 5.0V ± 5%, T_A = 0 – 70°C unless otherwise noted)

Symbol	Parameter	Min.	Max.	Unit
V_{IH}	Input High Voltage (all except $\phi 2$)	2.4	V_{CC}	V
V_{CH}	Clock High Voltage	2.4	V_{CC}	V
V_{IL}	Input Low Voltage	–0.3	0.4	V
I_{IN}	Input Leakage Current – V_{IN} = 0 to 5 Vdc R/$\overline{W}$, $\overline{RES}$, RS0, RS1, RS2, RS3, CS1, $\overline{CS2}$, CA1, $\phi 2$	–	±2.5	μA
I_{TSI}	Off-state Input Current – V_{IN} = 0.4 to 2.4V V_{CC} = Max, D0 to D7	–	±10	μA
I_{IH}	Input High Current – V_{IH} = 2.4V PA0–PA7, CA2, PB0–PB7, CB1, CB2	–100	–	μA
I_{IL}	Input Low Current – V_{IL} = 0.4 Vdc PA0–PA7, CA2, PB0–PB7, CB1, CB2	–	–1.6	mA
V_{OH}	Output High Voltage V_{CC} = min, I_{load} = –100 μAdc PA0–PA7, CA2, PB0–PB7, CB1, CB2	2.4	–	V
V_{OL}	Output Low Voltage V_{CC} = min, I_{load} = 1.6 mAdc	–	0.4	V
I_{OH}	Output High Current (Sourcing) V_{OH} = 2.4V V_{OH} = 1.5V (PB0–PB7)	 –100 –1.0	 – –	 μA mA
I_{OL}	Output Low Current (Sinking) V_{OL} = 0.4 Vdc	1.6	–	mA
I_{OFF}	Output Leakage Current (Off state) $\overline{IRQ}$	–	10	μA
C_{IN}	Input Capacitance – T_A = 25°C, f = 1 MHz (R/$\overline{W}$, $\overline{RES}$, RS0, RS1, RS2, RS3, CS1, $\overline{CS2}$, D0–D7, PA0–PA7, CA1, CA2, PB0–PB7) (CB1, CB2) ($\phi 2$ Input)	– – –	7.0 10 20	pF pF pF
C_{OUT}	Output Capacitance – T_A = 25°C, f = 1 MHz	–	10	pF
P_D	Power Dissipation (V_{CC} = 5.25V)	–	700	mW

Test Load



C = 130 pF MAX. FOR D0-D7
C = 30 pF MAX. FOR ALL OTHER OUTPUTS



OPEN COLLECTOR
OUTPUT TEST LOAD

Figure 2. Test Load (for all Dynamic Parameters)

I/O And Peripherals

Read Timing Characteristics (Figure 3.)

Symbol	Parameter	UM6522		UM6522A		Unit
		Min.	Max.	Min.	Max.	
T_{CY}	Cycle Time	1	50	0.5	50	μs
T_{ACR}	Address Set-Up Time	180	–	90	–	ns
T_{CAR}	Address Hold Time	0	–	0	–	ns
T_{PCR}	Peripheral Data Set-Up Time	300	–	300	–	ns
T_{CDR}	Data Bus Delay Time	–	340	–	200	ns
T_{HR}	Data Bus Hold Time	10	–	10	–	ns

Note: tr, tf = 10 to 30ns.

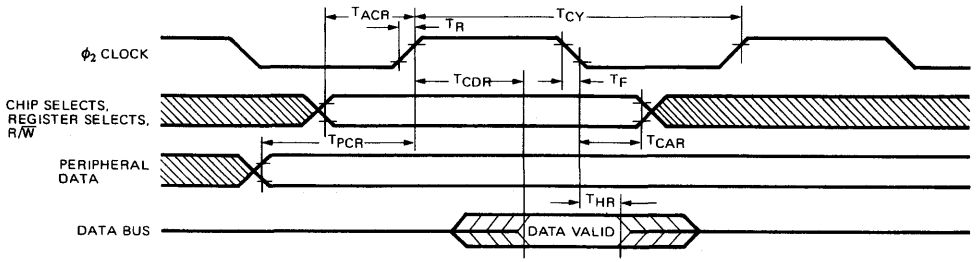


Figure 3. Read Timing Characteristics

Write Timing Characteristics (Figure 4.)

Symbol	Parameter	UM6522		UM6522A		Unit
		Min.	Max.	Min.	Max.	
T_{CY}	Cycle Time	1	50	0.50	50	μs
T_C	φ2 Pulse Width	0.44	25	0.22	25	μs
T_{ACW}	Address Set-Up Time	180	–	90	–	ns
T_{CAW}	Address Hold Time	0	–	0	–	ns
T_{WGW}	R/$\overline{W}$ Set-Up Time	180	–	90	–	ns
T_{CWW}	R/$\overline{W}$ Hold Time	0	–	0	–	ns
T_{DCW}	Data Bus Set-Up Time	300	–	150	–	ns
T_{HW}	Data Bus Hold Time	10	–	10	–	ns
T_{CPW}	Peripheral Data Delay Time	–	1.0	–	1.0	μs
T_{CMOS}	Peripheral Data Delay Time to CMOS Levels	–	2.0	–	2.0	μs

Note: tr, tf = 10 to 30ns.

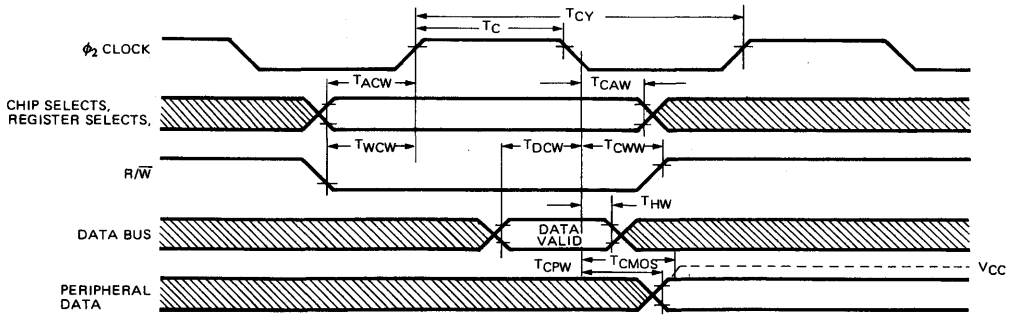


Figure 4. Write Timing Characteristics

Peripheral Interface Characteristics

Symbol	Parameter	Min.	Max.	Typ.	Unit	Figure
t_r, t_f	Rise and Fall Time for CA1, CB1, CA2, and CB2 Input Signals	–	1.0		μs	–
T_{CA2}	Delay Time, Clock Negative Transition to CA2, Negative Transition (read handshake or pulse mode)	–	1.0		μs	5a, 5b
T_{RS}	Delay Time, Clock Negative Transition to CA2, Positive Transition (pulse mode)	–	1.0		μs	5a
T_{RS2}	Delay Time, CA1 Active Transition to CA2, Positive Transition (handshake mode)	–	2.0		μs	5b
T_{WHS}	Delay Time, Clock Positive Transition to CA2 or CB2, Negative Transition (write handshake)	0.05	1.0		μs	5c, 5d
T_{DS}	Delay Time, Peripheral Data Valid to CB2, Negative Transition	0.20	1.5		μs	5c, 5d
T_{RS3}	Delay Time, Clock Transition to CA2 or CB2, Positive Transition (pulse mode)	–	1.0		μs	5c
T_{RS4}	Delay Time, CA1 or CB1 Active Transition to CA2 or CB2, Positive Transition (handshake mode)	–	2.0		μs	5d
T_{21}	Delay Time Required from CA2 Output to CA1, Active Transition (handshake mode)	400	–		ns	5d
T_{IL}	Set-up Time, Peripheral Data Valid to CA1 or CB1, Active Transition (input latching)	300	–		ns	5e
T_{SR1}	Shift-Out Delay Time – Time from ϕ_2 Falling Edge to CB2, Data Out	–	300		ns	5f
T_{SR2}	Shift-In Setup Time – Time from CB2 Data in to ϕ_2 Rising Edge	300	–		ns	5g
T_{SR3}	External Shift Clock (CB1) Setup Time Relative to ϕ_2 Trailing Edge	100	T_{CY}		ns	5g
T_{IPW}	Pulse Width – PB6 Input Pulse	2 x T_{CY}	–			5i
T_{ICW}	Pulse Width – CB1 Input Clock	2 x T_{CY}	–			5h
T_{IPS}	Pulse Spacing – PB6 Input Pulse	2 x T_{CY}	–			5i
T_{ICS}	Pulse Spacing – CB1 Input Pulse	2 x T_{CY}	–			5h
T_{AI}	CA1, CB1 Set-Up Prior to Transition to Arm Latch	T_C + 50	–		ns	5h
T_{PDH}	Peripheral Data Hold After CA1, CB1 Transition	150	–		ns	5e
T_{PWI}	Set-Up Required on CA1, CB1, CA2 or CB2 Prior to Triggering Edge	T_C + 50	–		ns	5j
	Shift Register Clock – Delay from ϕ_2					
T_{DPR}	to CB1 Rising Edge			200	ns	5k
T_{DPL}	to CB1 Falling Edge			125	ns	5k

Timing Waveforms

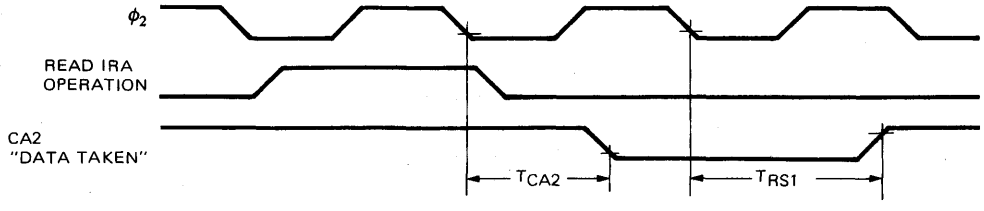


Figure 5a. CA2 Timing for Read Handshake, Pulse Mode

Timing Waveforms (Continued)

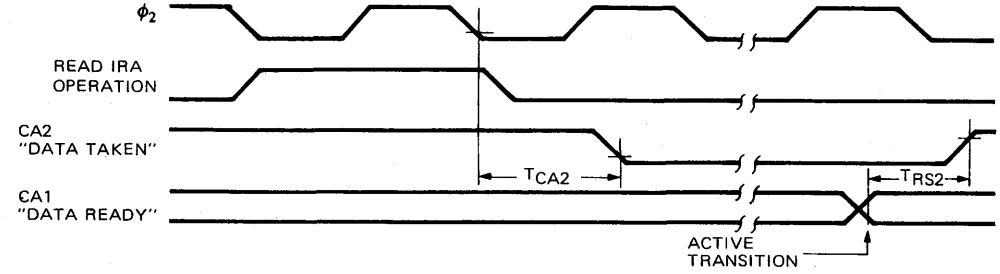


Figure 5b. CA2 Timing for Read Handshake, Handshake Mode

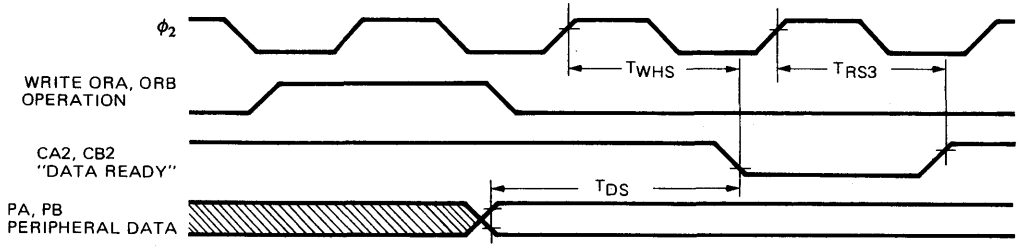


Figure 5c. CA2, CB2 Timing for Write Handshake, Pulse Mode

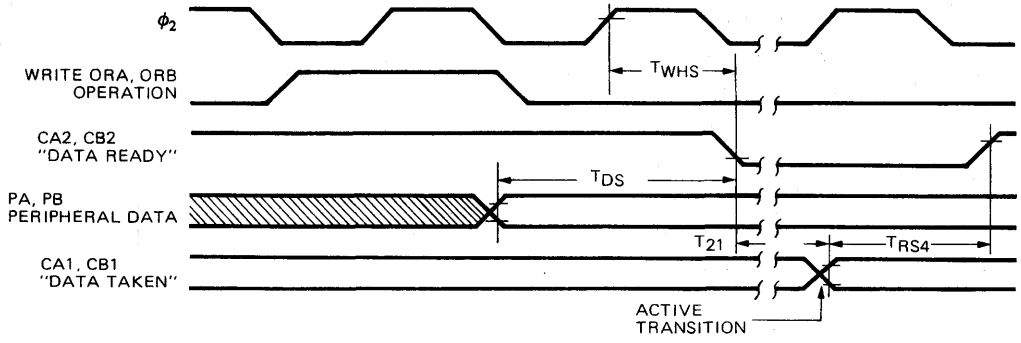


Figure 5d. CA2, CB2 Timing for Write Handshake, Handshake Mode

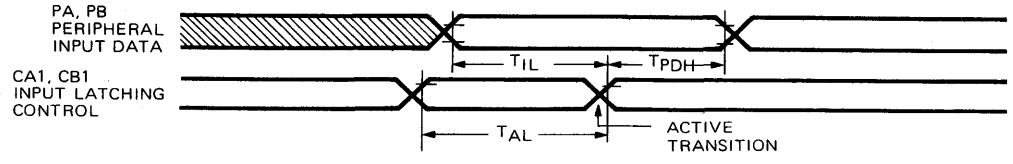


Figure 5e. Peripheral Data Input Latch Timing

Timing Waveforms (Continued)

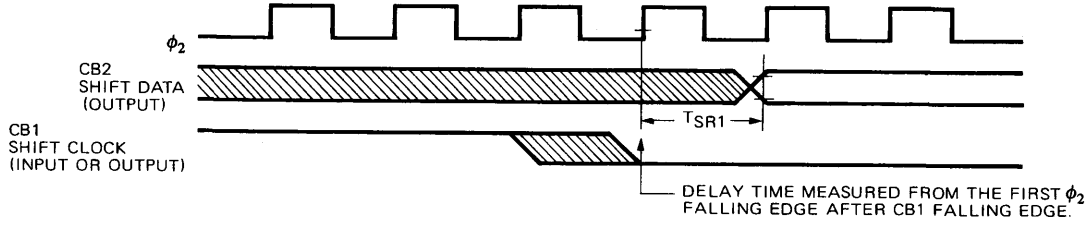


Figure 5f. Timing for Shift Out with Internal or External Shift Clocking

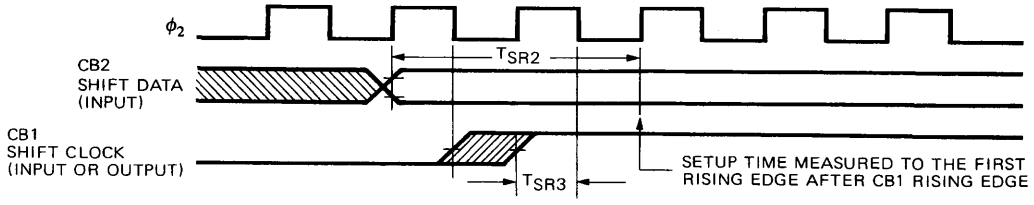


Figure 5g. Timing for Shift In with Internal or External Shift Clocking

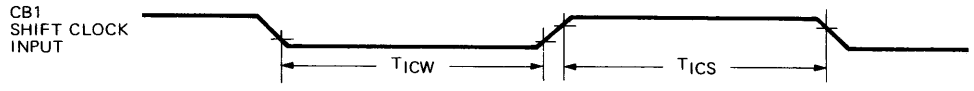


Figure 5h. External Shift Clocking

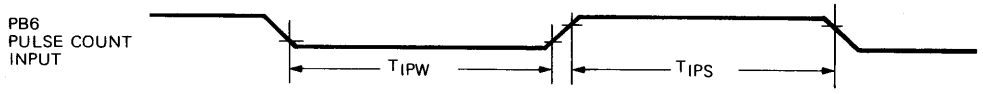


Figure 5i. Pulse Count Input Timing

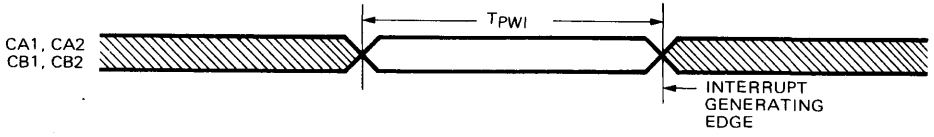


Figure 5j. Setup Time to Trigger Edge

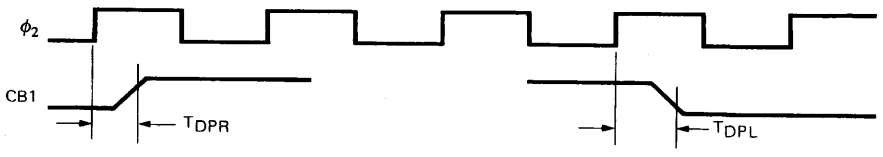


Figure 5k. Shift-in/out with Internal Clock Delay CD2 to CB1 Edge

Pin Description

$\overline{RES}$ (Reset)

The reset input clears all internal registers to logic "0" (except T1 and T2 latches and counters and the Shift Register). This places all peripheral interface lines in the input state, disables the timers, shift register, etc. and disables interrupting from the chip.

$\phi 2$ (Input Clock)

The input clock is the system $\phi 2$ clock and is used to trigger all data transfers between the system processor and the UM6522/A.

R/$\overline{W}$ (Read/Write)

The direction of the data transfers between the UM6522/A and the system processor is controlled by the R/$\overline{W}$ line. If R/$\overline{W}$ is low, data will be transferred out of the processor into the selected UM6522/A register (write operation). If R/$\overline{W}$ is high and the chip is selected, data will be transferred out of the UM6522/A (read operation).

DB0-DB7 (Data Bus)

The eight bi-directional data bus lines are used to transfer data between the UM6522/A and the system processor. During read cycles, the contents of the selected UM6522/A register are placed on the data bus lines and transferred into the processor. During write cycles, these lines are high-impedance inputs and data is transferred from the processor into the selected register. When the UM6522/A is unselected, the data bus lines are high-impedance.

CS1, $\overline{CS2}$ (Chip Selects)

The two chip select inputs are normally connected to processor address lines either directly or through decoding. The selected UM6522/A register will be accessed when CS1 is high and $\overline{CS2}$ is low.

RS0-RS3 (Register Selects)

The four Register Select inputs permit the system processor to select one of the 16 internal registers of the UM6522/A, as shown in Figure 6.

$\overline{IRQ}$ (Interrupt Request)

The Interrupt Request output goes low whenever an internal interrupt flag is set and the corresponding interrupt enable bit is a logic "1". This output is "open-drain" to allow the interrupt request signal to be wire-ORed with other equivalent signals in the system.

Register Number	RS Coding				Register Desig.	Description	
	RS3	RS2	RS1	RS0		Write	Read
0	0	0	0	0	ORB/IRB	Output Register "B"	Input Register "B"
1	0	0	0	1	ORA/IRA	Output Register "A"	Input Register "A"
2	0	0	1	0	DDRB	Data Direction Register "B"	
3	0	0	1	1	DDRA	Data Direction Register "A"	
4	0	1	0	0	T1C-L	T1 Low-Order Latches	T1 Low-Order Counter
5	0	1	0	1	T1C-H	T1 High-Order Counter	
6	0	1	1	0	T1L-L	T1 Low-Order Latches	
7	0	1	1	1	T1L-H	T1 High-Order Latches	
8	1	0	0	0	T2C-L	T2 Low-Order Latches	T2 Low-Order Counter
9	1	0	0	1	T2C-H	T2 High-Order Counter	
10	1	0	1	0	SR	Shift Register	
11	1	0	1	1	ACR	Auxiliary Control Register	
12	1	1	0	0	PCR	Peripheral Control Register	
13	1	1	0	1	IFR	Interrupt Flag Register	
14	1	1	1	0	IER	Interrupt Enable Register	
15	1	1	1	1	ORA/IRA	Same as Reg 1 Except No. "Handshake"	

Figure 6. UM6522/A Internal Register Summary

PA0-PA7 (Peripheral A Port)

The Peripheral A port consists of 8 lines which can be individually programmed to act as inputs or outputs under control of a Data Direction Register. The polarity of output pins is controlled by an Output Register and input data may be latched into an internal register under control of the CA1 line. All of these modes of operation are controlled by the system processor through the internal control registers. These lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. Figure 7 illustrates the output circuit.

CA1, CA2 (Peripheral A Control Lines)

The two Peripheral A control lines act as interrupt inputs or as handshake outputs. Each line controls an internal interrupt flag with a corresponding interrupt enable bit. In addition, CA1 controls the latching of data on Peripheral A port input lines. CA1 is a high impedance input only; while CA2 represents one standard TTL load in the input mode. CA2 will drive one standard TTL load in the output mode.

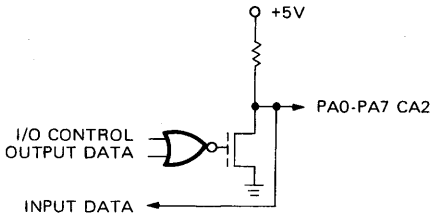


Figure 7. Peripheral A Port Output Circuit

PB0-PB7 (Peripheral B Port)

The Peripheral B port consists of eight bi-directional lines which are controlled by an output register and a data direction register in much the same manner as the PA port. In addition, the PB7 output signal can be controlled by one of the interval timers while the second timer can be programmed to count pulses on the PB6 pin. Peripheral B lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. In addition, they are capable of sourcing 1.0mA at 1.5VDC in the output mode to allow the outputs to directly drive Darlington transistor circuits. Figure 8 is the circuit schematic.

CB1, CB2 (Peripheral B Control Lines)

The Peripheral B control lines act as interrupt inputs or as handshake outputs. As with CA1 andCA2, each line controls an interrupt flag with a corresponding interrupt enable bit. In addition, these lines act as a serial port under control of the Shift Register. These lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. Unlike PB0-PB7. CB1 and CB2 cannot drive Darlington transistor circuits.

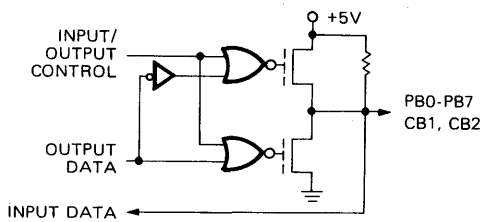


Figure 8. Peripheral B Port Output Circuit

Functional Description

Port A and Port B Operation

Each 8-bit peripheral port has a Data Direction Register (DDRA, DDRB) for specifying whether the peripheral pins are to act as inputs or outputs. A "0" in a bit of the Data Direction Register causes the corresponding peripheral pin to act as an input. A "1" causes the pin to act as an output.

When programmed as an output each peripheral pin is also controlled by a corresponding bit in the Output Register (ORA' ORB). A "1" in the Output Register causes the output to go high, and a "0" causes the output to go low. Data may be written into Output Register bits corresponding to pins which are programmed as inputs. In this case, however, the output signal is unaffected.

Reading a peripheral port causes the contents of the Input Register (IRA, IRB) to be transferred onto the Data Bus. With input latching disabled, IRA will always reflect the levels on the PA pins. With input latching enabled and the selected active transition on CA1 having occurred, IRA will contain the data present on the PA lines at the time of the transition. Once IRA is read, however, it will appear transparent, reflecting the current state of the PA lines until the next "latching" transition.

The IRB register operates similar to the IRA register. However, for pins programmed as outputs there is a difference. When reading IRA, the level on the pin determines whether a "0" or a "1" is sensed. When reading IRB, however, the bit stored in the output register, ORB, is the bit sensed. Thus, for outputs which have large loading effects and which pull an output "1" down or which pull an output "0" up, reading IRA may result in reading a "0" when a "1" was actually programmed, and reading a "1" when a "0" was programmed. Reading IRB, on the other hand, will read the "1" or "0" level actually programmed, no matter what the loading on the pin.

Figures 9, 10 and 11 illustrate the formats of the port registers. In addition, the input latching modes are selected by the Auxiliary Control Register (Figure 17.)

Handshake Control of Data Transfer

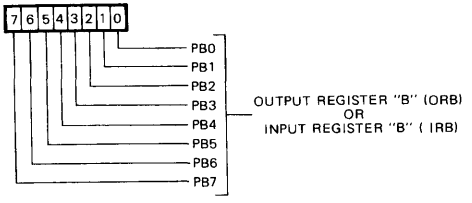
The UM6522/A allows positive control of data transfer between the system processor and peripheral devices through the operation of "handshake" lines. Port A lines (CA1, CA2) handshake data on both a read and a write operation while the Port B lines (CB1, CB2) handshake on a write operation only.

Read Handshake

Positive control of data transfer from peripheral devices into the system processor can be accomplished very effectively using Read Handshaking. In this case, the peripheral device must generate the equivalent of a "Data Ready" signal to the processor signifying that valid data is present on the peripheral port. This signal normally interrupts the processor, which then reads the data, causing generation of a "Data Taken" signal. The peripheral device responds by making new data available. This process continues until the data transfer is complete.

In the UM6522/A, automatic "Read" Handshaking is possible on the Peripheral A port only. The CA1 interrupt input pin accepts the "Data Ready" signal and CA2 generates the "Data Taken" signal. The "Data Ready" signal will set an internal flag which may interrupt the processor or which may be polled under program control. The "Data Taken" Signal can either be a pulse or a level which is set low by the system processor and is cleared by the "Data Ready" signal. These options are shown in Figure 12 which illustrates the normal Read Handshaking sequence.

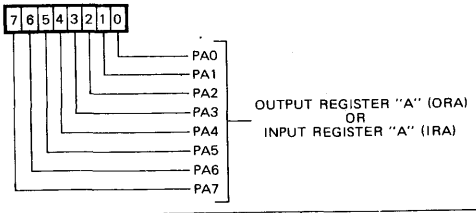
REG 0—ORB/IRB



Pin Data Direction Selection	Write	Read
DDRB="1" (OUTPUT)	MPU writes Output Level (ORB)	MPU reads output register but in ORB. Pin Level has no affect.
DDRB="0" (INPUT) (Input latching disabled)	MPU writes into ORB but no effect	MPU reads input level on PB Pin.
DDRB="0" (INPUT) (Input Latching enabled)	On Pin Level until DDRB changed	MPU reads IRB bit, which is the level of the PB pin at the time of the last CB1 active transition.

Figure 9. Output Register B (ORB), Input Register B (IRB)

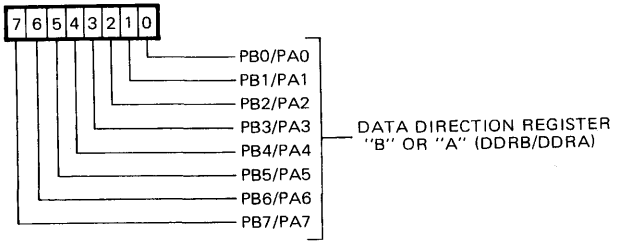
REG 1—ORA/IRA



Pin Data Direction Selection	Write	Read
DDRA="1" (OUTPUT) (Input latching disabled)	MPU writes Output Level (ORA)	MPU reads level on PA pin.
DDRA="1" (OUTPUT) (Input latching enabled)		MPU reads IRA bit which is the level of the PA pin at the time of the last CA1 active transition.
DDRA="0" (INPUT) (Input latching disabled)	MPU writes into ORA, but no effect on pin level, until DDRA changed.	MPU reads level on PA pin.
DDRA="0" (INPUT) (Input latching enabled)		MPU reads IRA bit which is the level of the PA pin at the time of the last CA1 active transition.

Figure 10. Output Register A (ORA), Input Register A (IRA)

REG 2 (DDRB) AND REG 3 (DDRA)



"0" ASSOCIATED PB/PA PIN IS AN INPUT (HIGH—IMPEDANCE)

"1" ASSOCIATED PB/PA PIN IS AN OUTPUT WHOSE LEVEL IS DETERMINED BY ORB/ORA REGISTER BIT

Figure 11. Data Direction Registers (DDRB, DDRA)

Write Handshake

The sequence of operations which allows handshaking data from the system processor to a peripheral device is very similar to that described for Read Handshaking. However, for Write Handshaking, the UM6522/A generates the "Data

Ready" signal and the peripheral device must respond with the "Data Taken" signal. This can be accomplished on both the PA port and the PB port on the UM6522/A. CA2 or CB2 act as a "Data Ready" output in either the handshake mode or pulse mode and CA1 or CB1 accept the "Data Taken" signal from the peripheral device, setting the interrupt flag and clearing the "Data Ready" output. This sequence is shown in Figure 13.

Selection of operating modes for CA1, CA2, CB1, and CB2 is accomplished by the Peripheral Control Register (Figure 14).

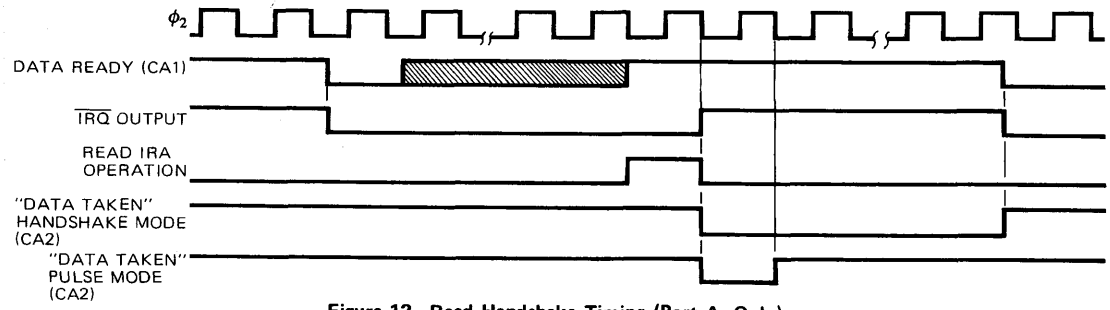


Figure 12. Read Handshake Timing (Port A, Only)

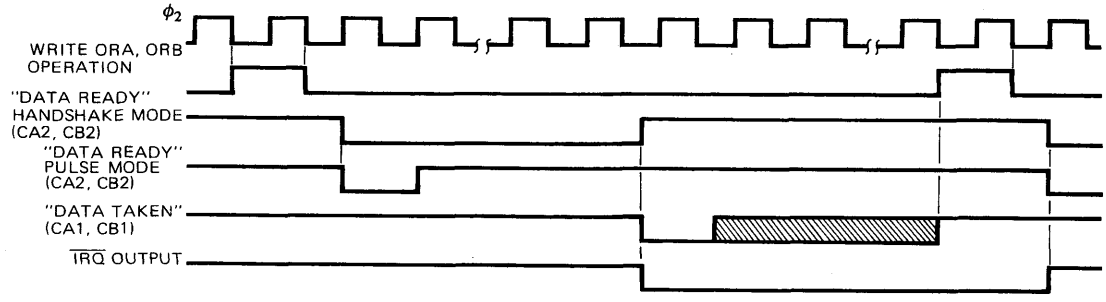


Figure 13. Write Handshake Timing

REG 12 – PERIPHERAL CONTROL REGISTER

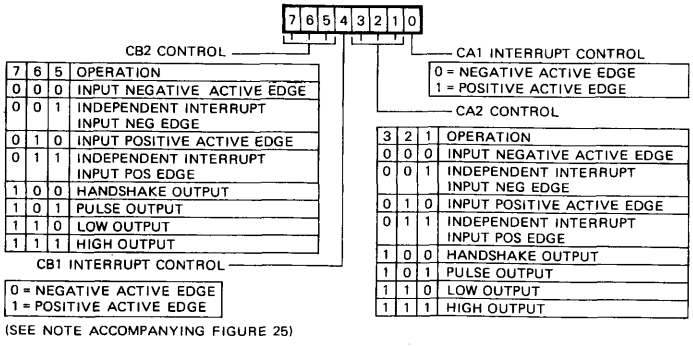


Figure 14. CA1, CA2, CB1, CB2 Control

Timer Operation

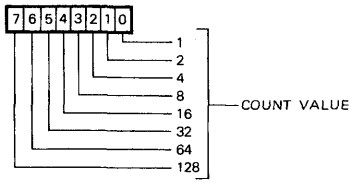
Interval Timer, T1, consists of two 8-Bit latches and a 16-bit decrement at the $\phi 2$ clock rate. Upon reaching "zero", an interrupt flag will be set, and IRQ will go low if the interrupt decrements at the $\phi 2$ clock rate. Upon reaching "zero" an interrupt flag will be set, and IRQ will go low if the interrupt is enabled. The timer will then disable any further interrupts, or (when programmed to) will automatically transfer the contents of the latches into the counter and begin to decrement again. In addition, the timer may be programmed to invert the output signal on a peripheral

pin each time it "times-out." Each of these modes is discussed separately below.

The T1 counter is depicted in Figure 15 and the latches in Figure 16.

Two bits are provided in the Auxiliary Control Register (bits 6 and 7) to allow selection of the T1 operating modes. The four possible modes are depicted in Figure 17.

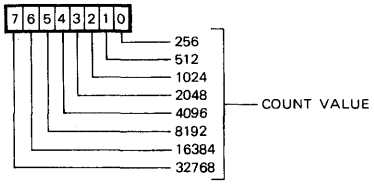
Reg 4 — Timer 1 Low-Order Counter



WRITE — 8 BITS ARE LOADED INTO T1 LOW-ORDER LATCHES. LATCH CONTENTS ARE TRANSFERRED INTO LOW ORDER COUNTER AT THE TIME THE HIGH ORDER COUNTER IS LOADED (REG. 5).

READ — 8 BITS FROM T1 LOW-ORDER COUNTER ARE TRANSFERRED TO MPU. IN ADDITION, T1 INTERRUPT FLAG IS RESET (BIT 6 IN INTERRUPT FLAG REGISTER).

Reg 5 — Timer 1 High-Order Counter

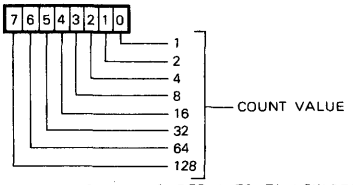


WRITE — 8 BITS LOADED INTO T1 HIGH-ORDER LATCHES. ALSO, AT THIS TIME BOTH HIGH AND LOW-ORDER LATCHES ARE TRANSFERRED INTO THE T1 COUNTER, AND INITIATES COUNTDOWN. T1 INTERRUPT FLAG IS ALSO RESET.

READ — 8 BITS FROM T1 HIGH-ORDER COUNTER TRANSFERRED TO MPU.

Figure 15. T1 Counter Registers

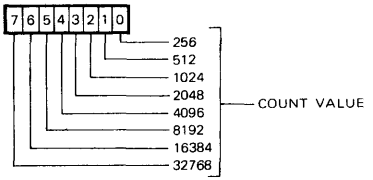
Reg 6 — Timer 1 Low-Order Latches



WRITE — 8 BITS ARE LOADED INTO T1 LOW-ORDER LATCHES. THIS OPERATION IS NO DIFFERENT FOLLOWING A WRITE INTO REG 4.

READ — 8 BITS FROM T1 LOW-ORDER LATCHES TRANSFERRED TO MPU. UNLIKE REG 4 OPERATION, THIS DOES NOT CAUSE RESET OF T1 INTERRUPT FLAG.

Reg 7 — Timer 1 High-Order Latches

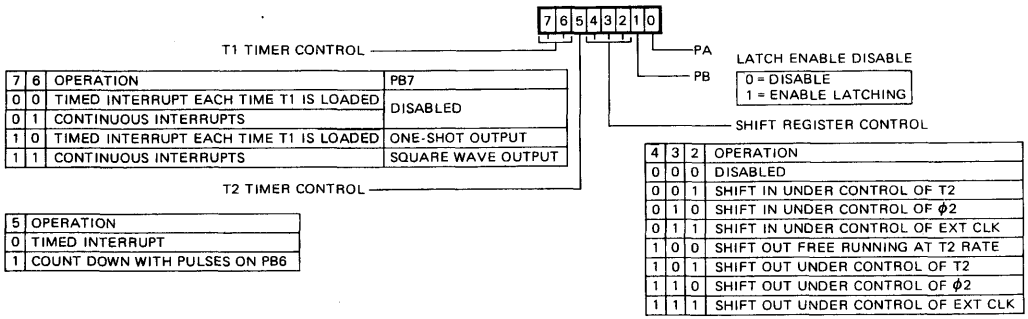


WRITE — 8 BITS LOADED INTO T1 HIGH-ORDER LATCHES. UNLIKE REG 4 OPERATION, NO LATCH-TO-COUNTER TRANSFERS TAKE PLACE.

READ — 8 BITS FROM T1 HIGH-ORDER LATCHES ARE TRANSFERRED TO MPU.

Figure 16. T1 Latch Registers

Reg 11 — Auxiliary Control Register



7	6	OPERATION	PB7
0	0	TIMED INTERRUPT EACH TIME T1 IS LOADED	DISABLED
0	1	CONTINUOUS INTERRUPTS	
1	0	TIMED INTERRUPT EACH TIME T1 IS LOADED	ONE-SHOT OUTPUT
1	1	CONTINUOUS INTERRUPTS	SQUARE WAVE OUTPUT

5	OPERATION
0	TIMED INTERRUPT
1	COUNT DOWN WITH PULSES ON PB6

4	3	2	OPERATION
0	0	0	DISABLED
0	0	1	SHIFT IN UNDER CONTROL OF T2
0	1	0	SHIFT IN UNDER CONTROL OF $\phi 2$
0	1	1	SHIFT IN UNDER CONTROL OF EXT CLK
1	0	0	SHIFT OUT FREE RUNNING AT T2 RATE
1	0	1	SHIFT OUT UNDER CONTROL OF T2
1	1	0	SHIFT OUT UNDER CONTROL OF $\phi 2$
1	1	1	SHIFT OUT UNDER CONTROL OF EXT CLK

Figure 17. Auxiliary Control Register

Note: The processor does not write directly to the low order counter (T1C-L). Instead, this half of the counter is loaded automatically from the low order latch when the processor writes to the high order counter. In fact, it may not be necessary to write to the low order counter in some applications since the timing operation is triggered by writing to the high order counter.

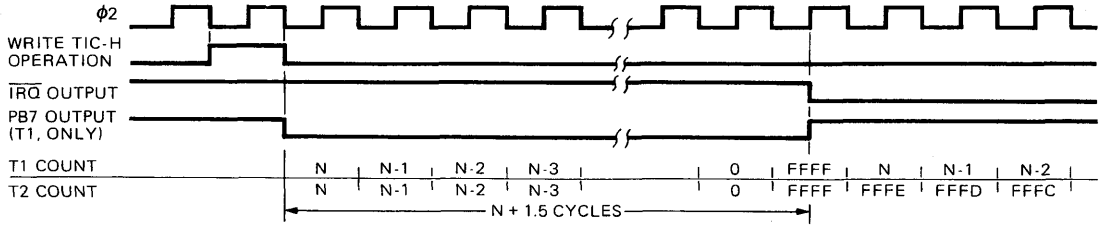


Figure 18. Timer 1 and Timer 2 One-Shot Mode Timing

Timer 1 One-Shot Mode

The interval timer one-shot mode allows generation of a single interrupt for each Timer load operation. In addition, Timer 1 can be programmed to produce a single negative pulse on PB7.

To generate a single interrupt ACR bits 6 and 7 must be "0", then either TIL-L or TIC-L must be written with the low-order count value. (A write to TIC-L is effectively a Write to TIL-L). Next, the high-order count value is written to TIC-H, (the value is simultaneously written into TIL-H), and TIL-L is transferred to TIC-L. Countdown begins on $\phi 2$ following the write TIC-H and decrements at the $\phi 2$ rate. T1 interrupt occurs when the counters reach "0". Generation of a negative pulse on PB7 is done in the same manner, except ACR bit 7 must be a one. PB7 will go low after a Write TIC-H and go high again when the counters reach "0".

The T1 interrupt flag is reset by either writing TIC-H (starting a new count) or by reading TIC-L.

Timing for the one-shot mode is illustrated in Figure 18.

Timer 1 Free-Run Mode

The most important advantage associated with the latches in T1 is the ability to produce a continuous series of evenly spaced interrupts and the ability to produce a square wave on PB7 whose frequency is not affected by variations in the processor interrupt response time. This is accomplished in the "free-running" mode.

In the free-running mode, the interrupt flag is set and the signal on PB7 is inverted each time the counter reaches zero. However, instead of continuing to decrement from zero after a time-out, the timer automatically transfers the contents of the latch into the counter (16 bits) and continues to decrement from there. It is not necessary to rewrite the timer to enable setting the interrupt flag on the next time-out. The interrupt flag can be cleared by reading TIC-L, by writing directly into the flag as will be described later, or if a new count value is desired by a write to TIC-H.

All interval timers in the UM6522/A are "re-triggerable". Rewriting the counter will always re-initialize the time-out period. In fact, the time-out can be prevented completely if the processor continues to rewrite the timer before it reaches zero. Timer 1 will operate in this manner if the processor writes into the high order counter (T1C-H). However, by loading the latches only, the processor can access the timer during each down-counting operation without affecting the time-out in process. Instead, the data loaded into the latches will determine the length of the next time-out period. This capability is particularly valuable in the free-running mode with the output enabled. In this mode, the signal on PB7 is inverted and the interrupt flag is set with each time-out. By responding to the interrupts with new data for the latches, the processor can determine the period of the next half cycle during each half cycle of the output signal on PB7. In this manner, very complex waveforms can be generated. Timing for the free-running mode is shown in Figure 19.

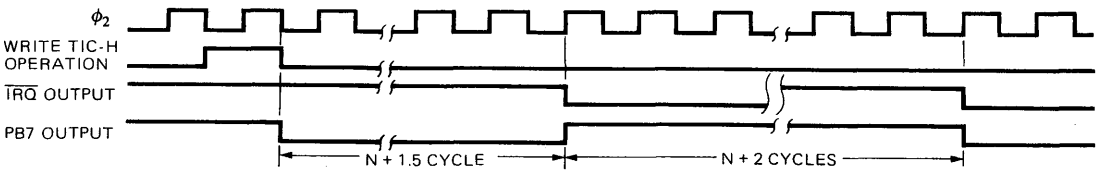


Figure 19. Timer 1 Free-Run Mode Timing

Note: A precaution to take when using PB7 as the timer output concerns the data direction Register contents for PB7. Both DDRB bit 7 and ACR bit 7 must be "1" for PB7 to function as the timer output. If either is a "0", then PB7 functions as a normal output pin, controlled by ORB bit 7.

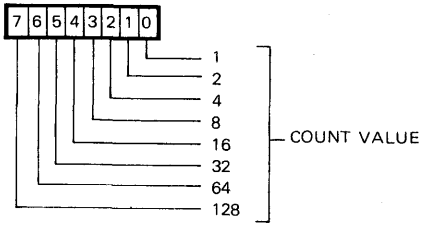
Timer 2 Operation

Timer 2 operates as an interval timer (in the "one-shot" mode only), or as a counter for counting negative pulses on the PB6 peripheral pin. A single control bit is provided in the Auxiliary Control Register to select between these two modes. This timer is comprised of a "write-only" low-order latch (T2L-L), a "read-only" low-order counter and a read/write high order counter. The counter registers act as a 16-bit counter which decrements at the $\phi 2$ rate. Figure 20 illustrates the T2 Counter Registers.

Timer 2 One-Shot Mode

As an interval timer, T2 operates in the "one-shot" mode similar to Timer 1. In this mode, T2 provides a single interrupt for each "write T2C-H" operation. After timing out, (reading 0) the counters "roll-over" to all 1's ($FFFF_{16}$) and continue decrementing, allowing the user to read them and determine how long T2 interrupt has been set. However, setting of the interrupt flag will be disabled after initial time-out so that it will not be set by the counter continuing to decrement through zero. The processor must rewrite T2C-H to enable setting of the interrupt flag. The interrupt flag is cleared by reading T2C-L or by writing T2C-H. Timing for this operation is shown in Figure 18.

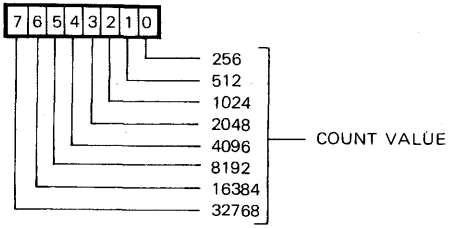
Reg 8 — Timer 2 Low-Order Counter



WRITE — 8 BITS LOADED INTO T2 LOW-ORDER LATCHES.

READ — 8 BITS FROM T2 LOW-ORDER COUNTER TRANSFERRED TO MPU. T2 INTERRUPT FLAG IS RESET.

Reg 9 — Timer 2 High-Order Counter



WRITE — 8 BITS LOADED INTO T2 HIGH-ORDER COUNTER. ALSO, LOW-ORDER LATCHES TRANSFERRED TO LOW-ORDER COUNTER, IN ADDITION, T2 INTERRUPT FLAG IS RESET.

READ — 8 BITS FROM T2 HIGH-ORDER COUNTER TRANSFERRED TO MPU.

Figure 20. T2 Counter Registers

Timer 2 Pulse Counting Mode

In the pulse counting mode, T2 serves primarily to count a predetermined number of negative-going pulses on PB6. This is accomplished by first loading a number into T2. Writing into T2C-H clears the interrupt flag and allows the counter to decrement each time a pulse is applied to PB6. The interrupt flag will be set when T2 reaches zero. At this time, the counter will continue to decrement with each pulse on PB6. However, it is necessary to rewrite T2C-H to allow the interrupt flag to be set on subsequent down-counting operations. Timing for this mode is shown in Figure 21. The pulse must be low on the leading edge of $\phi 2$.

Shift Register Operation

The Shift Register (SR) performs serial data transfer into and out of the CB2 pin under control of an internal modulo-8 counter. Shift pulses can be applied to the CB1 pin from an external source or, with the proper mode selection, shift pulses generated internally will appear on the CB1 pin for controlling external devices.

The control bits which select the various shift register operating modes are located in the Auxiliary Control Register. Figure 22 illustrates the configuration of the SR data bits and the SR control bits of the ACR.

Figures 23 and 24 illustrate the operation of the various shift register modes.

Interrupt Operation

Controlling interrupts within the UM6522/A involves three principal operations. These are flagging the interrupts, enabling interrupts and signaling to the processor that an active interrupt exists within the chip. Interrupt flags are set by interrupting conditions which exist within the chip or on inputs to the chip. These flags normally remain set until the interrupt has been serviced. To determine the source of an interrupt, the microprocessor must examine these flags in order from highest to lowest priority. This is accomplished by reading the flag register into the processor accumulator, shifting this register either right or left and then using conditional branch instructions to detect an active interrupt.

Associated with each interrupt flag is an interrupt enable bit. This can be set or cleared by the processor to enable interrupting the processor from the corresponding interrupt flag. If an interrupt flag is set to a logic "1" by an interrupting condition, and the corresponding interrupt enable bit is set to a "1", the Interrupt Request Output ($\overline{IRQ}$) will go low. $\overline{IRQ}$ is an "open-collector" output which can be wire-ORed to other devices in the system to interrupt the processor.

In the UM6522/A, all the interrupt flags are contained in one register. In addition, bit 7 of this register will be read as a logic "1" when an interrupt exists within the chip. This allows very convenient polling of several devices within a system to locate the source of an interrupt.

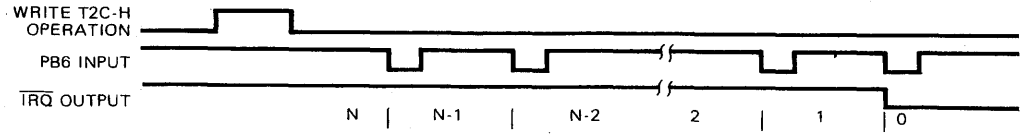
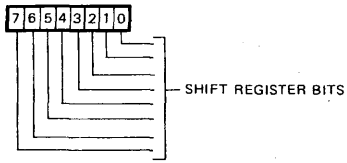


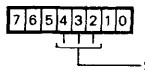
Figure 21. Timer 2 Pulse Counting Mode

Reg 10 — H Reg 10 — Shift Register



NOTES:
1. WHEN SHIFTING OUT, BIT 7 IS THE FIRST BIT OUT AND SIMULTANEOUSLY IS ROTATED BACK BIT 0 AND SHIFTED TOWARDS BIT 7.
2. WHEN SHIFTING IN, BITS INITIALLY ENTER BIT 0 AND ARE SHIFTED TOWARDS BIT 7.

Reg 11 — Auxiliary Control Register



4	3	2	OPERATION
0	0	0	DISABLED
0	0	1	SHIFT IN UNDER CONTROL OF T2
0	1	0	SHIFT IN UNDER CONTROL OF $\phi 2$
0	1	1	SHIFT IN UNDER CONTROL OF EXT CLK
1	0	0	SHIFT OUT FREE-RUNNING AT T2 RATE
1	0	1	SHIFT OUT UNDER CONTROL OF T2
1	1	0	SHIFT OUT UNDER CONTROL OF $\phi 2$
1	1	1	SHIFT OUT UNDER CONTROL OF EXT CLK

Figure 22. SR and ACR Control Bits

SR Disabled (000)

The 000 mode is used to disable the Shift Register. In this mode the microprocessor can write or read the SR, but the shifting operating is disabled and operation of CB1 and CB2 is controlled by the appropriate bits in the Peripheral Control Register (PCR). In this mode the SR Interrupt Flag is disabled (held to a logic "0").

Shift in Under Control of T2 (001)

In the 001 mode the shifting rate is controlled by the low order 8 bits of "T2". Shift pulses are generated on the CB1 Pin to control shifting in external devices. The time between transitions of this output clock is a function of the system clock period and the contents of the low order T2 latch (N).

The shifting operation is triggered by writing or reading the shift register. Data is shifted first into the low order bit of SR and is then shifted into the next higher order bit of the shift register on the negative-going edge of each clock pulse. The input data should change before the positive-going edge of the CB1 clock pulse. This data is shifted into the shift register during the $\phi 2$ clock cycle following the positive-going edge of the CB1 clock pulse. After 8 CB1 clock pulses, the shift register interrupt flag will be set and $\overline{IRQ}$ will go low.

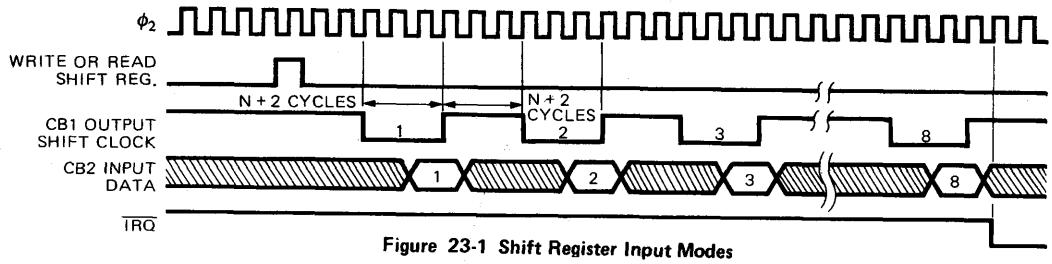


Figure 23-1 Shift Register Input Modes

Shift in Under Control of $\phi 2$ (010)

In mode 010 the shift rate is a direct function of the system clock frequency. CB1 becomes an output which generates shift pulses for controlling external devices. Timer 2 operates as an independent interval timer and has no effect on SR. The shifting operation is triggered by reading or writing the Shift Register. Data is shifted first into bit 0 and is then shifted into the next higher order bit of the shift register on the trailing edge of each $\phi 2$ clock pulse. After 8 clock pulses, the shift register interrupt flag will be set, and the output clock pulses on CB1 will stop.

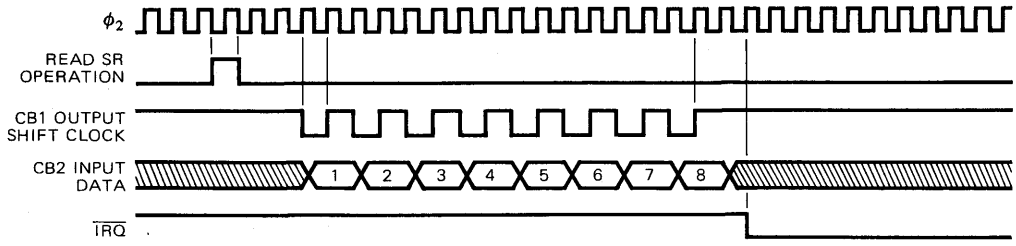


Figure 23-2 Shift Register Input Modes

Shift in Under Control of External CB1 Clock (011)

In mode 011 CB1 becomes an input. This allows an external device to load the shift register at its own pace. The shift register counter will interrupt the processor each time 8 bits have been shifted in. However, the shift register counter does not stop the shifting operation; it acts simply as a pulse counter. Reading or writing the Shift Register resets the Interrupt flag and initializes the SR counter to count another 8 pulses.

Note that the data is shifted during the first system clock cycle following the positive-going edge of the CB1 shift pulse. For this reason, data must be held stable during the first full cycle after CB1 goes high.

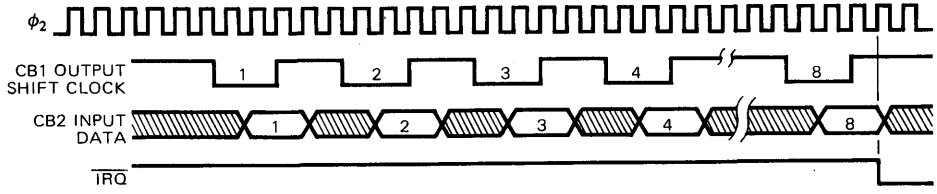


Figure 23-3 Shift Register Input Modes

Shift Out Free-Running at T2 Rate (100)

Mode 100 is very similar to mode 101 in which the shift rate is set by T2. However, in mode 100 the SR Counter does not stop the shift operation. Since Shift Register bit 7 (SR7) is circulated back into bit 0, the 8 bits loaded into the shift register will be clocked onto CR2 repeatedly. In this mode the shift register counter is disabled, and IRQ is never set.

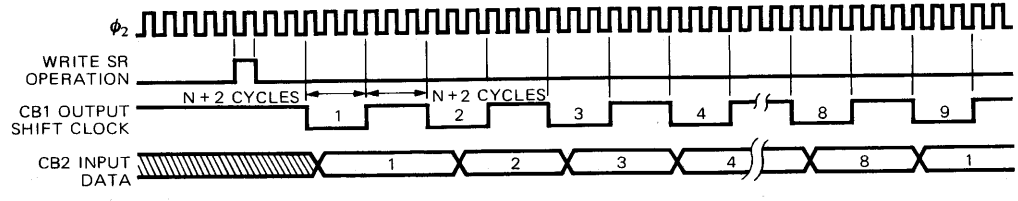


Figure 24-1 Shift Register Output Modes

Shift Out Under Control of T2 (101)

In mode 101 the shift rate is controlled by T2 (as in the previous mode). However, with each read or write of the shift register the SR Counter is reset and 8 bits are shifted onto CB2. At the same time, 8 shift pulses are generated on CB1 to control shifting in external devices. After the 8 shift pulses, shifting is disabled, the SR Interrupt Flag is set and CB2 remains at the last data level.

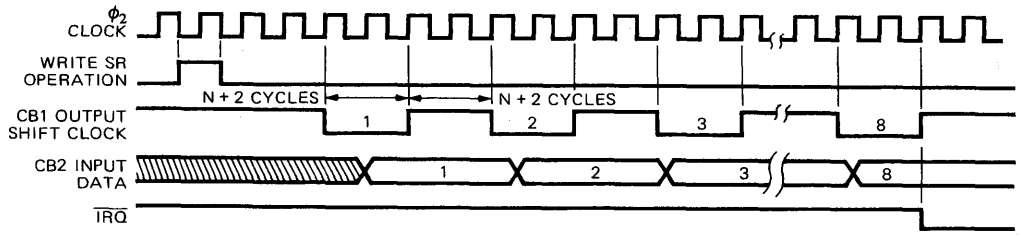


Figure 24-2 Shift Register Output Modes

Shift Out Under Control of $\phi 2$ (110)

In mode 110, the shift rate is controlled by the $\phi 2$ system clock.

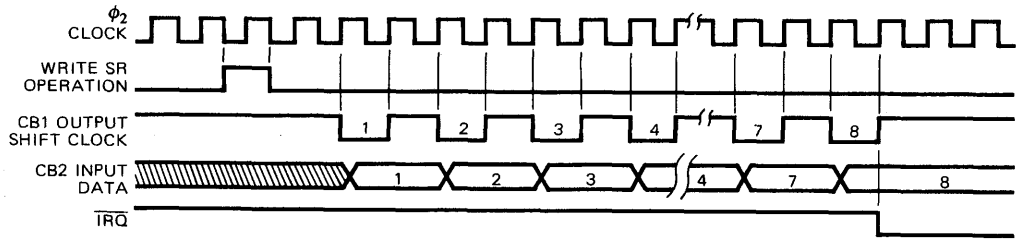


Figure 24-3 Shift Register Output Modes

Shift Out Under Control of External CB1 Clock (111)

In mode 111, shifting is controlled by pulses applied to the CB1 pin by an external device. The SR counter sets the SR Interrupt flag each time it counts 8 pulses but it does not disable the shifting function. Each time the microprocessor writes or reads the shift register, the SR Interrupt flag is reset and the SR counter is initialized to begin counting the next 8 shift pulses on pin CB1. After 8 shift pulses, the interrupt flag is set. The microprocessor can then load the shift register with the next byte of data.

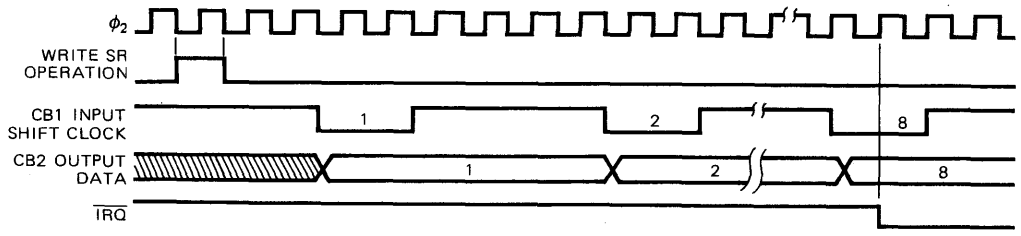


Figure 24-4 Shift Register Output Modes

The Interrupt Flag Register (IFR) and Interrupt Enable Register (IER) are depicted in Figures 25 and 26, respectively.

The IFR may be read directly by the processor. In addition, individual flag bits may be cleared by writing a "1" into the appropriate bit of the IFR. When the proper chip select and register signals are applied to the chip, the contents of this register are placed on the data bus. Bit 7 indicates the status of the IRQ output. This bit corresponds to the logic function: IRQ = IFR6 x IER6 + IFR5 x IER5 + IFR4 x IER4 + IFR3 x IER3 + IFR2 x IER2 + IFR1 x IER1 + IFR0 x IER0. Note: X = logic AND, + = Logic OR.

The IFR bit 7 is not a flag. Therefore, this bit is not directly cleared by writing a logic "1" into it. It can only be cleared by clearing all the flags in the register or by disabling all the active interrupts as discussed in the next section.

For each interrupt flag in IFR, there is a corresponding bit in the Interrupt Enable Register. The system processor can set or clear selected bits in this register to facilitate controlling individual interrupts without affecting others. This is accomplished by writing to address 1110 (IER address). If bit 7 of the data placed on the system data bus during this write operation is a "0", each "1" in bits 6 through 0 clears the corresponding bit in the Interrupt Enable Register. For each "zero" in bits 6 through 0, the corresponding bit is unaffected.

Setting selected bits in the Interrupt Enable Register is accomplished by writing to the same address with bit 7 in the data word set to a logic "1". In this case, each "1" in bits 6 through 0 will set the corresponding bit. For each "zero", the corresponding bit will be unaffected. The individual control of the setting and clearing operations allows very convenient control of the interrupts during system operation.

In addition to setting and clearing IER bits, the processor can read the contents of this register by placing the proper address on the register select and chip select inputs with the R/$\overline{W}$ line high. Bit 7 will be read as a logic "1".

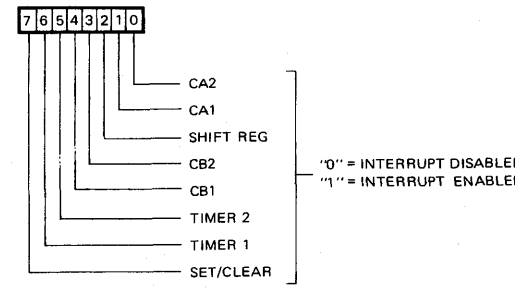
Reg 13 — Interrupt Flag Register

	SET BY	CLEARED BY
CA2	CA2 ACTIVE EDGE	READ OR WRITE REG 1 (ORA)*
CA1	CA1 ACTIVE EDGE	READ OR WRITE REG 1 (ORA)
SHIFT REG	COMPLETE 8 SHIFTS	READ OR WRITE SHIFT REG
CB2	CB2 ACTIVE EDGE	READ OR WRITE ORB*
CB1	CB1 ACTIVE EDGE	READ OR WRITE ORB
TIMER 2	TIME-OUT OF T2	READ T2 LOW OR WRITE T2 HIGH
TIMER 1	TIME-OUT OF T1	READ T1 LOW OR WRITE T1 HIGH
IRQ	ANY ENABLED INTERRUPT	CLEAR ALL INTERRUPTS

* IF THE CA2/CB2 CONTROL IN THE PCR IS SELECTED AS "INDEPENDENT" INTERRUPT INPUT, THEN READING OR WRITING THE OUTPUT REGISTER ORA/ORB WILL NOT CLEAR THE FLAG BIT. INSTEAD, THE BIT MUST BE CLEARED BY WRITING INTO THE IFR, AS DESCRIBED PREVIOUSLY.

Figure 25. Interrupt Flag Register (IFR)

Reg 14 — Interrupt Enable Register



Notes:
1. IF BIT 7 IS A "0", THEN EACH "1" IN BITS 0-6 DISABLES THE CORRESPONDING INTERRUPT.
2. IF BIT 7 IS A "1", THEN EACH "1" IN BITS 0-6 ENABLES THE CORRESPONDING INTERRUPT.
3. IF A READ OF THIS REGISTER IS DONE, BIT 7 WILL BE "1" AND ALL OTHER BITS WILL REFLECT THEIR ENABLE/DISABLE STATE.

Figure 26. Interrupt Enable Register (IER)

Ordering Information

Part Number	Frequency	Package
UM6522	1 MHz	40L DIP
UM6522A	2 MHz	40L DIP

UMC

UM6532/A

RAM, I/O, Timer Array

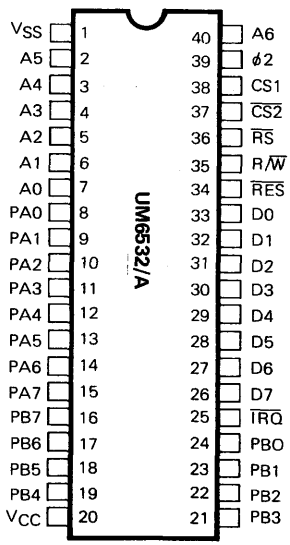
Features

- 8 bit bi-directional Data Bus for direct communication with the microprocessor
- Programmable edge-sensitive interrupt
- 128 x 8 static RAM
- Two 8 bit, bi-directional, data ports for interface to peripherals
- Two programmable I/O peripheral data direction registers
- Programmable interval-timer
- Programmable interval timer interrupt
- Peripheral pins with direct transistor drive capability
- High impedance, three-state, data pins

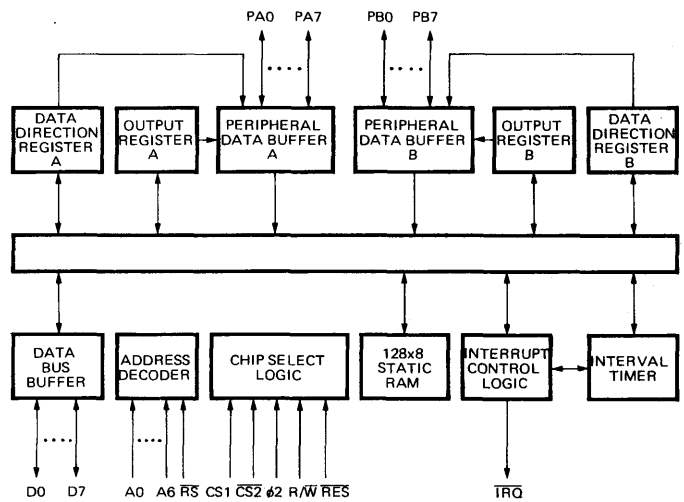
General Description

The UM6532/A is designed to operate in conjunction with the UM6500 Microprocessor Family. It is comprised of a 128 x 8-bit static RAM; two software controlled, 8-bit, bi-directional, data ports allowing direct interfacing between the microprocessor unit and peripheral devices; a software programmable interval timer with interrupt capable of timing in various intervals from 1 to 262,144 clock periods; and a programmable, edge-detect, interrupt circuit.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Supply Voltage . . . . . +8.0 Volts
Operating Voltage Range . . . . . +4V to +7V
Input Voltage, Applied . . . . . GND–2.0V to 6.5V
I/O Pin Voltage, Applied . . . . . GND–0.5V to V_{CC}+0.5V
Storage Temperature Range . . . . . –65°C to +150°C
Operating Temperature Range . . . . . 0°C to +70°C
Maximum Power Dissipation . . . . . 1 Watt

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

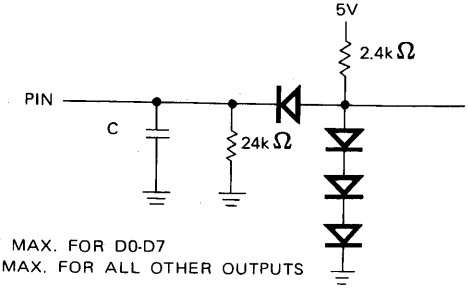
DC Characteristics

(V_{CC} = 5.0V ± 5%, V_{SS} = 0V, T_A = 0 – 70°C)

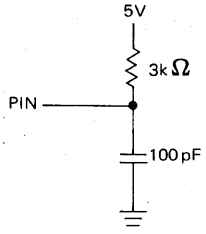
Parameter	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	2.4		V_{CC}	V
Input Low Voltage	V_{IL}	0.3		0.4	V
Input Leakage Current; V_{IN} = V_{SS}+ 5V A0-A6, $\overline{RS}$, R/W, $\overline{RES}$, ϕ2, CS1, $\overline{CS2}$	I_{IN}		1.0	2.5	μA
Input Leakage Current for High Impedance State (Three State); V_{IN} = 0.4V to 2.4V; D0-D7	I_{TSI}		±1.0	±10.0	μA
Input High Current; V_{IN} = 2.4V PA0-PA7, PB0-PB7	I_{IH}	–100	–300		μA
Output High Voltage V_{CC} = MIN, I_{LOAD} –100μA (PA0-PA7, PB0-PB7, D0-D7) I_{LOAD} 3MA (PB0-PB7)	V_{OH}	 2.4 1.5			V
Output Low Voltage V_{CC} = MIN, I_{LOAD} 1.6MA	V_{OL}			0.4	V
Output High Current (Sourcing); V_{OH} ⩾ 2.4V (PA0-PA7, PB0-PB7, D0-D7) ⩾ 1.5V Available for direct transistor drive (PB0-PB7)	I_{OH}	 –100 3.0	 –1000 5.0		 μA mA
Output Low Current (Sinking); V_{OL} ⩽ 0.4V	I_{OL}	1.6			mA
Clock Input Capacitance	C_{CIK}			30	pf
Input Capacitance	C_{IN}			10	pf
Output Capacitance	C_{OUT}			10	pf
Power Dissipation (V_{CC} = 5.25V)	P_D			680	mW

*All inputs contain protection circuitry to prevent damage due to high static charges. Care should be exercised to prevent unnecessary application of voltages outside the specification range.

Test Load

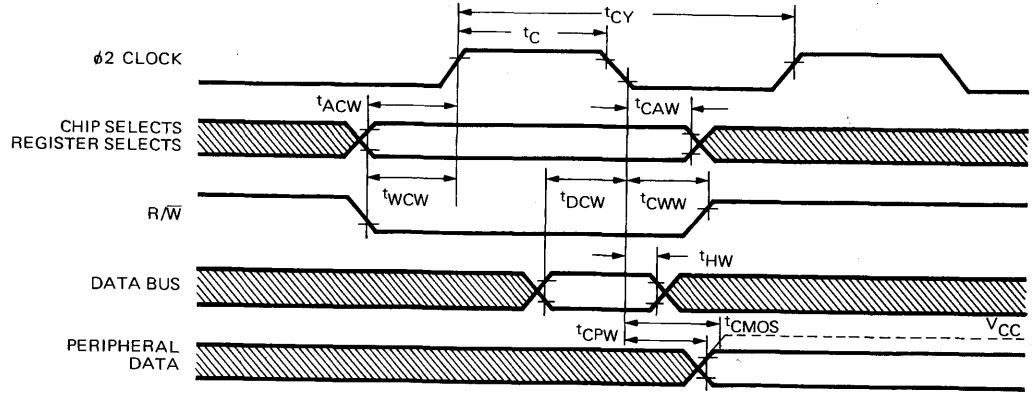


C = 130 pF MAX. FOR D0-D7
C = 30 pF MAX. FOR ALL OTHER OUTPUTS

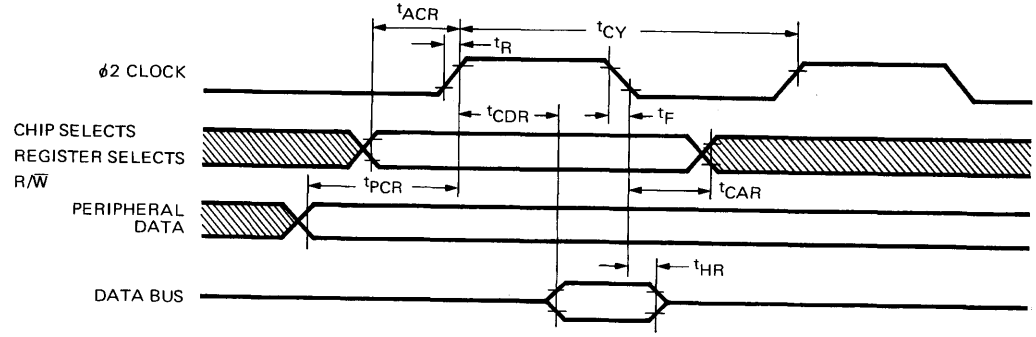


OPEN COLLECTOR
OUTPUT TEST LOAD

"Write" Timing Characteristics



"Read" Timing Characteristics



"Write" Timing Characteristics

Symbol	Parameter	UM6532		UM6532A		Unit
		Min.	Max.	Min.	Max.	
T_{CY}	Cycle Time	1	50	0.50	50	μs
T_C	ϕ2 Pulse Width	0.44	25	0.22	25	μs
T_{ACW}	Address Set-Up Time	180	–	90	–	ns
T_{CAW}	Address Hold Time	0	–	0	–	ns
T_{WCW}	R/W Set-Up Time	180	–	90	–	ns
T_{CWW}	R/W Hold Time	0	–	0	–	ns
T_{DCW}	Data Bus Set-Up Time	265	–	100	–	ns
T_{HW}	Data Bus Hold Time	10	–	10	–	ns
T_{CPW}	Peripheral Data Delay Time	–	1.0	–	1.0	μs
T_{CMOS}	Peripheral Data Delay Time to CMOS Levels	–	2.0	–	2.0	μs

Note: t_r , t_f = 10 to 30 ns.

"Read" Timing Characteristics

Symbol	Parameter	UM6532		UM6532A		Unit
		Min.	Max.	Min.	Max.	
T_{CY}	Cycle Time	1	50	0.5	50	μs
T_{ACR}	Address Set-Up Time	180	–	90	–	ns
T_{CAR}	Address Hold Time	0	–	0	–	ns
T_{PCR}	Peripheral Data Set-Up Time	300	–	300	–	ns
T_{CDR}	Data Bus Delay Time	–	340	–	200	ns
T_{HR}	Data Bus Hold Time	10	–	10	–	ns

Note: tr, tf = 10 to 30ns.

Interface Signal Description

Reset ($\overline{RES}$)

During system initialization a Logic "0" on the $\overline{RES}$ input will cause a zeroing of all four I/O registers. This in turn will cause all I/O buses to act as inputs, thus protecting external components from possible damage and erroneous data while the system is being configured under software control. The Data Bus Buffers are put into an "OFF" state during Reset. Interrupt capability is disabled with the $\overline{RES}$ signal. The $\overline{RES}$ signal must be held low for at least one clock period when reset is required.

Input Clock

The input clock is a system Phase Two clock which can be either a low level clock ($V_{IL}<0.4$, $V_{IH}>2.4$) or high level clock ($V_{IL}<0.2$, $V_{IH} = V_{CC}{}^{+0.3}_{-0.2}$).

Read/Write (R/$\overline{W}$)

The R/$\overline{W}$ signal is supplied by the microprocessor and is used to control the transfer of data to and from the UM6532/A. A high on the R/$\overline{W}$ pin allows the processor to read (with proper addressing) the UM6532/A. A low on the R/$\overline{W}$ pin allows a write (with proper addressing) to the UM6532/A.

Interrupt Request ($\overline{IRQ}$)

The $\overline{IRQ}$ output is derived from the interrupt control logic. It will normally be high, with a low indicating an interrupt from the UM6532/A. IRQ is an "open-drain" output, permitting several units to be wire-ORed to the common $\overline{IRQ}$ microprocessor input pin. The IRQ output may be activated by a transition on PA7 or "timeout" of the Interval Timer.

Data Bus (D0-D7)

The UM6532/A has eight, bi-directional, data lines (D0-D7). These lines connect to the system's data bus and allow transfer of data to and from the microprocessor. The output buffers remain in the "off" state, except when a Read operation occurs.

Peripheral Data Ports (PA0-PA7, PB0-PB7)

The UM6532/A has two 8-bit, peripheral, I/O Ports; Port A (lines PA0-PA7) and Port B (lines PB0-PB7). Each line is individually programmable as either an input or an output. By writing a "0" to any bit position of the Data Direction Register (DDRA or DDRB) the corresponding line will be programmed an an input. Likewise, by writing a "1" to any bit position in DDRA or DDRB will cause the corresponding line to act as an output.

When a Port line is programmed as an input, and its output register (ORA or ORB) is read by the MPU, the TTL level on the Port line will be transferred to the data bus. When the Port lines are programmed as outputs, the lines will reflect the data written by the MPU into the output registers. (See the Edge Sense Interrupt Section for an additional use of PA7.)

Address and Select Lines (A0-A6, $\overline{RS}$, CS1 and $\overline{CS2}$)

A0-A6 and $\overline{RS}$ are used to address the RAM, I/O registers, Timer and Flag register. CS1 and $\overline{CS2}$ are used to select (enable access to) the UM6532/A.

Internal Organization

A block diagram of the internal architecture is shown on Page 5-35. The UM6532/A is divided into four basic sections: RAM, I/O, Timer, and Interrupt Control. The RAM interfaces directly with the microprocessor through the system data bus and address lines. The I/O section consists of two 8-bit halves. Each half contains a Data Direction Register (DDR) and an I/O register.

RAM 128 Bytes (1024 Bits)

A 128 x 8-bit static RAM is contained on the UM6532/A. It is addressed by A0-A6 (Byte Select), RS, CS1, and CS2.

Internal Peripheral Registers

There are four 8-bit internal registers: two data direction registers and two output registers. The two data direction registers (A side and B side) control the direction of the data into and out of the peripheral I/O. A logic "zero" in a bit of the data direction register (DDRA and DDRB) causes the corresponding line of the I/O port to act as an input. A logic "one" causes the corresponding line to act as an output. The voltage on any line programmed as an output is determined by the corresponding bit in the output register (ORA and ORB).

Data is read directly from the PA lines during a peripheral read operation. For a PA pin programmed as an output, the data transferred into the processor will be the same as the data in the ORA, only if the voltage on the line is allowed to be $\geqslant$ 2.4 volts for a logic "one" and $\leqslant$0.4 volts for a "zero". If the loading on the line does not allow this, then the data resulting from the read operation may not match the contents of ORA.

The output buffers for the PB lines are somewhat different from the PA buffers. The PB buffers are push-pull devices which are capable of sourcing 3 mA at 1.5 volts. This allows these lines to directly drive transistor circuits. To assure that the processor will read the proper data when performing a peripheral read operation, logic is provided in the peripheral B port to permit the processor to read the contents of ORB, instead of the PB lines.

Interval Timer

The Timer section of the UM6532/A contains three basic parts: preliminary divide down register, programmable 8-bit register and interrupt logic. These are illustrated in Figure 1.

The Interval Timer can be programmed to count up to 256 time intervals. Each time interval can be either 1T, 8T, 64T, or 1024T increments, where T is the system clock period. When a full count is reached, the interrupt flag is set, to logic "1". After the interrupt flag is set, the internal clock continues counting down, but at a 1T rate to a maximum of 255T. This allows the user to read the counter and then determine how long the interrupt has been set.

The 8-bit system Data Bus is used to transfer data to and from the Interval Timer. If a total of 52 time intervals were to be counted, the pattern 0 0 1 1 0 1 0 0 would be put on the Data Bus and written into the Interval Time register.

At the same time that data is being written to the Interval Timer, the counting intervals of 1, 8, 64, and 1024T are decoded from address lines A0 and A1. During a Read or Write operation address line A3 controls the interrupt capability of $\overline{IRQ}$, i.e., A3 = "1" enables $\overline{IRQ}$, A3 = "0" disables $\overline{IRQ}$. In either case, when timeout occurs, bit 7 of the Interrupt Flag Register is set. This flag is cleared when the Timer register is either read from or written to by the processor. If $\overline{IRQ}$ is enabled by A3 and an interrupt occurs, $\overline{IRQ}$ will go low. When the Timer is read prior to the interrupt flag being set, the number of time intervals remaining will be read, i.e., 51, 50, 49, etc.

When the Timer has counted down to "0 0 0 0 0 0 0 0", an interrupt will occur on the next count time and the counter will read "1 1 1 1 1 1 1 1". After interrupt, the Timer register decrements at a divide by "1" rate of the system clock. If after interrupt, the Timer is read and a value of "1 1 1 0 0 1 0 0" is read, the time since interrupt is 28T. The value read is in two's complement.

Value read = 1 1 1 0 0 1 0 0
Complement = 0 0 0 1 1 0 1 1
Add 1 = 0 0 0 1 1 1 0 0 = 28.

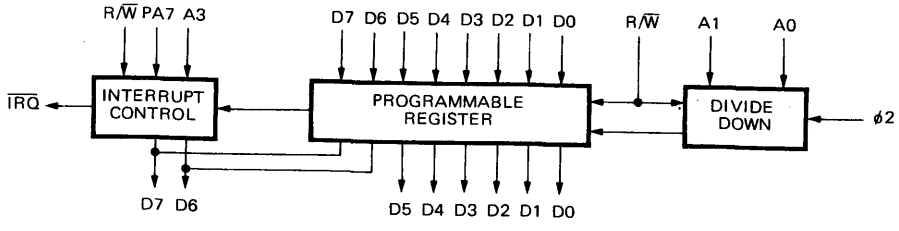


Figure 1. Basic Elements of Interval Timer

Thus, to arrive at the total elapsed time, merely do a two's complement and add "1" to the original time written into the Timer. Again, assume the time was written as "0 0 1 1 0 1 0 0" (= 52). With a divide by 8, total time to interrupt is (52 x 8) + 1 = 417T. Total elapsed time would be 416T + 28T = 444T, assuming the value read after interrupt was "1 1 1 0 0 1 0 0".

After an interrupt, whenever the Timer is written or read, the interrupt is reset. However, the reading of the Timer at the same time the interrupt occurs will not reset the interrupt flag.

Figure 2 illustrates an example of interrupt.

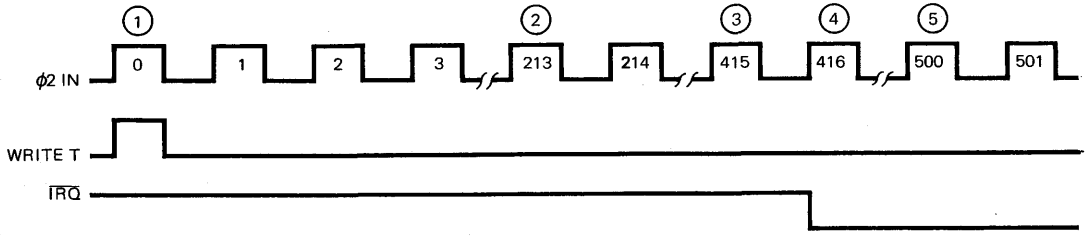


Figure 2. Timer Interrupt Timing

1. Data written into Interval Timers is "0 0 1 1 0 1 0 0" = 52_{10}
2. Data in Interval timer is "0 0 0 1 1 0 0 1" = 25_{10}

$$52 - \frac{231}{8} - 1 = 52 - 26 - 1 = 25$$

3. Data in Interval Timer is "0 0 0 0 0 0 0 0" = 0_{10}

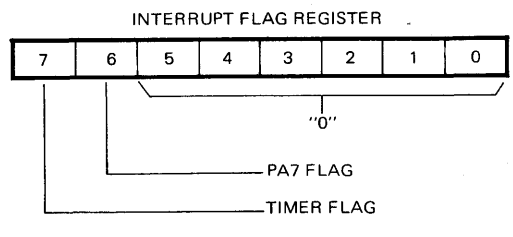
$$52 - \frac{415}{8} - 1 = 52 - 51 - 1 = 0$$

4. Interrupt has occurred at $\phi 2$ pulse #416
   Data in Interval Timer = "1 1 1 1 1 1 1 1"
5. Data in Interval Timer is "1 0 1 0 1 1 0 0"
   two's complement is "0 1 0 1 0 1 0 0" = 84_{10}
   $84 + (52 \times 8) = 500_{10}$

When reading the Timer after an interrupt, A3 should be low so as to disable the $\overline{IRQ}$ pin. This is done so as to avoid future interrupts until after another Write operation.

Interrupt Flag Register

The Interrupt Flag Register consists of two bits: the timer interrupt flag and the PA7 interrupt flag. When a read operation is performed on the Interrupt Flag Register, the bits are transferred to the processor on the data bus, as the diagram below indicates.



The PA7 flag is cleared when the Interrupt Flag Register is read. The timer flag is cleared when the timer register is either written or read.

Addressing

Addressing of the UM6532/A is accomplished by the 7 address inputs, the $\overline{RS}$ input and the two chip select inputs $\overline{CS1}$ and $\overline{CS2}$. To address the RAM, CS1 must be high with $\overline{CS2}$ and RS low. To address the I/O and Interval Timer, CS1 and $\overline{RS}$ must be high, with $\overline{CS2}$ low. As can be seen, to access the chip, CS1 is high and $\overline{CS2}$ is low. To distinguish between RAM or I/O-Timer Section, the $\overline{RS}$ input is used. When this input is low, the RAM is addressed; when high, the I/O Interval Timer section is addressed. To distinguish between Timer and I/O, address line A2 is utilized. When A2 is high, the Interval Timer is accessed. When A2 is low, the I/O section is addressed. Table 1 illustrates the chip addressing.

Edge Sense Interrupt

In addition to its use as a peripheral I/O line, PA7 can function as an edge sensing input. In this mode, an active transition on PA7 will set the internal interrupt flag (bit 6 of the Interrupt Flag Register). When this occurs, and providing the PA7 interrupt is enabled, the IRQ output will go low.

Control of the PA7 edge detecting logic is accomplished by performing a write operation to one of four addresses. The data lines for this operation are "don't care" and the addresses to be used are found in Table 1.

The setting of the internal interrupt flag by an active transition on PA7 is always enabled, whether PA7 is set up as an input or an output.

The $\overline{RES}$ signal disables the PA7 interrupt and sets the active transition to the "negative edge-detect" state. During the reset operation, the interrupt flag may be set by a negative transition. It may, therefore, be necessary to clear the flag before its normal use as an edge detecting input is enabled. This can be achieved by reading the Interrupt Flag Register.

I/O Register-Timer Addressing

Table 1 illustrates address decoding for the internal elements and timer programming. Address line A2 distinguishes I/O registers from the Timer. When A2 is low and $\overline{RS}$ is high, the I/O registers are addressed. Once the I/O registers are addressed, address lines A1 and A0 decode the desired register.

When the timer is selected A1 and A0 decode the "divide-by" matrix. This decoding is defined in Table 1. In addition, Address A3 is used to enable the interrupt flag to $\overline{IRQ}$.

Table 1. Addressing Decode

Functions	$\overline{RS}$	A6	A5	A4	A3	A2	A1	A0	WR	RD
RAM	L	X	X	X	X	X	X	X	✓	✓
ORA	H	–	–	–	–	L	L	L	✓	✓
DDRA	H	–	–	–	–	L	L	H	✓	✓
ORB	H	–	–	–	–	L	H	L	✓	✓
DDRB	H	–	–	–	–	L	H	H	✓	✓
Time, ÷1, IRQ ON	H	–	–	H	H	H	L	L	✓	
Timer, ÷8, IRQ ON	H	–	–	H	H	H	L	H	✓	
Timer, ÷64, IRQ ON	H	–	–	H	H	H	H	L	✓	
Timer, ÷1024, IRQ ON	H	–	–	H	H	H	H	H	✓	
Timer, ÷1, IRQ OFF	H	–	–	H	L	H	L	L	✓	
Timer, ÷8, IRQ OFF	H	–	–	H	L	H	L	H	✓	
Timer, ÷64, IRQ OFF	H	–	–	H	L	H	H	L	✓	
Timer, ÷1024, IRQ OFF	H	–	–	H	L	H	H	H	✓	
Read Timer, IRQ ON	H	–	–	–	H	H	–	L		✓
Read Timer, IRQ OFF	H	–	–	–	L	H	–	L		✓
Read Interrupt Flags	H	–	–	–	–	H	–	H		✓
RA7 IRQ OFF, NEG EDGE	H	–	–	L	–	H	L	L	*	
PA7 IRQ OFF, POS EDGE	H	–	–	L	–	H	L	H	*	
PA7 IRQ ON, NEG EDGE	H	–	–	L	–	H	H	L	*	
PA7 IRQ ON, POS EDGE	H	–	–	L	–	H	H	H	*	

Notes: "X" = Address, "–" = Address bits are "don't care", "*" = Data bits are "don't care"

Ordering Information

Part Number	Speed	Package
UM6532	1 MHz	40L DIP
UM6532A	2 MHz	40L DIP

UMC

UM6551

Asynchronous Communication Interface Adapter (ACIA)

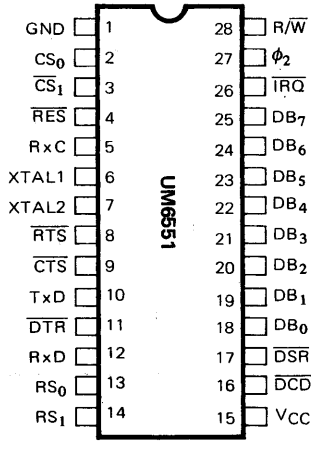
Features

- On-chip baud rate generator: 15 programmable baud rates derived from a standard 1.8432 MHz external crystal (50 to 19,200 baud)
- Programmable interrupt and status register to simplify software design
- Single +5 volt power supply
- Serial echo mode
- False start bit detection
- 8-bit, bi-directional data bus for direct communication with the microprocessor
- External 16x clock input for non-standard baud rates (up to 125k baud)
- Programmable: word lengths; number of stop bits; parity bit generation and detection
- Data set and modem control signals provided
- Parity: (odd, even, none, mark, space)
- Full-duplex or half-duplex operation
- 5, 6, 7, 8, and 9 bit transmission

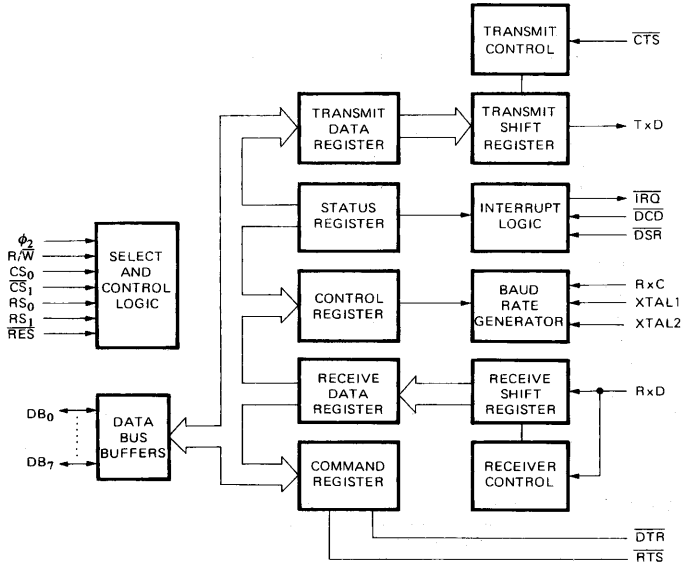
General Description

The UM6551 is an Asynchronous Communication Adapter (ACIA) intended for interfacing the 6500/6800 microprocessor families to serial communication data sets and modems. A unique feature is the inclusion of an on-chip programmable baud-rate generator, with a crystal being the only external component required.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Supply Voltage ..... −0.3V to +7.0V
Input/Output Voltage ..... −0.3V to +7.0V
Operating Temperature ..... 0°C to 70°C
Storage Temperature ..... −55°C to 150°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

(V_{CC} = 5.0V ± 5%, T_A = 0−70°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	2.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	−0.3	–	0.8	V
Input Leakage Current: V_{IN} = 0 to 5V ($\phi 2$, R/$\overline{W}$, $\overline{RES}$, CS_0, $\overline{CS_1}$, RS_0, RS_1, $\overline{CTS}$, RxD, $\overline{DCD}$, $\overline{DSR}$)	I_{IN}	–	±1.0	±2.5	μA
Input Leakage Current for High Impedance State (Three State)	I_{TSI}	–	±2.0	±10.0	μA
Output High Voltage: I_{LOAD} = −100μA (DB_0-DB_7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$)	V_{OH}	2.4	–	–	V
Output Low Voltage: I_{LOAD} = 1.6mA (DB_0-DB_7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$)	V_{OL}	–	–	0.4	V
Output High Current (Sourcing): V_{OH} = 2.4V (DB_0-DB_7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$)	I_{OH}	−100	–	–	μA
Output Low Current (Sinking): V_{OL} = 0.4V (DB_0-DB_7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$)	I_{OL}	1.6	–	–	mA
Output Leakage Current (Off State): V_{OUT} = 5V ($\overline{IRQ}$)	I_{OFF}	–	1.0	10.0	μA
Clock Capacitance ($\phi 2$)	C_{CLK}	–	–	20	pF
Input Capacitance (Except XTAL 1 and XTAL2)	C_{IN}	–	–	10	pF
Output Capacitance	C_{OUT}	–	–	10	pF
Power Dissipation (See Graph) (T_A = 0°C) V_{CC} = 5.25V	P_D	–	170	300	mW

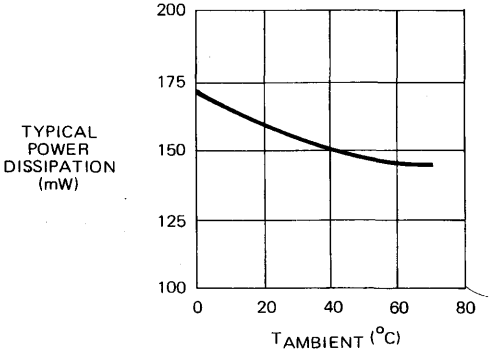


Figure 1. Power Dissipation vs. Temperature

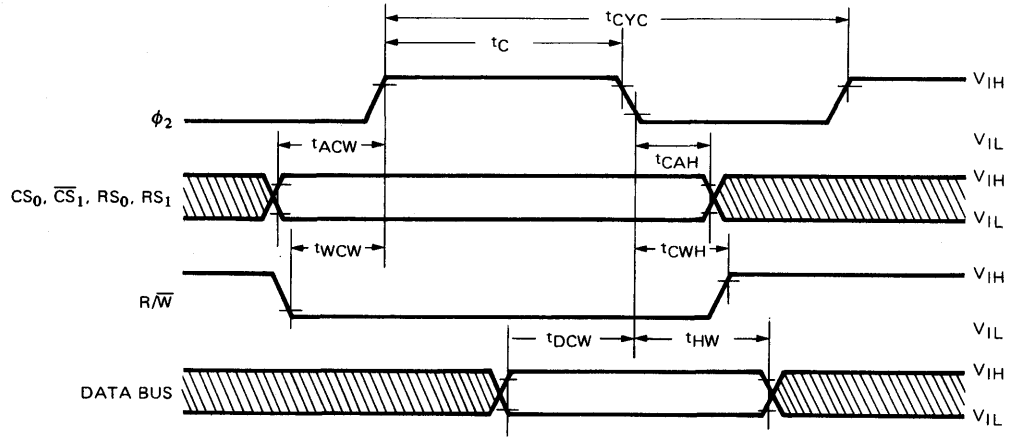


Figure 2. "Write" Timing Characteristics

Write Cycle

(V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)

Parameter	Symbol	UM6551		UM6551A		Unit
		Min.	Max.	Min.	Max.	
Cycle Time	t_{CYC}	1.0	–	0.5	–	μs
φ2 Pulse Width	t_C	400	–	200	–	ns
Address Set-Up Time	t_{ACW}	120	–	70	–	ns
Address Hold Time	t_{CAH}	0	–	0	–	ns
R/$\overline{W}$ Set-Up Time	t_{WCW}	120	–	70	–	ns
R/$\overline{W}$ Hold Time	t_{CWH}	0	–	0	–	ns
Data Bus Set-Up Time	t_{DCW}	150	–	60	–	ns
Data Bus Hold Time	t_{HW}	20	–	20	–	ns

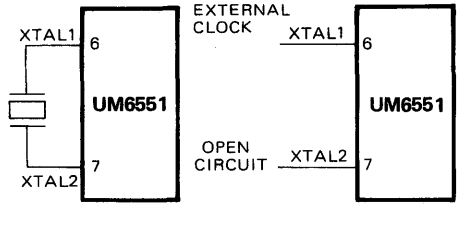
(t_r and t_f = 10 to 30 ns)

Crystal Specification

1. Temperature stability ± 0.01% (0° to 70°C)
2. Characteristics at 25°C ± 2°C
   a. Frequency (MHz) 1.8432
   b. Frequency tolerance (±%) 0.02
   c. Resonance mode Series
   d. Equivalent resistance (ohm) 400 max.
   e. Drive level mW 2
   f. Shunt capacitance pF 7 max.
   g. Oscillation mode Fundamental

No external components should be in the crystal circuit

Clock Generation



INTERNAL CLOCK EXTERNAL CLOCK

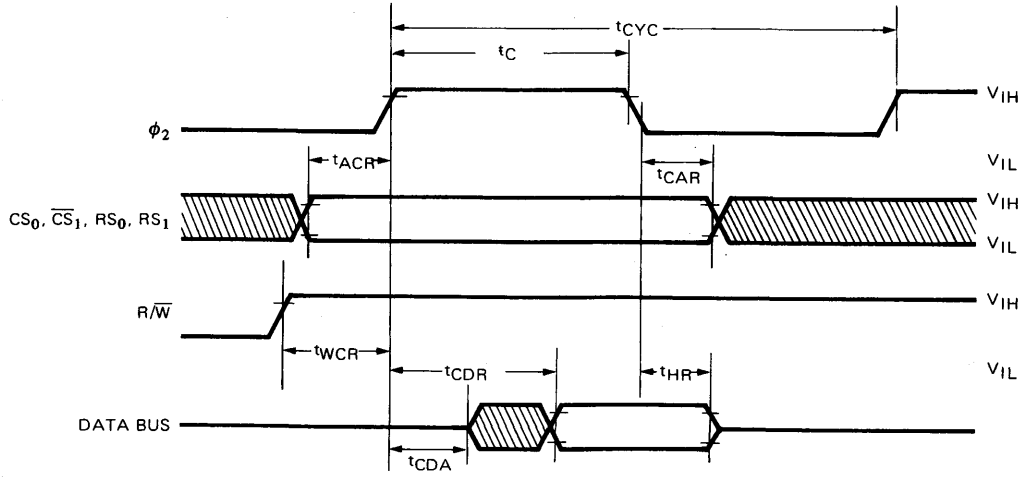


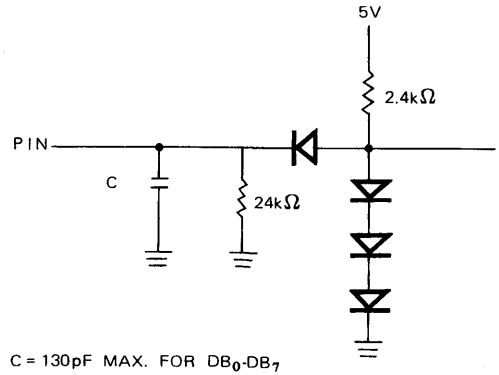
Figure 3. "Read" Timing Characteristics

Read Cycle

(V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)

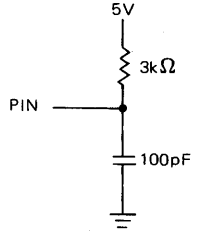
Parameter	Symbol	UM6551		UM6551A		Unit
		Min.	Max.	Min.	Max.	
Cycle Time	t_{CYC}	1.0	–	0.5	–	μs
Pulse Width (φ2)	t_C	400	–	200	–	ns
Address Set-Up Time	t_{ACR}	120	–	70	–	ns
Address Hold Time	t_{CAR}	0	–	0	–	ns
R/W Set-Up Time	t_{WCR}	120	–	70	–	ns
Read Access Time (Valid Data)	t_{CDR}	–	200	–	150	ns
Read Data Hold Time	t_{HR}	20	–	20	–	ns
Bus Active Time (Invalid Data)	t_{CDA}	40	–	40	–	ns

Test Load



C = 130pF MAX. FOR DB_0-DB_7
C = 30pF MAX. FOR ALL OTHER OUTPUTS

OPEN COLLECTOR
OUTPUT TEST LOAD



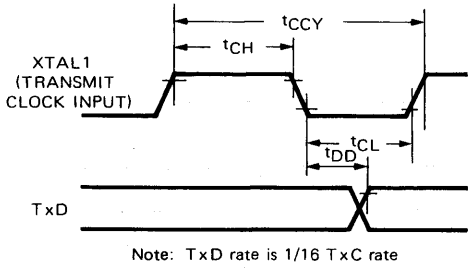


Figure 4a. "Transmit" Timing with External Clock

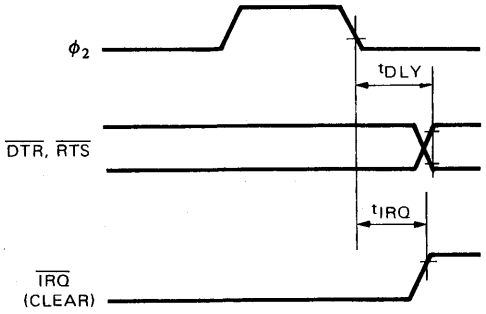


Figure 4b. "Interrupt" and "Output' Timing

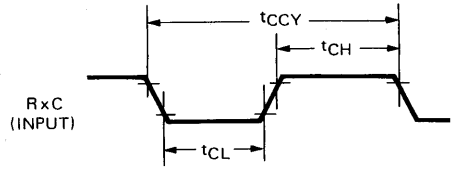


Figure 4c. "Receive" External Clock Timing

Transmit/Receive Characteristics

Parameter	Symbol	UM6551		UM6551A		Unit
		Min.	Max.	Min.	Max.	
Transmit/Receive Clock Rate	t_{CCY}	400*	–	400*	–	ns
Transmit/Receive Clock High Time	t_{CH}	175	–	175	–	ns
Transmit/Receive Clock Low Time	t_{CL}	175	–	175	–	ns
XTAL 1 to TxD Propagation Delay	t_{DD}	–	500	–	500	ns
Propagation Delay ($\overline{RTS}$, $\overline{DTR}$)	t_{DLY}	–	500	–	500	ns
$\overline{IRQ}$ Propagation Delay (Clear)	t_{IRQ}	–	500	–	500	ns

(t_r, t_f = 10 to 30 ns input clocks only)

* The baud rate with external clocking is: Baud Rate = $\frac{1}{16 \times T_{CCY}}$

Interface Signal Description

$\overline{RES}$ (Reset)

During system initialization, a low on the $\overline{RES}$ input will cause internal registers to be cleared.

$\phi 2$ (Input Clock)

The input clock is the system $\phi 2$ clock and is used to trigger all data transfer between the system microprocessor and the UM6551.

R/$\overline{W}$ (Read/Write)

The R/$\overline{W}$ is generated by the microprocessor and is used to control the direction of data transfer. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the UM6551. A low on the R/$\overline{W}$ pin allows a write to the UM6551.

$\overline{IRQ}$ (Interrupt Request)

The $\overline{IRQ}$ pin is an interrupt signal from the interrupt control logic. It is an "open drain" output, permitting several devices to be connected to the common $\overline{IRQ}$ microprocessor input. Normally a high level, $\overline{IRQ}$ goes low when an interrupt occurs.

DB_0-DB_7 (Date Bus)

The DB_0-DB_7 pins are the eight data lines used for transfer of data between the processor and the UM6551. These lines are bi-directional and are normally high-impedance, except during Read cycles, when selected.

CS_0, CS_1 (Chip Selects)

The two "chip select" inputs are normally connected to the processor address lines either directly or through decoders. The UM6551 is selected when CS_0 is high and $\overline{CS_1}$ is low.

RS_0, RS_1 (Register Selects)

The two "register select" lines are normally connected to the "processor address" lines to allow the processor to select the various UM6551 internal registers. The following table indicates the internal "register select" coding:

RS_1	RS_0	Write	Read
0	0	Transmit Data Register	Receiver Data Register
0	1	Programmed Reset (Data is "Don't Care")	Status Register
1	0	Command Register	
1	1	Control Register	

Register Select Coding

The table shows that only the "Command" and "Control" registers are read/write. The "Programmed Reset" operation does not cause a data transfer, but is used to clear the UM6551 registers. The Programmed Reset is slightly different from the Hardware Reset ($\overline{RES}$). These differences are described in the individual register definitions.

ACIA/Modem Interface Signal Description

XTAL1, XTAL2 (Crystal Pins)

These pins are normally directly connected to the external crystal (1.8432 MHz) used to derive the various baud rates. Alternatively, an externally generated clock may be used to drive the XTAL1 pin; in which case, the XTAL2 pin must "float".

TxD (Transmit Data)

The TxD output line is used to transfer serial NRZ (nonreturn-to-zero) data to the modem. The LSB (least significant bit) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected.

RxD (Receive Data)

The RxD input line is used to transfer serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is either the programmed baud rate or the rate of an externally generated receiver clock. This selection is made by programming the Control Register.

RxC (Receive Clock)

The RxC is a bi-directional pin which serves as either the receive 16x clock input or the receive 16x clock output. The latter mode results if the internal baud rate generator is selected for receive data clocking.

$\overline{RTS}$ (Request to Send)

The $\overline{RTS}$ output pin is used to control the modem from the processor. The state of the $\overline{RTS}$ pin is determined by the contents of the Command Register.

$\overline{CTS}$ (Clear to Send)

The $\overline{CTS}$ input pin is used to control the transmitter operation. The enable state is with $\overline{CTS}$ low. The transmitter is automatically disabled if $\overline{CTS}$ is high.

DTR (Data Terminal Ready)

This output pin is used to indicate the status of the UM6551 to the modem. A low on $\overline{DTR}$ indicates the UM6551 is enabled and a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

$\overline{DSR}$ (Data Set Ready)

The $\overline{DSR}$ input pin is used to indicate the status of the modem to the UM6551. A low indicates the "ready" state and a high, "not-ready". $\overline{DSR}$ is a high-impedance input and must not be a "no-connect". If unused, it should be driven high or low, but not switched.

Note: if Command Register Bit 0 = "1", and a change of state on $\overline{DSR}$ occurs, $\overline{IRQ}$ will be set, and Status Register Bit 6 will reflect the new level. The state of $\overline{DSR}$ does not affect either "Transmit" or "Receive" operations.

$\overline{DCD}$ (Data Carrier Detect)

The $\overline{DCD}$ input pin is used to indicate the status of the carrier detect output of the modem to the UM6551. A low indicates that the modem carrier signal is present and a high, that it is not. $\overline{DCD}$, like $\overline{DSR}$, is a high-impedance input and must not be a "no-connect".

Note: If Command Register Bit 0 = "1", and a change of state on $\overline{DCD}$ occurs, $\overline{IRQ}$ will be set, and Status Register Bit 5 will reflect the new level. The state of $\overline{DCD}$ does not affect "Transmit" operation, but must be low for the "Receive" to operate.

Internal Organization

The Transmitter/Receiver sections of the UM6551 are depicted by the block diagram in Figure 5.

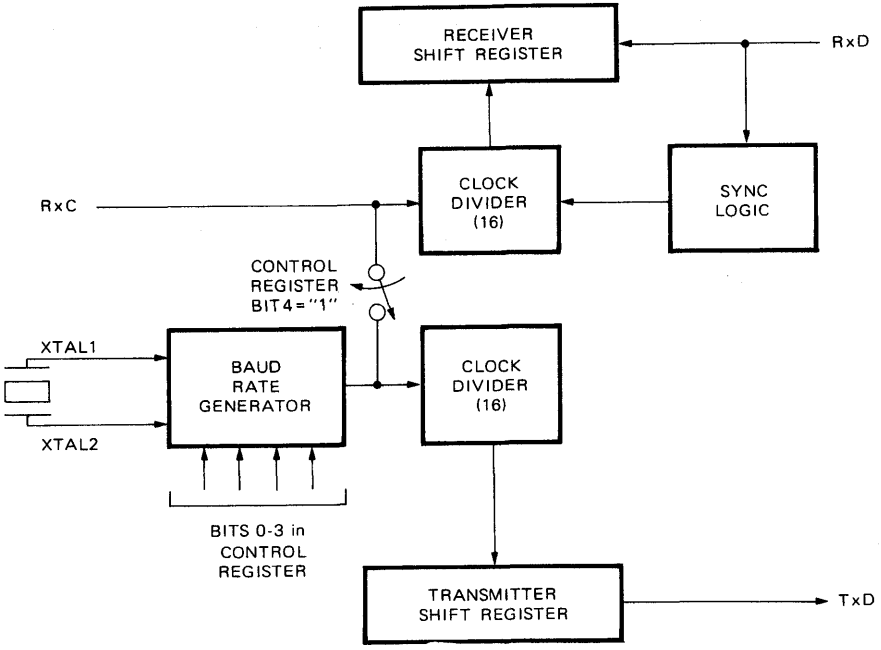


Figure 5. Transmitter/Receiver Clock Circuits

Bits 0-3 of the Control Register select the divisor used to generate the baud rate for the Transmitter. If the Receiver clock is to use the same baud rate as the Transmitter, then R x C becomes an output pin and can be used to slave other circuits to the UM6551.

Control Register

The Control Register is used to select the desired mode for the UM6551. The word length, number of stop bits, and clock controls are all determined by the Control Register, which is depicted in Figure 6.

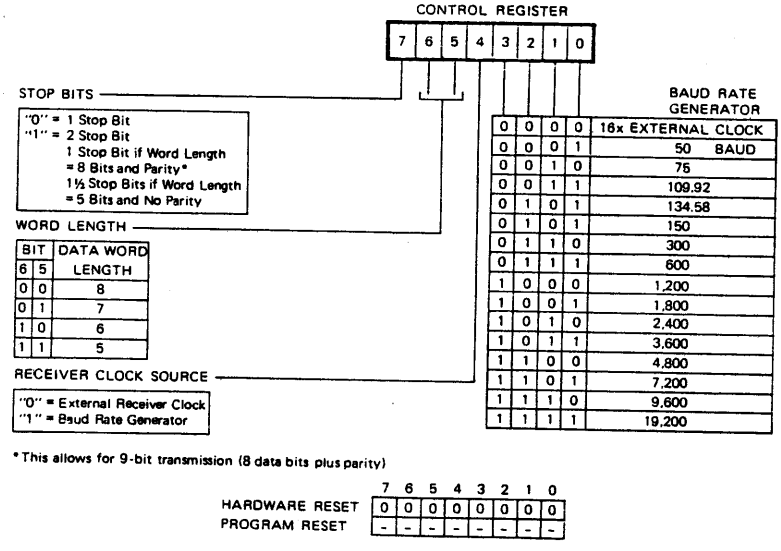


Figure 6. Control Register Format

Command Register

The Command Register is used to control Specific Transmit/Receive functions and is shown in Figure 7.

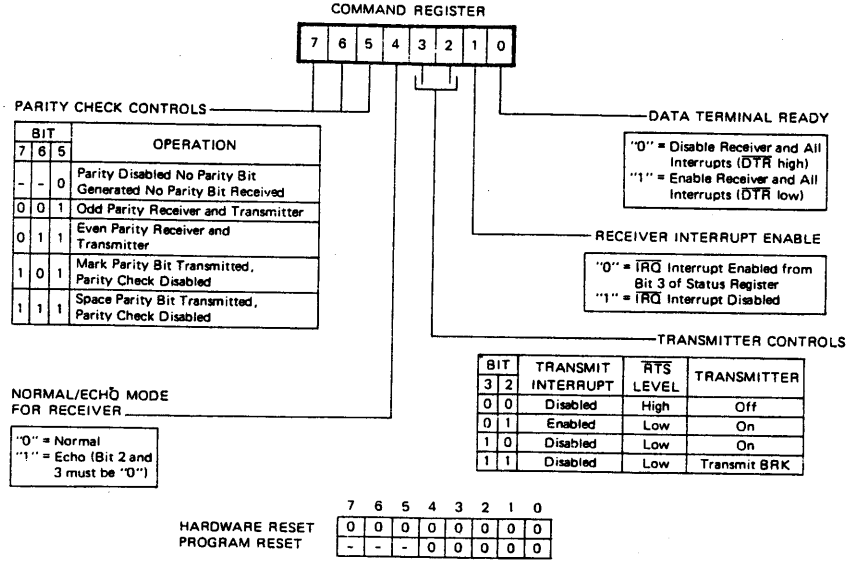
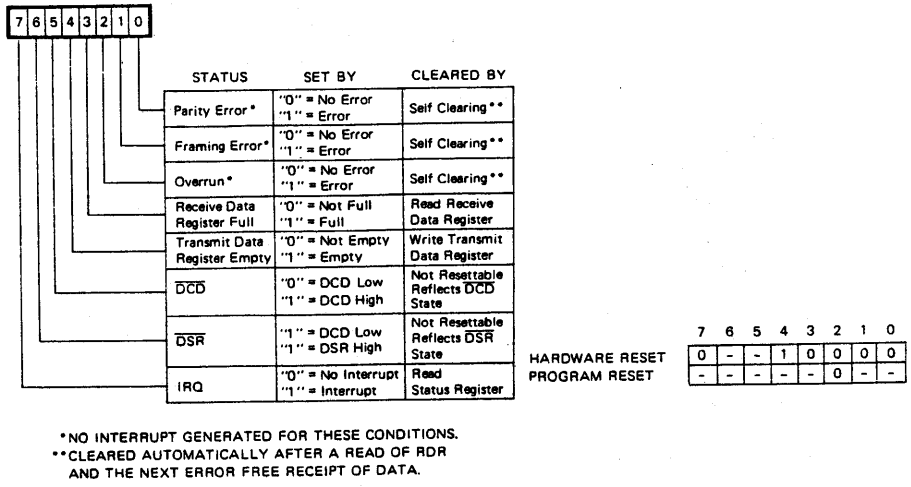


Figure 7. Command Register Format

Status Register

The Status Register is used to indicate to the processor the status of various UM6551 functions and is outlined in Figure 8.



*NO INTERRUPT GENERATED FOR THESE CONDITIONS.
**CLEARED AUTOMATICALLY AFTER A READ OF RDR AND THE NEXT ERROR FREE RECEIPT OF DATA.

Figure 8. Status Register Format

Transmit and Receive Data Registers

These registers are used as temporary data storage for the UM6551 Transmit and Receive circuits. The Transmit Data Register is characterized as follows:

- Bit 0 is the leading bit to be transmitted.
- Unused data bits are the high-order bits and are "don't care" for transmission.

The Receiver Data Register is characterized in a similar fashion:

- Bit 0 is the leading bit received.
- Unused data bits are the high-order bits and are "0" for the receiver.
- Parity bits are not contained in the Receive Data Register, but are stripped-off after being used for external parity checking. Parity and all unused high-order bits are "0".

Figure 9 illustrates a single transmitted or received data word, for the example of 8 data bits, parity, and 1 stop bit.

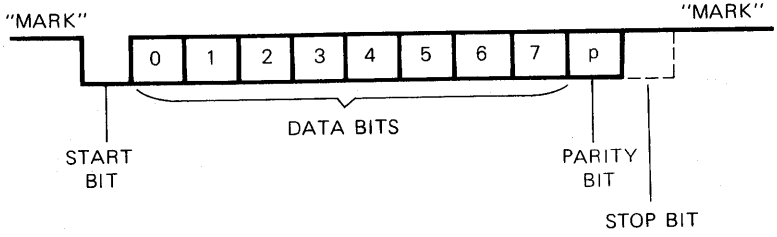


Figure 9. Serial Data Stream Example

Ordering Information

Part Number	Clock Rate	Package
UM6551	1 MHz	28L DIP
UM6551A	2 MHz	28L DIP

UMC

UM82C01

Capacitance Keyboard Encoder (CKE)

Features

- 16x8 matrix, can build up to 128 key capacitance keyboard
- Single chip with 16 scan drive outputs and 8 sense inputs
- Two packages 28 pin for 88 key KB and 40 pin for 128 key KB
- Keyboard scanning and encoding under complete control of the user's computer, especially 8048 microcomputer
- Single 5V supply
- High-speed CMOS technology
- Serve as easy interface to 8048
- New CMOS sense technology, CMOS analog sense circuit is built in
- Byte wide sense, higher performance than serial sense technology
- Wide frequency range, 1MHz to 11 MHz 8048 can be used

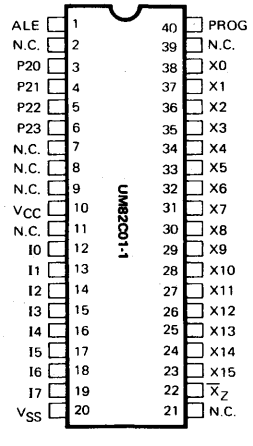
General Description

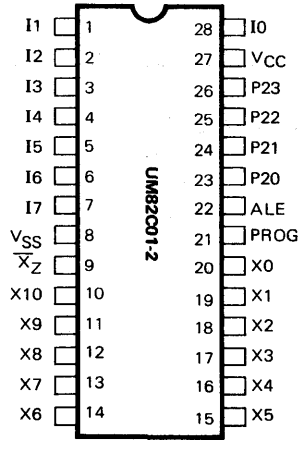
UM82C01 is a CMOS LSI, which offers interface between microcomputer and capacitive keyboard matrix. 40 pin UM82C01-1 is capable of scanning up to 128 low cost capacitive keys. 28 pin UM82C01-2 serves keyboard applications with less than 88 keys.

The keyboard scan is under complete control of the 8048 series microcomputer writing to expand I/O port. Port 2 data is multiplexed to initiate one of the scan lines. Sense circuit will receive the scan signal through capacitive keys if one key is pressed. Sense circuit includes CMOS analog and digital circuits which senses action by following amplifying and latching of analog signals from capacitive switches, these 8 data bits are then divided and latched making two nibbles. Two instructions can read these two nibbles from port 2. Then the microcomputer can analyze them and generate the scan code.

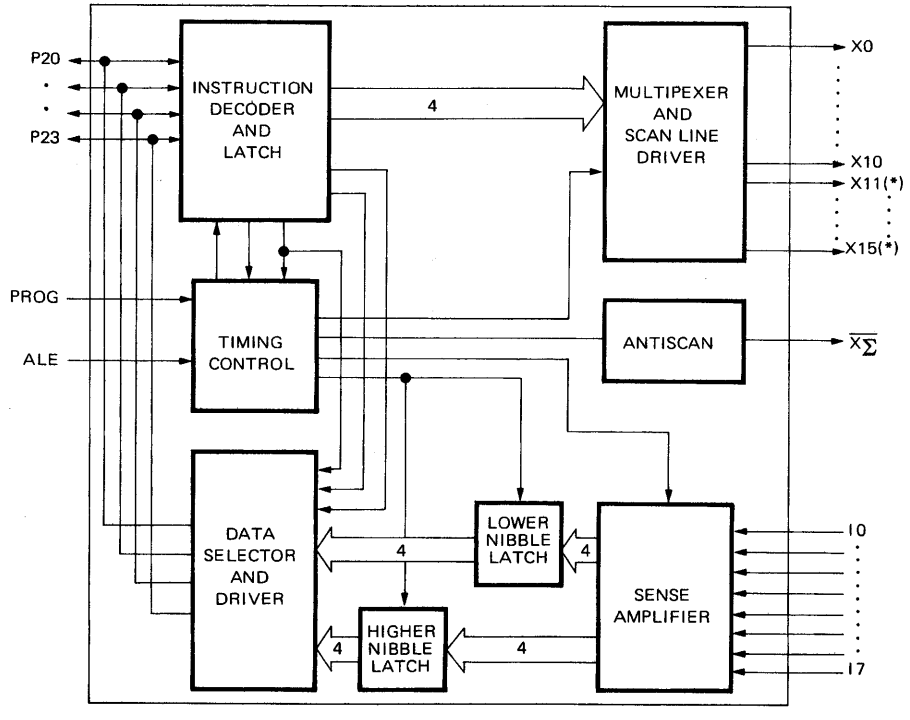
Antiscan is used to enhance the simple capacitive switches that are usually used in capacitive keyboards, offering switching threshold in sense input. This provides the keyboard with mechanical hysteresis which is built into the more expensive hall-effect and reed switches.

Pin Configurations





Block Diagram



(*) Only in UM82C01-1

Absolute Maximum Ratings *

Operating Temperature	0° to 70°C
Storage Temperature	−55° to 150°C
Power Supply	Max. 7V
Voltage on Any Pin	V_{SS} −0.7V to V_{CC} +0.7V

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

(Operating Voltage 5V ± 10%)

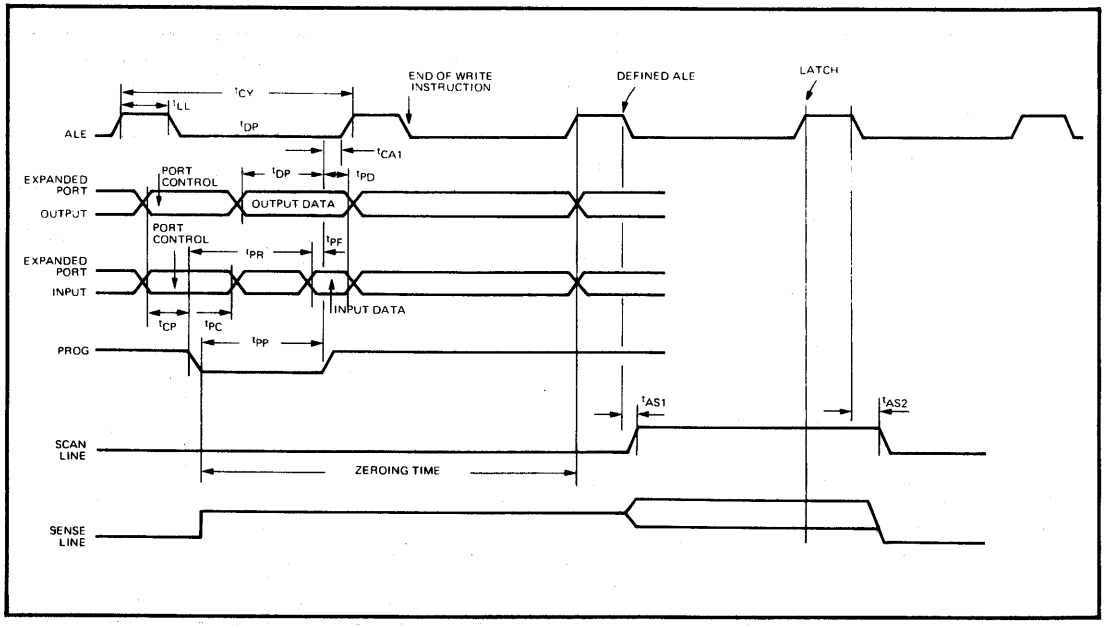
Item	Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Digital	Input Low Voltage	V_{IL}	−0.5		0.8	V	
	Input High Voltage	V_{IH}	2.0		V_{CC}	V	
	Output Low Voltage, I/O Port	V_{OLP}			0.45	V	I_{OL} = 5 mA
	Output High Voltage, I/O Port	V_{CHP}	V_{CC}-0.45		V_{CC}	V	I_{OH} = −400μA
	Output Low Voltage, Scan Line	V_{OLS}			0.45	V	I_{OL} = 5 mA
	Output High Voltage, Scan Line	V_{OHS}	V_{CC}-0.45		V_{CC}	V	I_{OH} = −5 mA
Analog	Input High to Reference	ΔV_H	0.1		1.8	V	Lying on Voltage Reference V_{REF}
	Input Low to Reference	ΔV_L	−0.1		−1.8	V	
Operating Current		I_{CC}			15	mA	
Stand by Power Supply Current		I_{SB}			200	μA	No sensing and Scanning

AC Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	UM82C01						Unit	Conditions
		4 MHz			11 MHz				
		Min.	Typ.	Max.	Min.	Typ.	Max.		
Address Latch Width	t_{LL}	700			150			ns	
Cycle Time	t_{CY}	3.75			1.36			μs	
Port Control Setup to PROG	t_{CP}	420			100			ns	
Port Control Hold to PROG	t_{PC}	800			160			ns	
Port Output Data Setup	t_{DP}	1350			400			ns	
Port Data Hold from PROG	t_{PD}	320			90			ns	
PROG Strobe to ALE	t_{CAI}	210			50			ns	
PROG Pulse Width	t_{PP}	2370			700			ns	
PROG to Port 2 Input Valid	t_{PR}			2130			700	ns	
Input Data Hold from PROG	t_{PF}			380			140	ns	
ALE to SCAN Setup	t_{AS_1}			200			100	ns	
ALE to SCAN Ended	t_{AS_2}			200			100	ns	

Timing Diagram



Pin Description

Symbol	Designation	I/O	Description
P20-P23	I/O Port	I/O	This four-bit bidirectional port contains the address and control bits from 8048 μC on a high to low transition of PROG. During a low to high transition of the PROG signal, the port contains the selected scan data for UM82C01 if the last command is a write operation. The sense nibble data from UM82C01 is latched during the low to high transition if the last command is a read operation. There exists a state flow in two continuous read operations which is called "read cycle". Upper nibble coming from sense inputs I4 to I7 is transferred in P20 to P23 from UM82C01 during low to high transition of PROG of MOVD A, P5 instruction, and lower nibble coming from I0 to I3 is transferred in P20 to P23 during low to high transition of PROG of MOVD A, P4 instruction.
ALE	Address Latch Enable Strobe	I	This pin comes direct from 8048 ALE. It is used as the time base as well as address latch strobe. Our target is to let 8048 work between 1 MHz to 11 MHz, so ALE varies from 66.6 KHz to 733.3 KHz. General PC key boards use 4 to 5 MHz 8048, hence, ALE is typically a 266.6 KHz strobe signal for a 4 MHz 8048. When ALE first goes from low to high in a write cycle, the PROG is activated and goes to low and at this time, Port 2 containing port address and write instruction codes is valid and should be latched by UM82C01 to initiate the scan mode.

Pin Description (Continued)

Symbol	Designation	I/O	Description
ALE	Address Latch Enable Strobe	I	UM82C01 begins Zeroing stage of its sense amplifier at this instant. PROG will go to high before second ALE of this write instruction. The Zeroing stage ends at the next ALE low to high transient. Timing Diagram, shows that this edge triggers the selected scan line to be active. The second ALE, which is next to end write instruction, is used to control scan line to inactive and its active transient is the high to low edge. In read cycle, when first ALE goes from high to low, PROG is activated to go to low, port 2 containing port address and read instruction code is valid and should be latched by UM82C01 to initiate the read mode.
PROG	Control Strobe	I	An active low strobe comes direct from 8048 PROG. 8048, PROG is a control strobe to expanded I/O. UM82C01 is designed to locate expanded port 4 and port 5 in 8048. Every time PROG is activated, UM82C01 is initiated in either write or read mode. When PROG goes inactive in a write cycle, selected scan data is valid in port 2 and is latched by UM82C01 to encode the scan line. In a read cycle, latched upper and lower nibbles are valid circularly in port 2 at every PROG low to high transition.
X0-X15	Scan Line Out	O	These are the 16 full range drive outputs. One of the lines is activated in a write cycle. Selected scan data is latched and used to decode these sixteen scan lines so the scanning is fully programmable by 8048. The selected scan line is activated in the defined ALE rising edge and ended in the next ALE falling edge. (Reference to Timing Diagram). The defined ALE is the first ALE after the write instruction is finished. There are eleven scan lines for 28 pin UM82C01-2, X11 to X15 and are included in scan line driver for 40 pin UM82C01-1.
$\overline{X}_Z$	Antiscan Out	O	This is the antiscan output. This output is activated whenever no scanning occurs, and is deactivated when any one of X0 to X15 is activated. Antiscan is used to reduce the voltage in sense input when there is no scanning which prevents logic error.
I0-I7	Sense Line Input	I	These eight lines are inputs from capacitance keyboard matrix. The small current pulses caused by the scan lines and pressed keyswitches are detected here.
V_{CC}	Power Supply	I	Connected to +5V power supply.
V_{SS}	Ground	I	Normally connected to +0V ground.

Application Description

The Microprocessor

The capacitance keyboard encoder (CKE) UM82C01 is designed to serve as an interface to 8048 series 8-bit microprocessors. The user can control the keyboard function easily through programming of microprocessor, which includes scanning reading and serves as an interface to host computer.

The Keyboard

A keyboard is an aray of switches. The array consists of a two dimensional matrix. One side of the matrix (X-lines) is used to drive the array with a microprocessor chosen signal, while the other side (I-Lines) is connected to sense circuits. In traditional configuration, users make use of mechanical contact switches. With a new sensing mechanism, capacitive switches present a good solution.

The Capacitive Switch

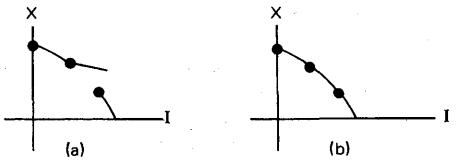


Figure 1. Mechanical Switch (a) Key off (b) Key on

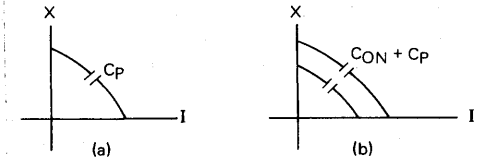
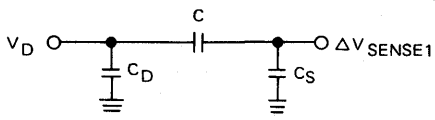


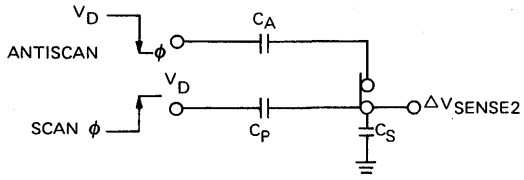
Figure 2. Capacitive Switch (a) Key off (b) key on

Fig. 1 shows the traditional mechanical switch, (a) When the key switch is off, X-lines and I-lines are open to each other, (b) When the key switch is on, X-lines and I-lines short together. Fig. 2, shows the capacitive switch, (a) The key switch is off; only a small parasitic capacitance exists between X-lines and I-lines (b) The key switch is on, a Con + Cp appears between X-lines and I-lines.



$$\Delta V_{SENSE1} = V_D \cdot \frac{\frac{1}{C_S}}{\frac{1}{C_S} + \frac{1}{C}} = V_D \cdot \frac{C}{C_S + C}$$

Figure 3a. Equivalent circuit for Capacitive Key



$$\Delta V_{SENSE2} = V_D \frac{C_P}{C_S + C_P + C_A} - V_D \frac{C_A}{C_S + C_P + C_A}$$

Figure 3b. Equivalent circuit for Capacitive Key with Antiscan Consideration

In Fig. 3a, an equivalent circuit for a capacitive key is shown. The voltage ΔV_{SENSE1} is decided by the scanning voltage V_D, capacitance C and C_S.

In Fig. 3b, an antiscanning consideration is presented. The scanning trigger edge is taking place with the inverse voltage "antiscan". After this edge, the voltage ΔV_{SENSE2} is decided by the voltage divided by C_P minus the voltage divided by C_A.

Writing

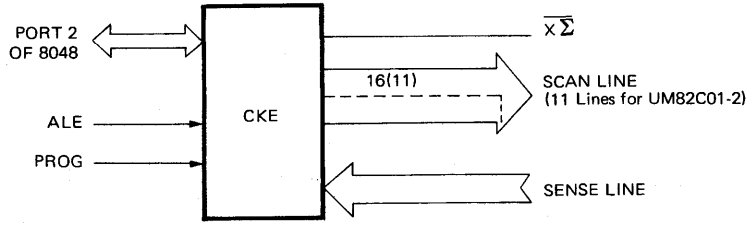


Figure 4. Logic Symbol of the CKE

In system configuration, the CKE is designed to stand in the expanded I/O port of 8048 microcomputer. The CKE uses the PORT 2, ALE and PROG to serve as an interface to the microprocessor. When 8048 writes a scan code to CKE, the CKE must be accessed through the expanded PORT 4. When 8048 reads the sensing code from the CKE, the CKE must be accessed through the expanded PORTS 4 and 5. PORTS 6 and 7 are reserved for the user.

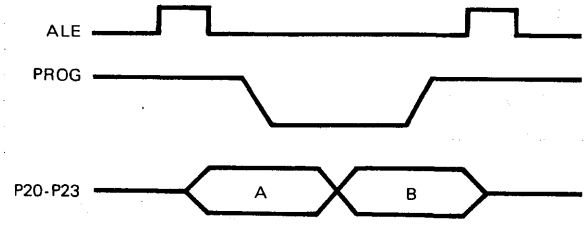


Figure 5. PROG Timing of 8048 I/P PORT Expansion

Address	P21	P20	PORT	Definitions
	0	0	PORT 4	Writing Port
	0	1	PORT 5	(Same as PORT 4)
	1	0	PORT 6	
	1	1	PORT 7	
Instruction	**P23**	**P22**	**Instruction**	**Definitions**
	0	0	READ	
	0	1	WRITE	Writing Instruction
	1	0	OR	
	1	1	AND	

Figure 6. Expanded Port Definition in Writing Cycle

By using PORT 4 (PORT 5 the same) of 8048 series microcomputer, the user can write his scanning data to the CKE chip. After the writing, two NOP instructions should be used to permit correct decoding and scanning. The timing diagram is shown in Fig. 7.

For example, if the user wants to scan X_1-line, the recommended Assembly is as listed:

Label	Command	Arguments	Comments
	⋮		
SCAN1:	MOV	A, #ϕ1H	; #ϕ1H Can Vary From ; #ϕϕH To #ϕFH
	MOVD	P4, A	
	NOP		; Wait Until CKE Starts
	NOP		; Scanning.
	⋮		

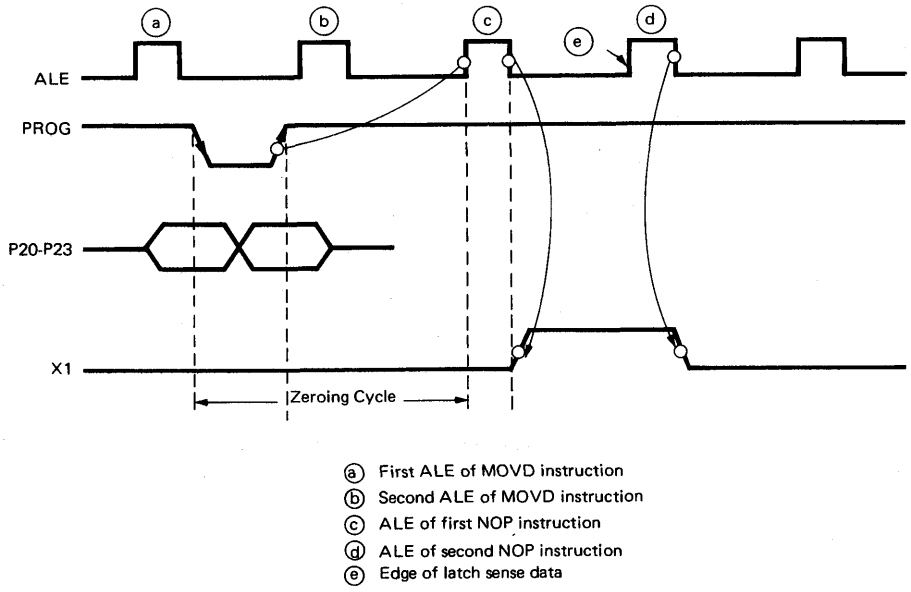


Figure 7. Timing Diagram of Writing and Scanning

Scanning

The CKE latches port address and instruction at the PROG high to low edge in Fig. 7, then enters the writing mode. At the PROG low to high edge, the CKE latches the data in P20–P23 which is now defined as the expanded PORT 4, and decodes the data to select the programmed scan line. Although the decoding and selection does not take much time, the scan line does not activate immediately.

From the PROG falling edge to the rising edge of the ALE, to the MOVD instruction in Fig. 7, the Sense Amplifier of CKE is "Zeroing". After the zeroing cycle, all the sense inputs are balanced at the reference voltage, and the selected scan line is activated at the falling edge of this ALE.

The scanning lines X_0 to X_{15} can each be decoded from the hexadecimal data programmed in PORT 4 at the writing cycle.

The scanning cycle equals an ALE cycle, so the scanning closes at the ALE falling edge of second NOP instruction as shown in Fig. 7. Before the end of scanning, Sense Amplifier will latch the sense data; These will be discussed in the Sensing section.

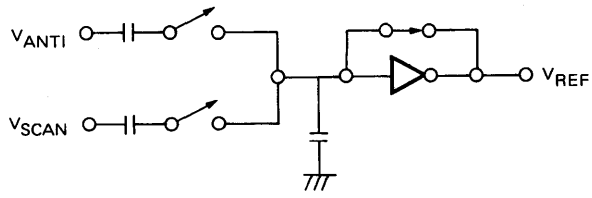
Antiscan

Antiscan line X_Σ is low whenever any scanning is activated, and is high when all scan lines X_0 to X_{15} are low.

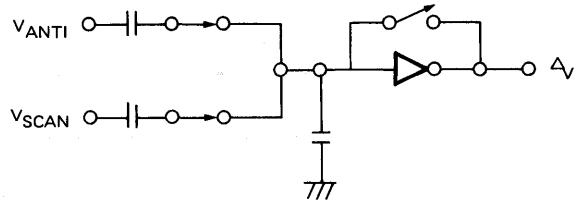
If no key is pressed, the antiscan will generate a $-\Delta V$ to the reference voltage, so that the Sense Amplifier will sense a voltage lower than reference voltage and latch a denoted low after amplification. If any key is pressed and the key is scanned, the voltage divided by the on capacitance will be a $+\Delta V$, so that the Sense Amplifier will sense a voltage higher than reference and latch a logic high after amplification.

The effect on whether antiscanning is larger than scanning depends on whether the key is pressed or not A new CMOS sense technology called "Sense Amplifier" is built in the CKE. In Fig. 8, we show the zeroing and sensing of this technology. In zeroing cycle, the switch between the input and output of the inverter is closed, so the sense input pad equals the reference voltage. After zeroing cycle, the shorting switch at the inverting stage is opened and sensing circuit is activated. In Fig. 7, we can see scanning also starts after zeroing. In fact, sensing is there writing for scanning. During the scanning cycle,

Sensing



(a) Zeroing



(b) Sensing

Fig. 8. Zeroing and Sensing

the CKE will latch the sensing input at the edge in Fig. 7.

The CKE uses byte-wide sensing, and has 8-bit latches. After latching, the data is separated into two nibbles, Higher Nibble and Lower Nibble, and stored.

Reading

Because the CKE serves as an interface to 8048 microcomputer by expanded PORT, the data must be 4-bits wide. Whenever there is data in the latches, the user can read the sensing data in nibble form. The CKE is designed to stand at PORT 4 and PORT 5 in the reading cycle.

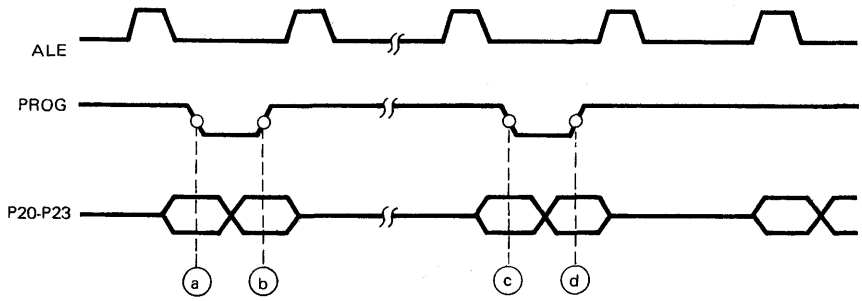
Address	P21	P20	PORT	Definitions
	0	0	PORT 4	Reading Lower Nibble
	0	1	PORT 5	Reading Higher Nibble
	1	0	PORT 6	Not used
	1	1	PORT 7	Not Used

Instruction	P23	P22	Instruction	Definitions
	0	0	Read	Reading Instruction
	0	1	Write	
	1	0	Or	
	1	1	And	

The latched data can be read by 8048 in two read instructions, these two instructions need not but can be continuous, and higher nibble is defined to be read from PORT 5, lower nibble from PORT 4. Users must pay attention for if no reading is instructed before the next writing, UM82C01 will reject the writing instruction until the reading instruction has been executed.

The recommended reading Assembly is as listed and the timing diagram is shown in Fig. 10.

Label	Command	Arguments	Comments
	⋮		
Read 1:	MOVD	A, P5	; Read Higher Nibble
	SWAP	A	
	MOV	Rn, A	
Read 2:	MOVD	A, P4	; Read Lower Nibble and
	ORL	A, Rn	; Combine Nibbles to Byte
	⋮		



(a) Port address and instruction of READ 1

(b) High nibble output from CKE

(c) Port address and instruction of READ 2

(d) Lower nibble output from CKE

Figure 10. Port Timing of Reading

After the reading cycle, the microcomputer can use the read data to generate scan code or key code easily.

Application Note

UM82C01 is a new solution for capacitance keyboard. The application therefore differs from the present capacitance Con and P. C. board parasitic capacitance Cp of general capacitance keyboards and consideration should be given to design them in. Con and Cp are listed in Table 1. C_S, C_A and C_{BS} are listed in Table 2. Table 3 (a) and (b) are recommendations for capacitance selection.

Table 1. Definition of Con and C_p

Name	Symbol	Min.	Typ.	Max.	Unit
Key on Capacitance	C_{ON}	8	20		pf
P.C.B. Parasitic Capacitance	C_P		1	3	pf

Table 2. Definition of C_S, C_A and C_{BS}

Name	Symbol	Min.	Typ.	Max.	Unit
Shunt Capacitance	C_S		80	150	pf
Antiscan Capacitance	C_A	4		8	pf
Capacitance between two senses	C_{BS}			5	pf

Table 3. Recommended Application of C_A for various C_{ON}

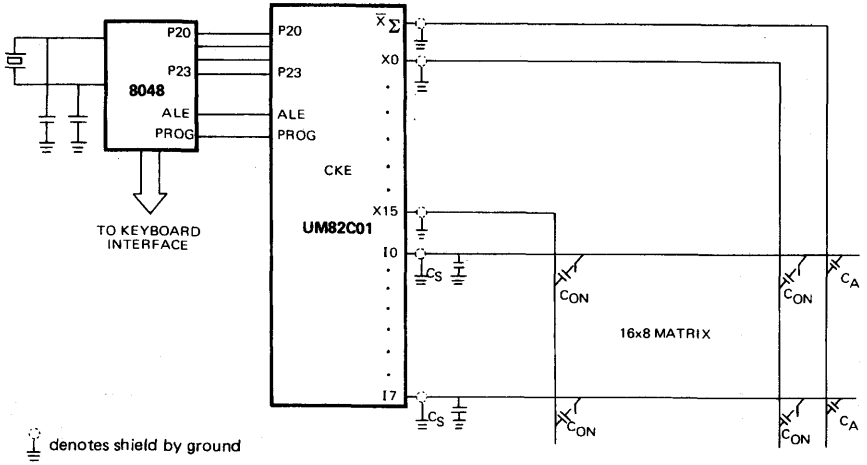
Symbol	Range		Unit
	Lower	Upper	
C_{ON}	10	25	pf
C_A	4	8	pf
C_P	0	3	pf

(a)

Symbol	Range		Unit
	Lower	Upper	
C_{ON}	25	35	pf
C_A	8	15	pf
C_P	0	3	pf

(b)

Typical Application



Ordering Information

Part Number	KB Type	Package
UM82C01–1	128 Key	40 DIP
UM82C01–2	88 Key	28 DIP

UM82C11-C

Printer Adapter Interface (PAI)

Features

- Programmable parallel printer interface
- Completely TTL-compatible I/O
- Reduces system package count
- User-controlled interrupt request
- Fully compatible with Z-80 and 8086 microprocessor families
- High driving capability
- On-chip oscillator can be used to generate 1.5 MHz to 20 MHz oscillation
- Single 5V supply

General Description

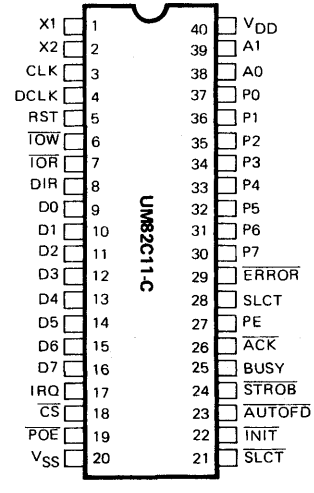
The UM82C11-C, Printer Adapter Interface (PAI), fabricated with a silicon gate CMOS process, offers parallel port interface between the CPU and the printer, and is especially suitable as a printer adapter for industry-standard personal computers.

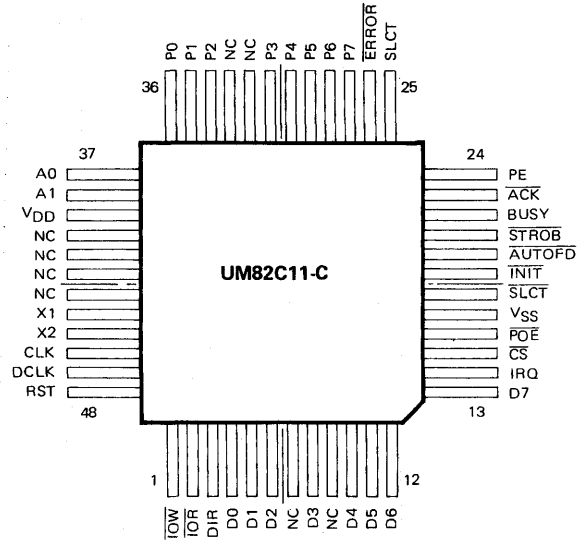
The UM82C11-C uses TTL logic to interface with the printer. Printer data bus pins can each source 2.6 mA and sink 24 mA. Each of the four printer control pins can source 1.5 mA and sink 7mA. The UM82C11-C fits the well-known Centronics printer interface.

PAI is also suitable for a personal computer interface board which contains RS-232C interface or display interface. The on-chip oscillator and ÷10 divider can be used to offer the BAUD-rate clock with RS-232C interface or the dot clock with monochrome display interface.

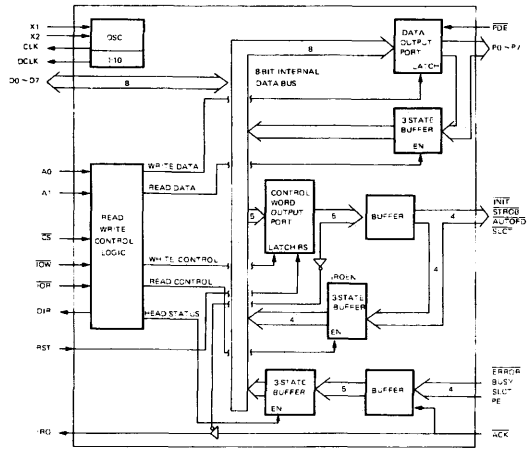
The user can use the Data Bus, $\overline{IOR}$, $\overline{IOW}$, IRQ, and $\overline{CS}$ to interface PAI with 8086 or Z-80 microprocessors.

Pin Configurations





Block Diagram



Absolute Maximum Ratings*

D.C Supply Voltage V_{DD}
. . . . . –0.5V to 7V (with respect to V_{SS})
Operating Temperature . . . . . 0°C – 70°C
Storage Temperature . . . . . –65°C – 150°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(T_A = 0° – 70°C, V_{DD} = +5V ± 10%)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{IL}	Input Low Voltage	–	0.4	0.8	V	–
V_{IH}	Input High Voltage	2.0	2.4	–	V	–
V_{OL}	Output Low Voltage	–	0.2	0.4	V	V_{DD} = 5.5V I_{OL} = Max
V_{OH}	Output High Voltage	2.4	–	–	V	V_{DD} = 4.5V I_{OH} = Max
I_{IN}	Input Leakage Current	–	–	± 10	μA	V_{DD} = 5.5V V_{IN} = V_{DD} or GND
I_{OLD}	Output Low Current Printer Data Bus = 0	–	–	24	mA	V_{OL} = 0.45V
I_{OHD}	Output High Current Printer Data Bus = 1	–	–	–2.6	mA	V_{DD} = 5.5V V_{OH} = 2.4V
I_{OLC}	Output Low Current Printer Control Bus = 0	–	–	7	mA	V_{OL} = 0.45V
I_{OHC}	Output High Current Printer Control Bus = 1	–	–	–1.5	mA	V_{DD} = 5.5V V_{OH} = 2.4V
I_{FL}	Tristate Leakage Current	–	–	± 10	μA	V_{DD} = 5.5V V_{FL} = V_{DD} or GND
I_{CC}	Quiescent Supply Current	–	–	200	μA	V_{DD} = 5.5V V_{IN} = 0V or V_{DD} I_O = 0
I_{OP}	Operating Current*	–	10	–	mA	Oscillation Frequency = 20 MHz, Typical Application

*Operating Current depends on oscillator frequency, output loading and operating temperature.

A C Characteristics

($T_A = 0° - 70°C$, $V_{CC} = +5V \pm 10\%$, $C_L = 50$ pF)

WRITE

Symbol	Parameter	Min.	Max.	Unit
T_{WW}	Write Pulse Width	200	–	ns
T_{AW}	Address to $\overline{IOW}$ Set-up Time	20	–	ns
T_{WA}	Address Hold Time after $\overline{IOW}$	20	–	ns
T_{DW}	Data to $\overline{IOW}$ Set-up Time	70	–	ns
T_{WD}	Data Hold Time after $\overline{IOW}$	30	–	ns
T_{WOL}	$\overline{IOW}$ = 1 to Data Latched	–	90	ns

READ

Symbol	Parameter	Min.	Max.	Unit
T_{RR}	Read Pulse Width	300	–	ns
T_{DD}	DIR Delay after $\overline{IOR}$	–	35	ns
T_{AR}	Address to $\overline{IOR}$ Set-up Time	20	–	ns
T_{RA}	Address Hold Time after $\overline{IOR}$	20	–	ns
T_{PR}	Printer Bus to $\overline{IOR}$ Set-up Time	0	–	ns
T_{RP}	Printer Bus Hold Time after $\overline{IOR}$	0	–	ns
T_{RDS}	$\overline{IOR}$ to D0 – D7 Output	–	70	ns
T_{RDR}	D0 – D7 Released after $\overline{IOR}$	0	30	ns

*Note: When the CPU reads the printer's status, output data may change if the printer signals are unstable.

OTHERS

Symbol	Parameter	Min.	Max.	Unit
T_{RSW}	Reset Pulse Width	40	–	ns
T_{RSCH}	Reset to Control Bus = 1 ($\overline{STROB}$, $\overline{AUTOFD}$, $\overline{SLCT}$) Propagation Delay	–	90	ns
T_{RSINI}	Reset to Control Bus $\overline{INIT}$ = 0 Propagation Delay	–	60	ns
T_{ID}	$\overline{ACK}$ to IRQ Propagation Delay	–	45	ns
T_{IZ}	IRQ Disable Time	–	50	ns
T_{IE}	IRQ Enable Time	–	50	ns
T_{RSIRZ}	IRQ floating after RST	–	50	ns
T_{DCKD}	CLK to DCLK Printer Data Enable	–	20	ns
T_{ZP}	POE low to Printer Data Enable	–	40	ns
T_{PZ}	POE high to Printer Data Disable	–	40	ns

Pin Description

Pin	Symbol	Name	I/O	Description
1 2	X1 X2	Crystal In	I	X1, X2 are the pins to which a crystal (whose frequency is between 1.5 MHz and 20 MHz) is attached.
3	CLK	Clock Out	O	A buffered oscillating clock output.
4	DCLK	Divided Clock	O	A buffered clock output whose frequency is one-tenth that of Pin 3.
5	RST	Reset	I	An active high RESET pin. When activated, printer control outputs $\overline{STROB}$, $\overline{AUTOFD}$, and $\overline{SLCT}$ are inactive, $\overline{INIT}$ is active, and IRQ is disabled remaining high impedance.
6	$\overline{IOW}$	I/O Write	I	A "Low" on this pin enables the CPU to write data or control words to PAI.
7	$\overline{IOR}$	I/O Read	I	A "Low" on this pin enables PAI to send data, control words or printer status to the CPU. It allows the CPU to read from PAI.
8	DIR	Direction	O	This output pin is active high only when $\overline{CS}$ and $\overline{IOR}$ are activated. It indicates the direction of data transfer between the CPU data bus and PAI. When high, PAI sends data, control words or printer status to the CPU.
9 ~ 16	D0 ~ D7	System Data Bus	I/O	The bidirectional 8-bit data bus pins are connected to the system data bus. Data or control words are transmitted or received upon execution of input or output instructions by the CPU. Status information on the printer is also received through the data bus.
17	IRQ	Interrupt Request	O	This is an interrupt request output pin, which is generated when $\overline{ACK}$ is high. This pin is enabled by writing D4 = 1 in the control word, and is disabled when D4 = 0. When RST is activated, this pin is disabled.
18	$\overline{CS}$	Chip Select	I	When $\overline{CS}$ = 0 it enables communications between the CPU and PAI.
19	$\overline{POE}$	Printer Data Output Enable	I	The printer data output (P0 ~ P7) is enabled when $\overline{POE}$ = 0 and disabled otherwise.
20	V_{SS}	Ground		Power ground pin.
21	$\overline{SLCT}$	Printer Select	I/O	When activated low, the printer is selected. This pin is programmable in bit $\overline{D3}$ by writing a control command. PAI outputs the inverted D3 to the $\overline{SLCT}$ pin.

(Cont.)

Pin Description (Continued)

Pin	Symbol	Name	I/O	Description
22	$\overline{INIT}$	Initialize	I/O	When activated low, the printer buffer is cleared. This pin is programmable in bit D2 by writing a control command and PAI outputs the D2 signal to this pin. The pulse width of the $\overline{INIT}$ must be more than 50 μs for initialization of most printers.
23	$\overline{AUTOFD}$	Auto Feed	I/O	When this pin is low, the printer is fed automatically, one line after printing. This pin is programmable in $\overline{D1}$ by writing a control command, and PAI outputs the inverted D1 to this pin.
24	$\overline{STROB}$	Data Strobe	I/O	When activated low, the printer reads in the data on printer data bus P0 ~ P7. It synchronizes the data strobe between PAI and the printer. This pin is programmable in bit D0 by writing a control command, and PAI outputs the inverted $\overline{D0}$ to this pin.
25	BUSY	Busy State	I	This is an input pin driven by the printer. A "High" indicates that the printer can't receive data at "During Data Entry", "During Part of Paper Feed", "During Printer Error Status", "During Printing" or "In Off-Line State". The CPU can read this signal in D7 by READ STATUS command.
26	$\overline{ACK}$	Acknowledge	I	This is an input pin driven by the printer. A "Low" indicates that the data has been received and that printer is ready to accept other data. The CPU can read this signal in $\overline{D6}$ by the READ STATUS command.
27	PE	Paper End	I	This is a pin output from the printer. A "High" indicates that the printer is out of paper. The CPU can read this signal in $\overline{D5}$ by the "READ STATUS" command.
28	SLCT	Printer Selected Status	I	This is always "High" unless the printer power is down. The CPU can read this signal in $\overline{D4}$ by the "READ STATUS" command.
29	$\overline{ERROR}$	Error Status	I	This is input pin driven by the printer. It is "Low" only when the printer is in error status as shown below: (1) Paper end status. (2) Abnormal motor operation. (3) Off-line state. The CPU can read this status in $\overline{D3}$ by the "READ STATUS" command.
30 ~ 37	P7 ~ P0	Printer Data Bus	I/O	These output pins send out the data to the printer by the CPU "Writing Data" command. They are compatible with the TTL logic level. The CPU can also "Read Back" these data which the CPU last wrote by the "READ DATA" command.
38 39	A0 A1	Address	I	These input addresses, in conjunction with $\overline{IOR}$, $\overline{IOW}$, $\overline{CS}$, control the selection of one of the five commands.
40	V_{DD}	Power Supply		+5V.

Note: The CPU can "Read Back" the control command it last wrote by reading the control word. These are $\overline{STROB}$, $\overline{AUTOFD}$, $\overline{INIT}$, $\overline{SLCT}$ and IRQEN on the data bus D0 ~ D4.

Function Description

When reset is activated (RST = 1), $\overline{STROBE}$ = 1, $\overline{AUTOFD}$ = 1, $\overline{INIT}$ = 0, $\overline{SLCT}$ = 1, and Interrupt Request "IRQ" is disabled. PAI offers five kinds of commands selected by A0, A1, $\overline{IOW}$, $\overline{IOR}$ and $\overline{CS}$, as shown below:

Input					Output	Operation
$\overline{CS}$	A1	A0	$\overline{IOR}$	$\overline{IOW}$	DIR	
1	X	X	X	X	0	PAI not activated.
0	0	0	1	0	0	Write data to the printer.
0	0	0	0	1	1	Read data on printer data bus.
0	0	1	0	1	1	Read status from the printer.
0	1	0	1	0	0	Write control word to the printer.
0	1	0	0	1	1	Read control word on printer control bus.
0	Others					(No operation.**)

Notes: **It is illegal to read anything when chip select is active and A0 = A1 = 1.

1. WRITE DATA to the PRINTER

Data on D0 ~ D7 are present on P0 ~ P7 bus, parallel and sent to the printer. At the rising edge of $\overline{IOW}$, data is latched on the P0 ~ P7 bus until the next falling edge of $\overline{IOW}$. When $\overline{POE}$ = 1, P0 ~ P7 bus are disabled to tristate. When $\overline{POE}$ = 0 the P0 ~ P7 is enabled.

2. READ DATA on PRINTER DATA BUS

At the falling edge of $\overline{IOR}$, data on P0 ~ P7 is sent back to CPU through D0 ~ D7, CPU reads back the printer data.

3. READ STATUS from the PRINTER

CPU reads the real-time status of the printer. The states are:

Data	$\overline{D7}$	D6	D5	D4	D3	D2	D1	D0
STATE	BUSY	$\overline{ACK}$	PE	SLCT	$\overline{ERROR}$	–	–	–

Note: The BUSY state is inverted on D7.

4. WRITE CONTROL WORD to the PRINTER

CPU writes the control word to the printer. The control signals are:

Data Bus	D7	D6	D5	D4	$\overline{D3}$	D2	$\overline{D1}$	$\overline{D0}$
CONTROL Signal	–	–	–	IRQEN	$\overline{SLCT}$	$\overline{INIT}$	$\overline{AUTOFD}$	$\overline{STROB}$

The control signals are latched on printer control bus at the rising edge of $\overline{IOW}$.

Note: "Interrupt Request Enable (IRQEN)" is not present on any output pin, but enables the output pin IRQ when D4 = 1, and disables IRQ to high impedance when D4 = 0 $\overline{SLCT}$, $\overline{AUTOFD}$ and $\overline{STROBE}$ are inverted on D3, D1 and D0 individually.

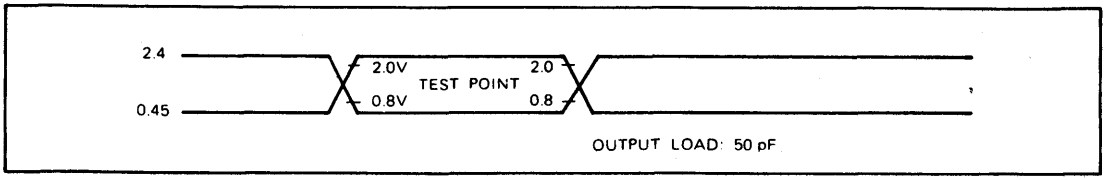
5. READ CONTROL WORD on PRINTER CONTROL BUS

At the falling edge of $\overline{IOR}$, control signal is latched on IRQEN, $\overline{SLCT}$ pin, $\overline{INIT}$ pin, $\overline{AUTOFD}$ pin and $\overline{STROB}$ pin are sent back to CPU on D4, D3, D2, D1 and D0 individually.

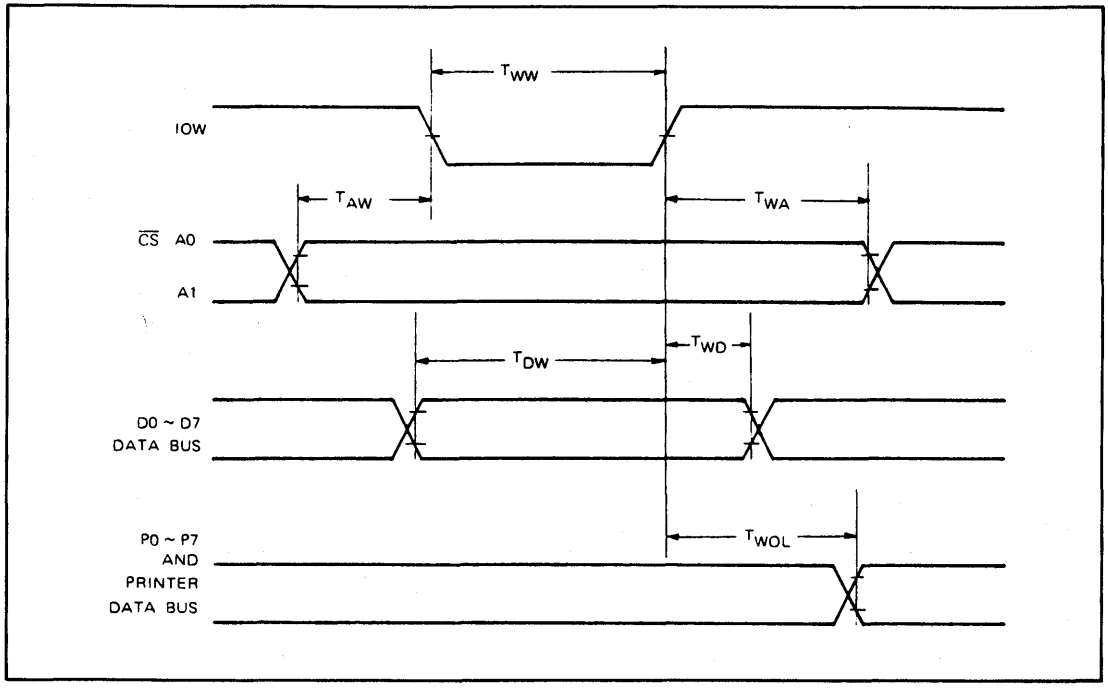
(1) When control word D4 = 0 ——→ IRQ pin floating.

(2) When control word D4 = 1 ——→ IRQ = $\overline{ACK}$.

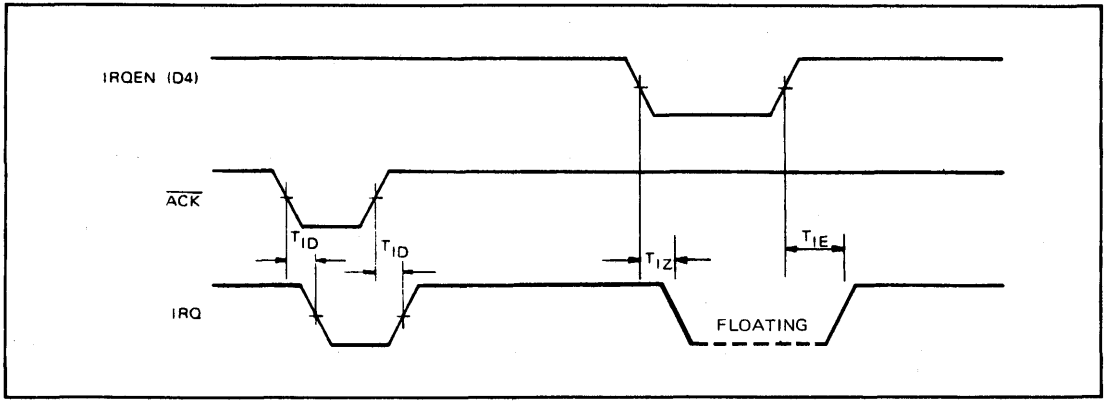
A.C. Testing Input Waveforms



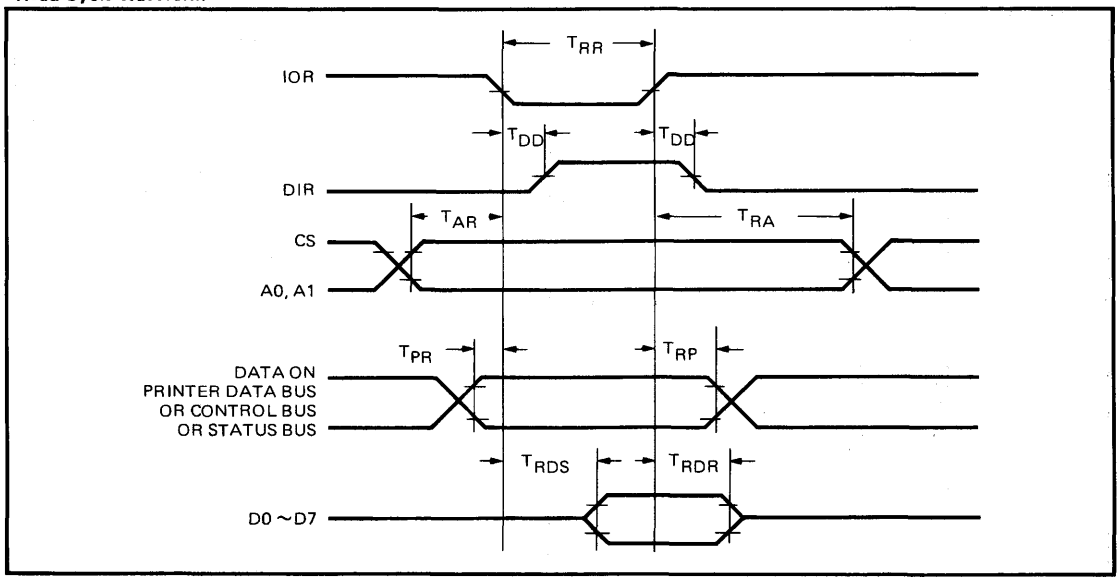
Write Cycle Waveform



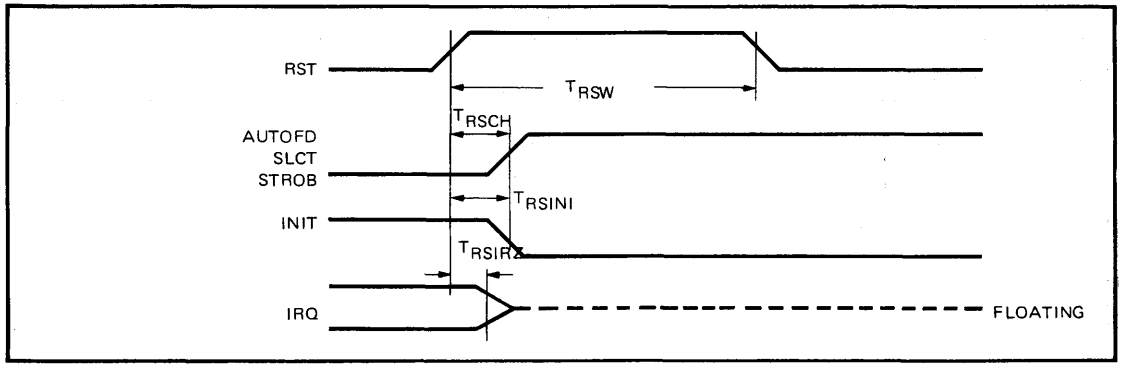
Interrupt Request Waveform



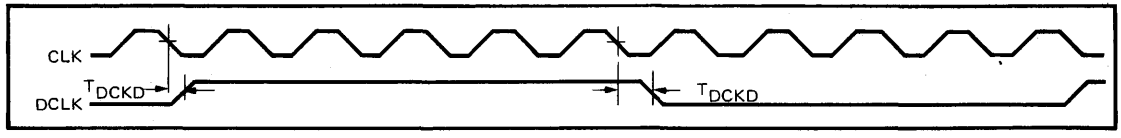
Read Cycle Waveform



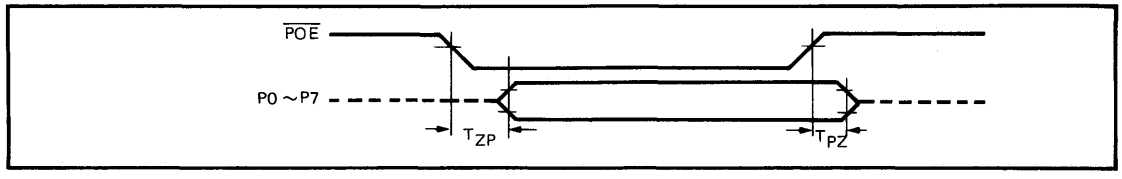
Reset Waveform



Clock Waveform

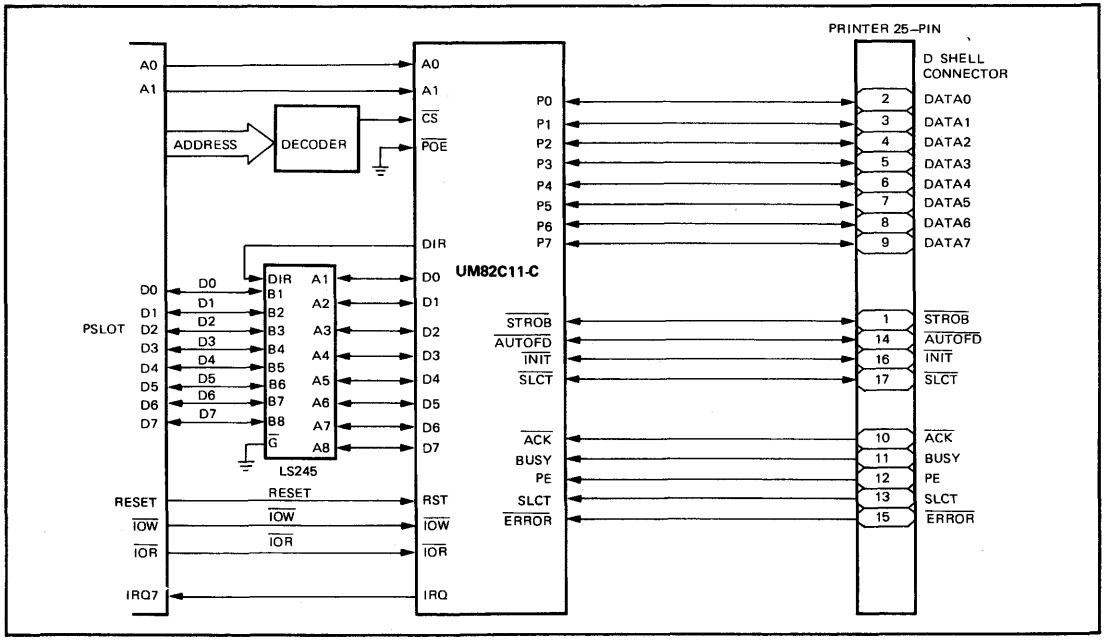


Printer Port Enable/Disable Waveform

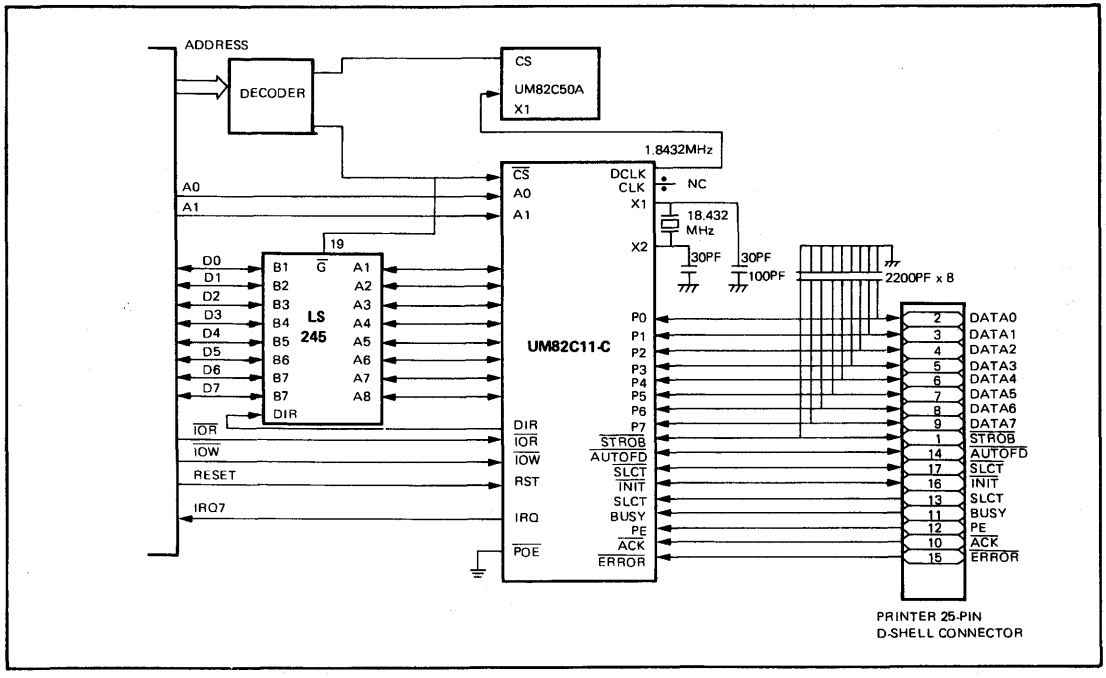


Typical Applications

PAI on Printer Card



PAI on Multifunction Card



UMC

UM82C450

Asynchronous Communication Element (ACE)

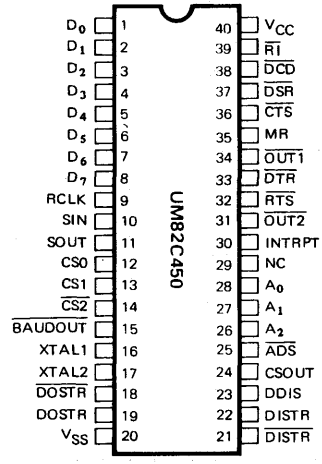
Features

- Adds or deletes standard asynchronous communication bits (start, stop, and parity) to or from a serial data stream
- Full double buffering eliminates the need for precise synchronization
- Independently controlled transmit, receive, line status, and data set interrupts
- Programmable baud rate generator allows division of any input clock by 1 to $(2^{16}-1)$ and generates the internal 16x clock
- Independent receiver clock input
- Modem control functions (CTS, RTS, DSR, DTR, RI, and carrier detect)
- Single +5 volt power supply
- Fully programmable serial-interface characteristics
  - 5-, 6-, 7-, or 8-bit characters
  - Even, odd, or no-parity bit generation and detection
  - 1, 1½, or 2-stop bit generation
  - Baud rate generation (DC to 56K baud)
- False start bit detection
- Complete status reporting capabilities
- Easily interfaces to most popular microprocessors
- Line break generation and detection
- Internal diagnostic capabilities
  - Loopback controls for communications link fault isolation
  - Break, parity, overrun, framing error simulation
- Fully prioritized interrupt system controls

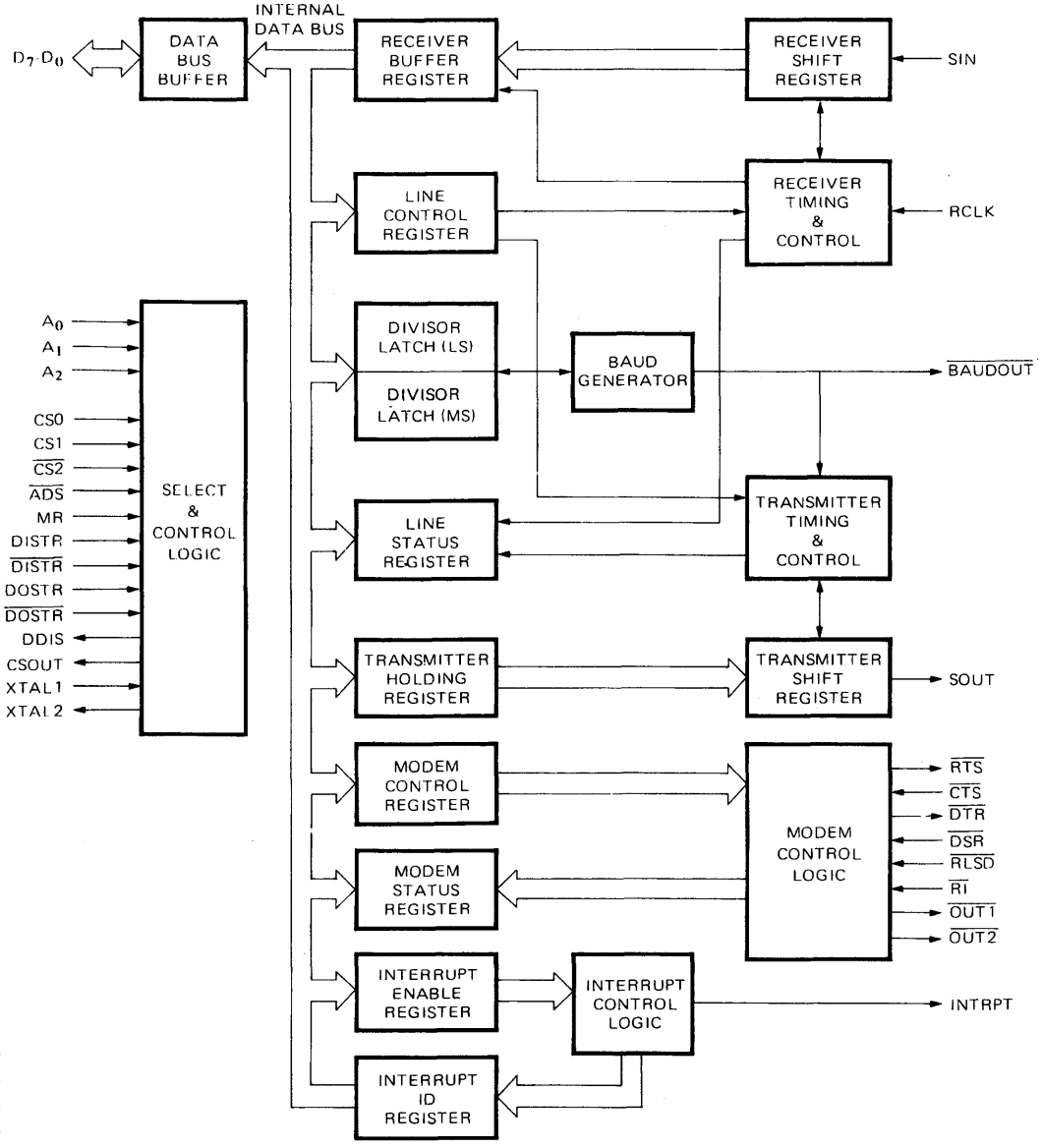
General Description

The UM82C450 is a programmable Asynchronous Communication Element (ACE) chip fabricated using the Si-Gate CMOS process. The UM82C450 is an improved version of the UM82C50. It performs serial-to-parallel conversion on data characters received from a peripheral device or a modem, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the ACE at any time during functional operation. The UM82C450 also includes a programmable baud rate generator that is capable of dividing the timing reference clock input by divisors of 1 to $(2^{16}-1)$ and producing a 16x clock for driving the internal transmitter logic.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias . . . . . 0°C to +70°C
Storage Temperature . . . . . –65°C to + 150°C
All input or Output Voltages with
Respect to V_{SS} . . . . . –0.5V to + 7.0V
Power Dissipation . . . . . 60 mW

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

T_A = 0°C to +70°C, V_{CC} = +5V ± 5%, V_{SS} = 0V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{ILX}	Clock Input Low Voltage		–0.5	0.8	V
V_{IHX}	Clock Input High Voltage		2.0	V_{CC}	V
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA on all*		0.4	V
V_{OH}	Output High Voltage	I_{OL} = –1.0 mA*	2.4		V
I_{CC} (AV)	Avg Power Supply Current (V_{CC})	V_{CC} = 5.25V, T_A = 25°C No Loads on output SIN, DSR, RLSD, CTS, RI = 2.0V All other inputs = 0.8V		10	mA
I_{IL}	Input Leakage	V_{CC} = 5.25V, V_{SS} = 0V All other pins floating. V_{IN} = 0V, 5.25V		± 10	μA
I_{CL}	Clock Leakage			± 10	μA
I_{OZ}	TRI-STATE Leakage	V_{CC} = 5.25V, V_{SS} = 0V V_{OUT} = 0V, 5.25V 1) Chip deselected 2) WRITE Mode, chip selected		± 20	μA
V_{ILMR}	MR Schmitt V_{IL}			0.8	V
V_{IHMR}	MR Schmitt V_{IH}		2.0		V

* Does not apply to XTAL2

Capacitance

T_A = 25°C, V_{CC} = V_{SS} = 0V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C_{XTAL2}	Clock Input Capacitance	f_C = 1 MHz Unmeasured pins returned to V_{SS}		15	20	pF
C_{XTAL1}	Clock Output Capacitance			20	30	pF
C_{IN}	Input Capacitance			6	10	pF
C_{OUT}	Output Capacitance			10	20	pF

AC Characteristics

T_A = 0°C to 70°C, V_{CC} = +5V ± 5%

Symbol	Parameter	Conditions	Min.	Max.	Unit
t_{AW}	Address Strobe Width		60	–	ns
t_{AS}	Address Setup Time		60		ns
t_{AH}	Address Hold Time		0		ns
t_{CS}	Chip Select Setup Time		60		ns
t_{CH}	Chip Select Hold Time		0		ns
t_{DIW}	$\overline{DISTR}$/DISTR Strobe Width		125		ns
t_{RC}	Read Cycle Delay		175		ns
RC	Read Cycle = t_{AR}* + t_{DIW} + t_{RC}		360		ns
t_{DD}	$\overline{DISTR}$/DISTR to Driver Disable Delay	@ 100 pF loading***		60	ns
t_{DDD}	Delay from $\overline{DISTR}$/DISTR to Data	@ 100 pF loading		125	ns
t_{HZ}	$\overline{DISTR}$/DISTR to Floating Data Delay	@ 100 pF loading***	0	100	ns
t_{DOW}	$\overline{DOSTR}$/DOSTR Strobe Width		100		ns
t_{WC}	Write Cycle Delay		200		ns
WC	Write Cycle = t_{AW} + t_{DOW} + t_{WC}		360		ns
t_{DS}	Data Setup Time		40		ns
t_{DH}	Data Hold Time		40		ns
t_{CSC}*	Chip Select Output Delay from Select	@ 100 pF loading		100	ns
t_{RA}*	Address Hold Time from $\overline{DISTR}$/DISTR		20		ns
t_{RCS}*	Chip Select Hold Time from $\overline{DISTR}$/DISTR		20		ns
t_{AR}*	$\overline{DISTR}$/DISTR Delay from Address		60		ns
t_{CSR}*	$\overline{DISTR}$/DISTR Delay from Chip Select		50		ns
t_{WA}*	Address Hold Time from $\overline{DOSTR}$/DOSTR		20		ns
t_{WCS}*	Chip Select Hold Time from $\overline{DOSTR}$/DOSTR		20		ns
t_{AW}*	$\overline{DOSTR}$/DOSTR Delay from Address		60		ns
t_{CSW}*	$\overline{DOSTR}$/DOSTR Delay from Select		50		ns
t_{MRW}	Master Reset Pulse Width		5		ns
t_{XH}	Duration of Clock High Pulse	External Clock (3.1 MHz Max.)	140		μs
t_{XL}	Duration of Clock Low Pulse	External Clock (3.1 MHx Max.)	140		ns
Baud Generator					
N	Baud Divisor		1	$2^{16}-1$	
t_{BLD}	Baud Output Negative Edge Delay	100 pF Load		125	ns
t_{BHD}	Baud Output Positive Edge Delay	100 pF Load		125	ns
t_{LW}	Baud Output Down Time	f_x = 2 MHz, ÷ 2, 100 pF Load	425		ns
t_{HW}	Baud Output Up Time	f_x = 3 MHz, ÷ 3, 100 pF Load	330		ns
Receiver					
t_{SCD}	Delay from RCLK to Sample Time			2	μs
t_{SINT}	Delay from Stop to Set Interrupt		1	1	RCLK** Cycles
t_{RINT}	Delay from $\overline{DISTR}$/DISTR (RD RBR/RDLSR) to Reset Interrupt	100 pF Load		1	μs

* Applicable only when $\overline{ADS}$ is tied low.

** RCLK is equal to t_{XH} and t_{XL}.

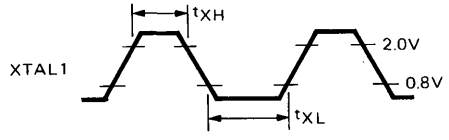
*** Charge and discharge time is determined by V_{OL}, V_{OH} and the external loading.

AC Characteristics

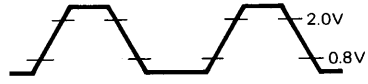
Symbol	Parameter	Conditions	Min.	Max.	Unit
Transmitter					
t_{HR}	Delay from $\overline{DOSTR}$/DOSTR (WR THR) to Reset Interrupt	100 pF Load		175	ns
t_{IRS}	Delay from Initial INTR Reset to Transmit Start		8	24	RCLK Cycles
t_{SI}	Delay from Initial Write to Interrupt		16	32	RCLK Cycles
t_{STI}	Delay from Stop to Interrupt (THRE)		8	8	RCLK Cycles
t_{IR}	Delay from $\overline{DISTR}$/DISTR (RD IIR) to Reset Interrupt (THRE)	100 Pf Load		250	ns
Modem Control					
t_{MDO}	Delay from $\overline{DOSTR}$/DOSTR (WR MCR) to Output	100 pF Load		200	ns
t_{SIM}	Delay to Set Interrupt from MODEM Input	100 pF Load			
t_{RIM}	Delay to Reset Interrupt from $\overline{DISTR}$/ DISTR (RD MSR)	100 pF Load		250	ns

Timing Waveforms

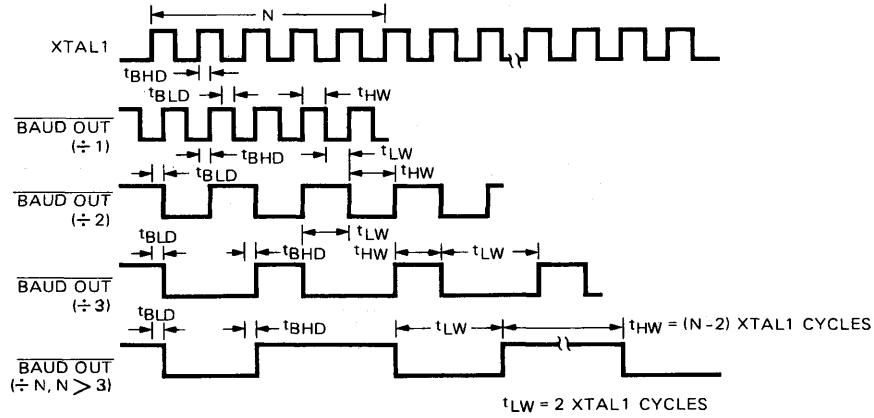
EXTERNAL CLOCK INPUT (3.1 MHz MAX.)



AC TEST POINTS

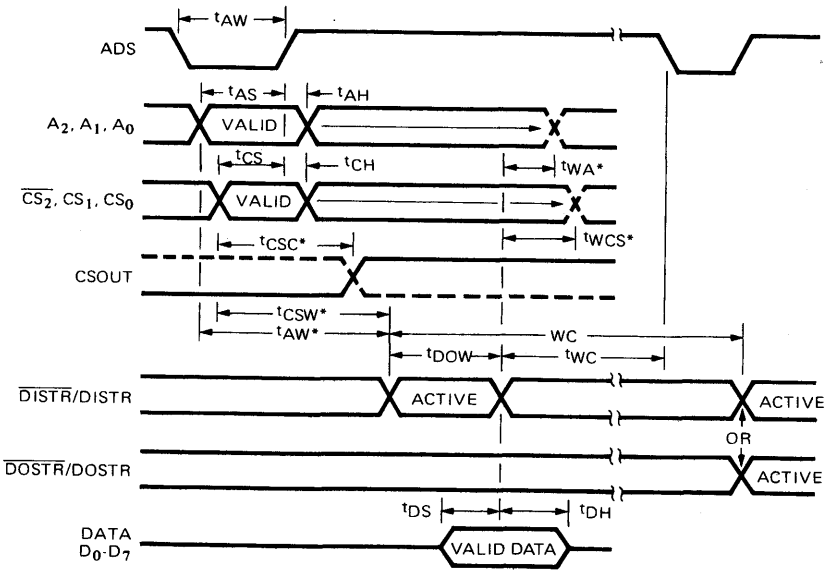


$\overline{BAUDOUT}$ TIMING



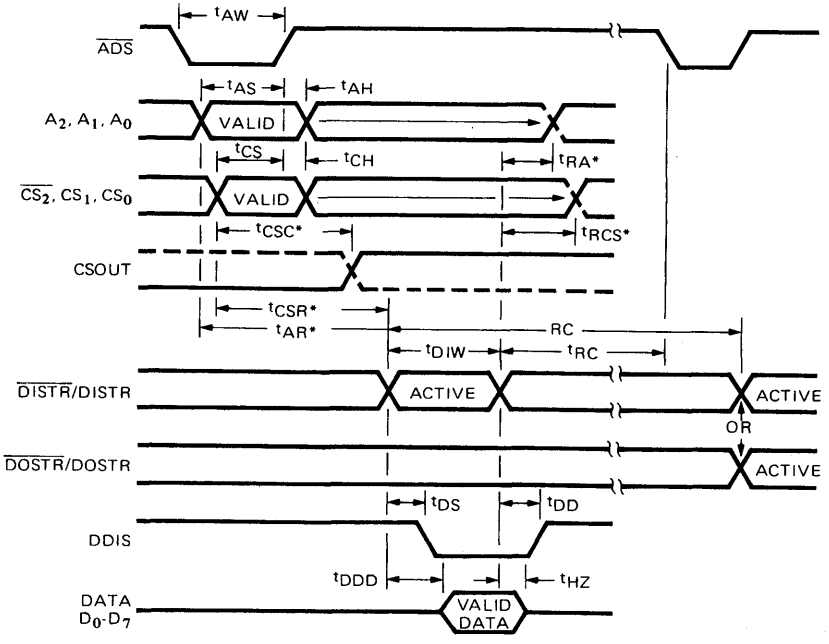
Timing Waveforms (Continued)

WRITE CYCLE



* Applicable Only When $\overline{ADS}$ is Tied Low.

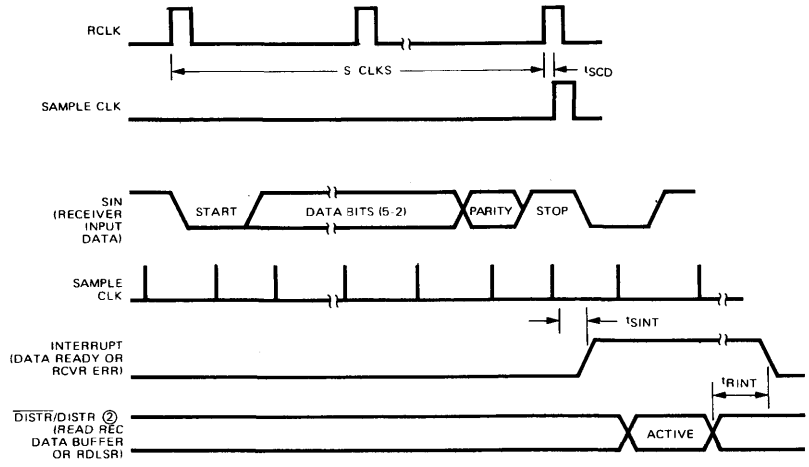
READ CYCLE



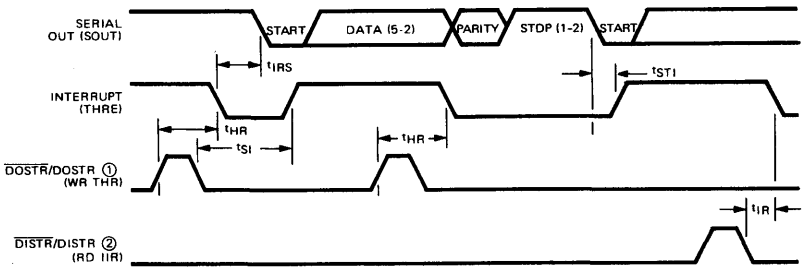
* Applicable Only When $\overline{ADS}$ is Tied Low.

Timing Waveforms (Continued)

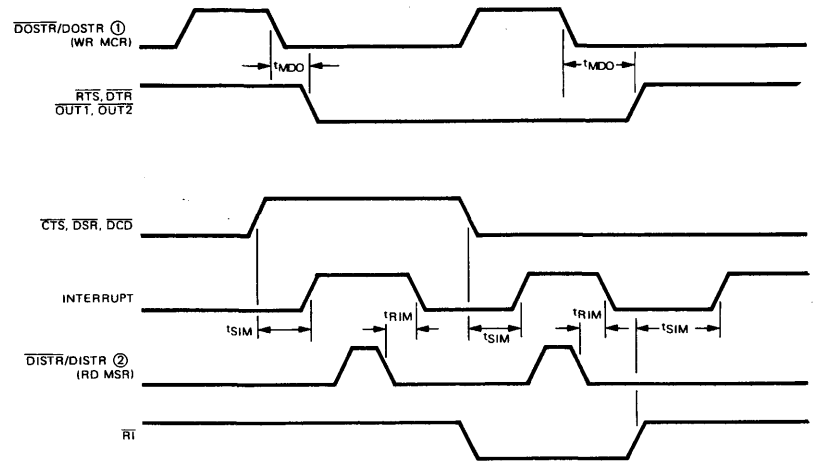
RECEIVER TIMING



TRANSMITTER TIMING



MODEM CONTROL TIMING



Pin Description

Input Signals

Chip Select (CS0, CS1, $\overline{CS2}$), Pins 12–14: When CS0 and CS1 are high and $\overline{CS2}$ is low, the chip is selected. Chip selection is complete when the decoded chip select signal is latched with an active (low) Address Strobe ($\overline{ADS}$) input. This enables communication between the ACE and the CPU.

Data Input Strobe (DISTR, $\overline{DISTR}$), Pins 22 and 21: When DISTR is high or $\overline{DISTR}$ is low while the chip is selected, it allows the CPU to read status information or data from a selected register of the ACE. Only an active DISTR or $\overline{DISTR}$ input is required to transfer data from the ACE during a read operation. Therefore, tie either the DISTR input permanently low or the $\overline{DISTR}$ input permanently high, if not used.

Data Output Strobe (DOSTR, $\overline{DOSTR}$), Pins 19 and 18: When DOSTR is high or $\overline{DOSTR}$ is low while the chip is selected, it allows the CPU to write data or control words into a selected register of the ACE. Only an active DOSTR or $\overline{DOSTR}$ input is required to transfer data to the ACE during a write operation. Therefore, tie either the DOSTR input permanently low or the $\overline{DOSTR}$ input permanently high, if not used.

Address Strobe ($\overline{ADS}$), Pin25: When low, provides latching for the Register Select (A_0, A_1, A_2) and Chip Select (CS0, CS1, $\overline{CS2}$) signals. An active $\overline{ADS}$ input is required when the Register Select (A_0, A_1, A_2) signals are not stable for the duration of a read or write operation. If not required, tie the $\overline{ADS}$ input permanently low.

Register Select (A_2, A_1, A_0), Pins 26–28: These three inputs are used during a read or write operation to select an ACE register to read from or write to as indicated in Table A. The DLAB must be set high by the system software to access the Baud Generator Divisor Latches.

Master Reset (MR), Pin 35: This input is buffered with a TTL-compatible Schmitt Trigger with 0.5V typical hysteresis. When high, it clears all the registers (except the Receiver Buffer, Transmitter Holding, and Divisor Latches), and the control logic of the ACE. Also, the state of various output signals (SOUT, INTRPT, $\overline{OUT\ 1}$, $\overline{OUT\ 2}$, $\overline{RTS}$, $\overline{DTR}$) are affected by an active MR input. (Refer to Table 1.)

Receiver Clock (RCLK), Pin 9: This input is the 16x baud rate clock for the receiver section of the chip.

Serial Input (SIN), Pin 10: Serial data input from the communications link (peripheral device, MODEM, or data set).

Clear to Send ($\overline{CTS}$), Pin 36: The $\overline{CTS}$ signal is a MODEM control function input whose conditions can be tested by the CPU by reading bit 4 (CTS) of the MODEM Status Register. Bit 0 (DCTS) of the MODEM Status Register indicates whether the $\overline{CTS}$ input has changed state since the previous reading of the MODEM Status Register. $\overline{CTS}$ has no effect on the Transmitter. Whenever the CTS bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

DLAB	A_2	A_1	A_0	Register
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	1	Line Control
X	1	0	0	MODEM Control
X	1	0	1	Line Status
X	1	1	0	MODEM Status
X	1	1	1	Scratch
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

Table A. Register Address

Data Set Ready ($\overline{DSR}$), Pin 37: When low, this indicates that the MODEM or data set is ready to establish the communications link and transfer data with the ACE. The $\overline{DSR}$ signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 5 (DSR) of the MODEM Status Register. Bit 1 (DDSR) of the MODEM Status Register indicates whether the $\overline{DSR}$ input has changed state since the previous reading of the MODEM Status Register. Whenever the DSR bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Data Carrier Detect ($\overline{DCD}$), Pin 38: When low, indicates that the data carrier has been detected by the MODEM or data set. The $\overline{DCD}$ signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 7 (DCD) of the MODEM Status Register. Bit 3 (DDCD) of the MODEM Status Register indicates whether the $\overline{DCD}$ input has changed state since the previous reading of the MODEM Status Register. $\overline{DCD}$ has no effect on the receiver. Whenever the DCD bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Ring Indicator ($\overline{RI}$), Pin 39: When low, indicates that a telephone ringing signal has been received by the MODEM or data set. The $\overline{RI}$ signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 6 (RI) of the MODEM Status Register. Bit 2 (TERI)

of the MODEM Status Register indicates whether the $\overline{RI}$ input has changed from a low to a high state since the previous reading of the MODEM Status Register. Whenever the RI bit of the MODEM Status Register changes from a high to a low state, an interrupt is generated if the MODEM Status Register is enabled.

V_{CC}, Pin 40: +5V supply.

V_{SS}, Pin 20: Ground (0V) reference.

Output Signals

Data Terminal Ready ($\overline{DTR}$), Pin 33: When low, informs the MODEM or data set that the ACE is ready to communicate. The DTR output signal can be set to an active low by programming bit 0 (DTR) of the MODEM Control Register to a high level. The DTR signal is set high upon a Master Reset operation. The DTR signal is forced to its inactive state (high) during loop mode operation.

Request to Send ($\overline{RTS}$), Pin 32: When low, informs the MODEM or data set that the ACE is ready to transmit data. The $\overline{RTS}$ output signal can be set to an active low by programming bit 1 (RTS) of the MODEM Control Register. The $\overline{RTS}$ signal is set high upon a Master Reset operation. The $\overline{RTS}$ signal is forced to its inactive state (high) during loop mode operation.

Output 1 ($\overline{OUT\ 1}$), Pin 34: User-designated output that can be set to an active low by programming bit 2 (OUT 1) of the MODEM Control Register to a high level. The $\overline{OUT\ 1}$ signal is set high upon a Master Reset Operation. The $\overline{OUT\ 1}$ signal is forced to its inactive state (high) during loop mode operation.

Output 2 ($\overline{OUT\ 2}$), Pin 31: User-designated output that can be set to an active low by programming bit 3 (OUT 2) of the MODEM Control Register to a high level. The $\overline{OUT\ 2}$ signal is set high upon a Master Reset Operation. The $\overline{OUT\ 2}$ signal is forced to its inactive state (high) during loop mode operation.

Chip Select Out (CSOUT), Pin 24: When high, indicates that the chip has been selected by active, CS0, CS1, and CS2 inputs. No data transfer can be initiated until the CSOUT signal is a logic 1. CSOUT goes low when chip is deselected.

Driver Disable (DDIS), Pin 23: Goes low whenever the CPU is reading data from the ACE. A high-level DDIS output can be used to disable an external transceiver (if used between the CPU and ACE on the D_7–D_0 Data Bus) at all times, except when the CPU is reading data.

Baud Out ($\overline{BAUDOUT}$), Pin 15: 16 x clock signal for the transmitter section of the ACE. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches. The BAUDOUT may also be used for the receiver section by tying this output to the RCLK input of the chip.

Interrupt (INTRPT), Pin 30: Goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER: Receiver Error Flag; Received Data Available; Transmitter Holding Register Empty; and MODEM Status. The INTRPT signal is reset low upon the appropriate interrupt service or a Master Reset operation.

Serial Output (SOUT), Pin 11: Composite serial data output to the communications link (peripheral, MODEM or data set). The SOUT signal is set to the Marking (logic 1) state upon a Master Reset operation.

Input/Output Signals

Input/Output Signals for the data bus and External clock.

Data (D_7–D_0) Bus, Pins 1–8: This bus comprises eight TRI-STATE input/output lines. The bus provides bidirectional communications between the ACE and the CPU. Data, control words, and status information are transferred via the D_7–D_0 Data Bus.

External Clock Input/Output (XTAL 1, XTAL 2), Pins 16 and 17: These two pins connect the main timing reference (crystal or signal clock) to the ACE.

Programmable Registers

The system programmer may access or control any of the ACE registers summarized in Table 2 via the CPU. These registers are used to control ACE operations and to transmit and receive data.

Line Control Register

The system programmer specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format, the programmer may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. The contents of the Line Control Register are indicated in Table 2 and are described below.

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits in each transmitted character. If bit 2 is a logic 0, one Stop bit is generated in the transmitted data. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one and a half Stop bits are generated. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two Stop bits are generated. The Receiver checks the first Stop-bit only, regardless of the number of Stop bits selected.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1s is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bits 3, 4 and 5 are logic 1 the Parity bit is transmitted and checked by the receiver as a logic 0. If bits 3 and 5 are 1 and bit 4 is a logic 0 then the Parity bit is transmitted as a 0.

Bit 6: This bit is the Break Control bit. When it is set to a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state. The break is disabled by setting bit 6 to a logic 0. The Break Control bit acts only on SOUT and has no effect on the transmitter logic.

Note: This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all 0s, pad character, in response to THRE.
2. Set break after the next THRE.
3. Wait for the transmitter to be idle, (TEMT = 1), and clear break when normal transmission has to be restored.

During the break, the Transmitter can be used as a character timer to accurately establish the break duration.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

Table 1. Reset Functions

Register/Signal	Reset Control	Reset State
Interrupt Enable Register	Master Reset	All Bits Low (0 - 3 forced and 4 - 7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High, Bits 1 and 2 Low Bits 3 - 7 are permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low,
Line Status Register	Master Reset	All Bits Low, Except Bits 5 & 6 are High
MODEM Status Register	Master Reset	Bits 0 - 3 Low Bits 4 - 7 — Input Signal
SOUT	Master Reset	High
INTRPT (RCVR Errs)	Read LSR/MR	Low
INTRPT (RCVR Data Ready)	Read RBR/MR	Low
INTRPT (THRE)	Read IIR/Write THR/MR	Low
INTRPT (Modem Status Changes)	Read MSR/MR	Low
$\overline{\text{OUT 2}}$	Master Reset	High
$\overline{\text{RTS}}$	Master Reset	High
$\overline{\text{DTR}}$	Master Reset	High
$\overline{\text{OUT 1}}$	Master Reset	High

Table 2. Summary of Accessible Registers

Bit No.	Register Address										
	0 DLAB=0	0 DLAB=0	1 DLAB=1	2	3	4	5	6	7	0 DLAB=1	1 DLAB=1
	Receiver Buffer Register Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident. Register Read Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Register	Divisor Latch (LS)	Divisor Latch (MS)
	RBR	THR	IER	IIR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Data Bit 0*	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	(WL Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OR)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	0	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Data Carrier Detect (DDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

* Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Programmable Baud Generator

The ACE contains a programmable Baud Generator that is capable of taking any clock input (DC to 3.1 MHz) and dividing it by any divisor from 1 to $2^{16}-1$). The output frequency of the Baud Generator is 16 x the Baud [divisor # = (frequency input) ÷ (baud rate x 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to ensure desired operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables 3 and 4 illustrate the use of the Baud Generator with crystal frequencies of 1.8432 MHz and 3.072 MHz respectively. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen. The maximum operating frequency of the Baud Generator is 3.1 MHz. However, when using divisors of 3 and below, the maximum frequency is equal to the divisor in MHz. For example, if the divisor is 1, then the maximum frequency is 1 MHz. In no case should the data rate be greater than 56K Baud.

Line Status Register

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of the Line Status Register are indicated in Table 2 and are described below.

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 is reset to a logic 0 by reading the data in the Receiver Buffer Register.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

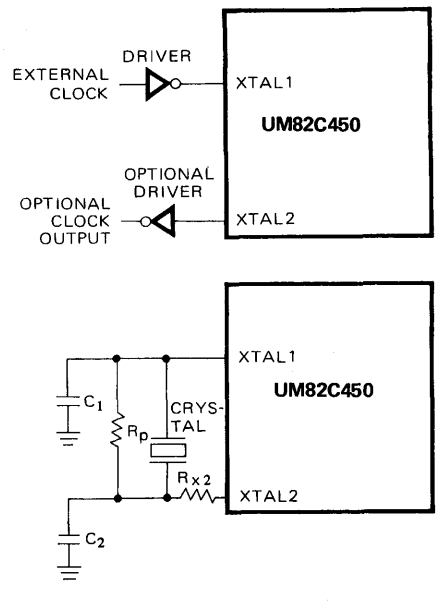
Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level). The FE indicator is reset whenever the CPU reads the contents of the Line Status indicator.

Table 3. Baud Rates Using 1.8432 MHz Crystal

Desired Baud Rate	Divisor Used to Generate 16 x Clock	Percent Error Difference Between Desired and Actual
50	2304	–
75	1536	–
110	1047	0.026
134.5	857	0.058
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.69
2400	48	–
3600	32	–
4800	24	–
7200	16	–
9600	12	–
19200	6	–
38400	3	–
56000	2	2.86

Typical Oscillator Application



Typical Crystal Oscillator Network

Crystal	R_p	R_{x2}	C_1	C_2
3.1 MHz	1 MΩ	1.5K	10 - 30 pF	40-60 pF
1.8 MHz	1 MΩ	1.5K	10 - 30 pF	40-60 pF

Table 4. Baud Rates Using 3.072 MHz Crystal

Desired Baud Rate	Divisor Used to Generate 16 x Clock	Pencent Error Difference Between Desired and Actual
50	3840	–
75	2560	–
110	1745	0.026
134.5	1428	0.034
150	1280	–
300	640	–
600	320	–
1200	160	–
1800	107	0.312
2000	96	–
2400	80	–
3600	53	0.628
4800	40	–
7200	27	1.23
9600	20	–
19200	10	–
38400	5	–

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits). The BI indicator is reset whenever the CPU reads the contents of the Line Status indicator. Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the ACE is ready to accept a new character for transmission. In addition, this bit causes the ACE to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrent with the loading of the Transmitter Holding Register by the CPU.

Bit 6: This bit is the Transmitter Empty (TEMT) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. It is reset to a logic 0 whenever either the THR or TSR contains a data character.

Table 5. Interrupt Control Functions

Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 2	**Bit 1**	**Bit 0**	**Priority Level**	**Interrupt Type**	**Interrupt Source**	**Interrupt Reset Control**
0	0	1	–	None	None	–
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

Bit 7: This bit is permanently set to logic 0. The Line Status Register is intended for read operations only. Writing to this register is not recommended as this operation is used for factory testing.

Interrupt Identification Register

The ACE has an on-chip interrupt capability that allows for flexibility in interfacing popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the ACE prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and Modem Status (priority 4).

Information indicating that a prioritized interrupt is pending and the type of that interrupt are stored in the Interrupt Identification Register (IIR). When addressed during chip-select time, the IIR freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The contents of the IIR are indicated in Table 2 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table 5.

Bits 3 through 7: These five bits of the IIR are always logic 0.

Interrupt Enable Register

This 8-bit register enables the four types of interrupts of the ACE to separately activate the chip interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are indicated in Table 2 and are described below.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bits 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

MODEM Control Register

This 8-bit register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in Table 2 and are described below.

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1. The DTR output of the ACE may be applied to an EIA inverting line drive (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send $\overline{RTS}$ output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the Output 1 ($\overline{OUT\ 1}$) signal, which is an auxiliary user-designated output. Bit 2 affects the $\overline{OUT\ 1}$ output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the Output 2 ($\overline{OUT\ 2}$) signal, which is an auxiliary user-designated output. Bit 3 affects the $\overline{OUT\ 2}$ output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a local loopback feature for diagnostic testing of the ACE. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to the Marking (logic 1) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and RI) are disconnected; and the four MODEM Control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT\ 1}$, and $\overline{OUT\ 2}$) are internally connected to the four MODEM Control inputs, and the MODEM Control output pins are forced to their inactive state (high). In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit-and received-data paths of the ACE.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational, but the interrupts' sources are

now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

Bit 5 through 7: These bits are permanently set to logic 0.

MODEM Status Register

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

Accessible Registers

The contents of the MODEM Status Register are indicated in Table 2 and are described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the Chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from a low to a high state.

Bit 3: This bit is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the $\overline{DCD}$ input to the chip has changed state. Whenever bits 0, 1, 2, or 3 are set to logic 1, a MODEM Status Interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send ($\overline{CTS}$) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.

Bit 5: This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to DTR in the MCR.

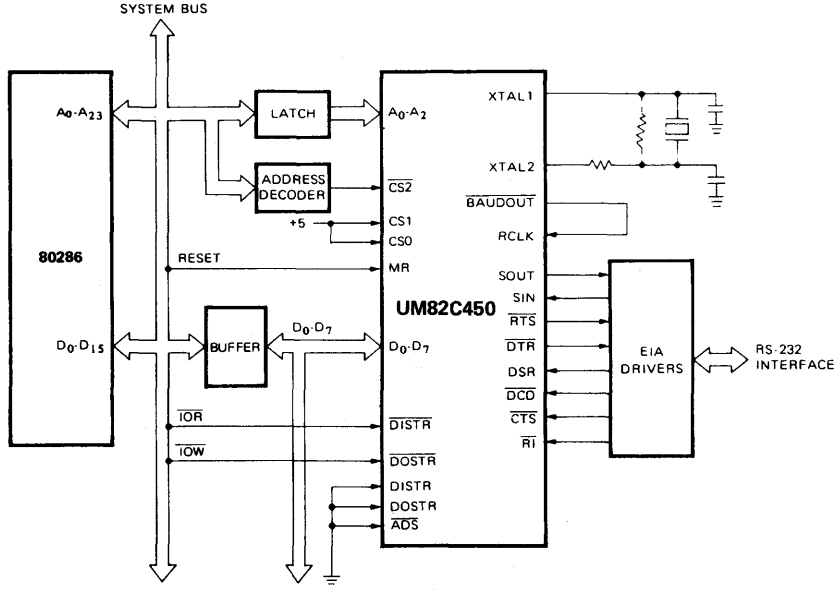
Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 1 in the MCR.

Bit 7: This bit is the complement of the Data Carrier Detect ($\overline{DCD}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 2 of the MCR.

Scratchpad Register

This 8-bit Read/Write Register does not control the ACE in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

Typical Application



UM82C451

Parallel/Asynchronous Communication Element

Features

- IBM PC/AT compatible
- UM82C450 with on-board Centronix printer interface
- Completely pin-and upward-compatible with the dual serial channel UM82C452
- Independent control of transmit, receive, line status and data set interrupts
- Individual modem control signals
- Programmable Serial interface characteristics:
  - 5-, 6-, 7- or 8-bit characters
  - Even-, odd-or no-parity bit generation and detection
  - 1, 1 1/2 or 2 stop bit generation
- Three-state TTL drive for the data and control bus

Description

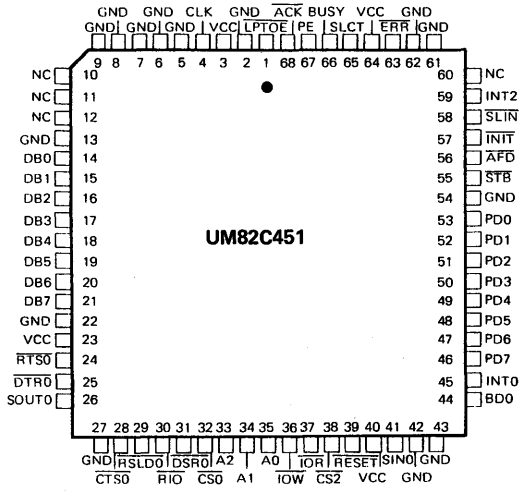
The UM82C451 is an enhanced version of the popular UM82C450 asynchronous communications element (ACE). The serial channel performs serial-to-parallel conversion on data characters received from peripheral devices or modems, and parallel-to-serial conversion of data characters transmitted by the CPU. The complete status of the Parallel/Asychronous Communications Element (P/ACE) can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the transfer operations being performed, and error conditions. It is fully pin-and upward-compatible with the dual serial channel UM82C452. The second serial channel of the UM82C452 occupies pins that are VCC, GND, or NC (not connected) on the UM82C451.

The UM82C451 also provides the user with a fully bi-directional parallel data port that fully supports the parallel Centronics type printer. This port allows information received from either serial communication port to be printed from the P/ACE. The parallel port, together with the serial port, provides IBM PC/AT compatible computers with a single device to serve the two system ports.

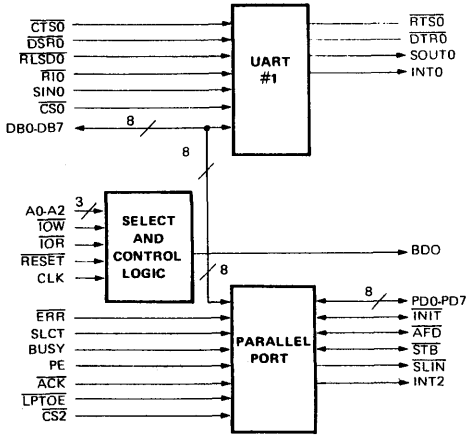
A programmable baud rate generator is included that can divide the timing reference clock input by a divisor between 1 and $(2^{16}-1)$.

The UM82C451 is packaged in a 68-pin plastic leaded chip carrier.

Pin Configuration



Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description
37	$\overline{IOR}$	I	Input/Output Read strobe: This is an active Low input signal used to cause the selected channel to output data to data bus (DB0-DB7).
36	$\overline{IOW}$	I	Input/Output Write strobe: This is an active Low input signal used to cause data input from data bus (DB0-DB7) to the channel selected.
33-35	A2-A0	I	Address lines A2-A0: The address lines are used to select the internal register in selected channels during CPU cycle.
32, 38	$\overline{CS0}$, $\overline{CS2}$	I	Chip Selects: Each chip select input acts as an enable of each channel during read and write, $\overline{CS0}$ selects Serial Channel 0 and $\overline{CS2}$ selects Parallel Port.
44	BDO	O	Bus Buffer Output: This active high output is asserted when any channel is selected. This output can be used to control the system bus driver device (74LS245).
14-21	DB0-DB7	I/O	Data Bit DB0-DB7: The data bus provides eight three-state I/O lines for the transfer of data, control and status information between CPU and UM82C451. These lines are normally in a high-impedance state except during read operation. D0 is the least significant bit (LSB) and is the first serial bit to be transmitted or received.
39	$\overline{RESET}$	I	Reset: When low, the reset input forces the UM82C451 into an idle state in which all serial data activities are suspended. The Registers and signals of the UM82C451 are all cleared to the state as indicated in Table 1.
26	SOUT0	O	Serial Data Output: This line is the serial data output of UART, used to transmit serial data to communication link. SOUT is held in marking (logic 1) state when the transmitter is disabled, reset, the Transmitter Register is empty, or when in the loop mode.
41	SIN0	I	Serial Data Input: This line is used to receive serial data from the communication line or modem into the UART. Data on serial data inputs is disabled during the loop mode.
24	$\overline{RTS0}$	O	Request To Send: This signal is an active low output for UART, When active, it informs the Modem or data set that the controller is ready to send data. This signal is set low by writing logic 1 to MCR (1) and reset to high by Reset.
25	$\overline{DTR0}$	O	Data Terminal Ready: This signal is an active low output for UART. When active, it informs the modem or data set that the controller is ready to communicate. This signal is set low by writing logic 1 to MCR (0) and reset to high by Reset.

Pin Description (Continued)

Pin No.	Symbol	I/O	Description
28	$\overline{CTS0}$	I	Clear to send: This signal is an active low input for UART. The logic state of this signal is reflected in MSR (4) and any change of state in either $\overline{CTS}$ pin will set DCTS bit MSR (0) of each Modem Status Register. When active, this pin informs that the Modem or data set is ready to receive data.
31	$\overline{DSR0}$	I	Data Set Ready: This signal is an active low input for UART. The logic state of this signal is reflected in MSR (5) and any change of state in either DSR pin will set DDSR bit MSR (1) of each Modem Status Register. When active, the signal informs that the Modem or data set is ready to establish communication.
29	$\overline{RLSD0}$	I	Receiver Line Signal Detect: This is an active low input for UART. The logic state of this signal is reflected in MSR (7) and any change of state in either DCD pin will set DDCD bit MSR (3) of each Modem Status Register. When active, this pin informs that the data carrier has been detected by Modem or data set.
30	$\overline{RI0}$	I	Ring Indicator: This signal is an active low input for UART. The logic state of this signal is reflected in MSR (6) and TERI bit MSR (2) will be set when the state of either RI pin is changed from low to high.
4	CLK	I	Clock Input: The external clock input from a crystal oscillator.
1	$\overline{LPTOE}$	I	Line Printer Output Enable: This input signal enables the data outputs of the parallel line printer when it is low. When it is high, the data pins of line printer are held in a high-impedance state. This pin may be tied to ground for normal line printer operation.
53-46	PD0-PD7	O	Parallel Data Bus: This bus provides a byte-wide input or output port to the system. The eight lines are held in a high-impedance state when the port is not selected.
68	$\overline{ACK}$	I	Acknowledge: This signal goes low to indicate that the printer has already received a character and is ready to accept another.
67	PE	I	Paper Empty: This signal goes high when the line printer has run out of paper.
66	BUSY	I	Busy: This signal goes high when the line printer has a local operation in progress and cannot accept data.
65	SLCT	I	Selected: This signal goes high when the line printer has been selected.

Pin No.	Symbol	I/O	Description
63	$\overline{ERR}$	I	Error: This signal goes low when the line printer has encountered an error condition.
58	$\overline{SLIN}$	I/O	Line Printer Select: This signal is used to select the printer when it is low.
57	$\overline{INIT}$	I/O	Line Printer Initialize: When this signal goes low, it will allow the line printer initialization routine to be started.
56	$\overline{AFD}$	I/O	Line Printer Autofeed: When this signal goes low, it will cause the printer to line-feed after a line is printed.
55	$\overline{STB}$	I/O	Line Printer Strobe: When this signal is low, it provides the line printer a signal to latch the data currently on the parallel port. This signal should keep low at least 0.5 μs to ensure the completion of data latch.
45	INT0	O	Serial Channel Interrupt: Serial channel interrupt goes high when one of the following interrupts has an active condition and is enabled by the IER of its associated channel: Receiver Error Flag, Receiver Data Available, Transmitter Holding Register Empty, and Modem Status. The interrupt is reset to low upon appropriate service. This pin will be held in a high-impedance state if the MCR (3) of each associated channel is programmed low (logic 0).
59	INT2	O	Line Printer Interrupt: This interrupt goes low when ACK goes low. This signal is enabled by Bit 4 of the Printer Control Register and will be held in a high-impedance state if Bit 4 of the printer Control Register is programmed low.
3, 23, 40, 64	V_{CC}	I	Power Supply: +5V
2, 5, 6-9, 13, 22, 27, 42, 43, 54, 61, 62	GND		Ground: 0V
10-12, 60	NC		No Connection

Functional Description:

Serial Channel Registers

Three types of internal registers are used in the serial channel of the UM82C451. They are used in the operation of the device, and are the control, status, and data registers. The control registers are the Bit Rate Select Register DLL (Divisor Latch LSB) and DLM (Divisor Latch MSB), Line Control Register. Interrupt Enable Register, and the Modem Control registers, while the status registers are the Line Status Registers and the Modem Status Register. The data registers are the Receiver Buffer Register and the Transmitter Holding Register. The Address, Read, and Write inputs are used in conjunction with the Divisor Latch Access Bit in the Line Control Register [LCR (7)] to select the register to be written to or read (see Table 1). Individual bits within these registers are referred to by the register mnemonic and the bit number in parenthesis. An example, LCR (7) refers to Line Control Register Bit 7.

The Transmitter Buffer Register and Receiver Buffer Register are data registers holding from five to eight bits of data. If less than eight data bits are transmitted, data is right justified to the LSB. Bit 0 of a data word is always the first serial data bit received and transmitted. The UM82C451 data registers are double-buffered so that read and write operations can be performed at the same

Table 1. Serial Channel Internal Registers

DLAB	A2	A1	A0	Mnemonic	Register
0	0	0	0	RBR	Receiver Buffer Register (read only)
0	0	0	0	THR	Transmitter Holding Register (write only)
0	0	0	1	IER	Interrupt Enable Register
X	0	1	0	IIR	Interrupt Identification Register (read only)
X	0	1	1	LCR	Line Control Register
X	1	0	0	MCR	Modem Control Register
X	1	0	1	LSR	Line Status Register
X	1	1	0	MSR	Modem Status Register
X	1	1	1	SCR	Scratch Register
1	0	0	0	DLL	Divisor Latch (LSB)
1	0	0	1	DLM	Divisor Latch (MSB)

X = "Don't Care" 0 = Logic Low 1 = Logic High

Note: The Serial Channel 0 is accessed when $\overline{CS0}$ is low.

time the UART is performing the parallel-to-serial and serial-to-parallel conversion.

The format of the data character is controlled by the Line Control Register. The contents of the LCR may be read, eliminating the need for separate storage of the line characteristics in system memory. The contents of the LCR are described below.

LCR (0) Word Length Select Bit 0 (WLS0)
LCR (1) Word Length Select Bit 1 (WLS1)
LCR (2) Stop Bit Select (STB)
LCR (3) Parity Enable (PEN)
LCR (4) Even Parity Select (EPS)
LCR (5) Stick Parity
LCR (6) Set Break
LCR (7) Divisor Latch Access Bit (DLAB)

LCR (0) and LCR (1) word length select bit 1: The number of bits in each serial character is programmed as shown in the following chart:

LCR (1)	LCR (0)	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

LCR (2) Stop Bit Select: LCR (2) specifies the number of stop bits in each transmitted character. If LCR (2) is a logic 0, one stop bit is generated in the transmitted data. If LCR (2) is a logic 1 when a 5-bit word length is selected, 1.5 stop bits are generated. If LCR (2) is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two stop bits are generated. The receiver checks for two stop bits if programmed.

LCR (3) Parity Enable: When LCR (3) is high, a parity bit between the last data word bit and stop bit is generated and checked.

LCR (4) Even Parity Select: When parity is enabled (LCR (3) = 1). LCR (4)-0 selects odd parity, and LCR (4) = 1 selects even parity.

LCR (5) Stick Parity: When parity is enabled (LCR (3) = 1), LCR (5) = 1 causes the transmission and reception of a parity bit to be in the opposite state from that indicated by LCR (4). This allows the user to force parity to a known state and for the receiver to check the parity bit in a known state.

LCR (6) Break Control: When LCR (6) is set to a logic "1", the serial output (SOUT) is forced to the spacing (logic 0) state. The break is disabled by setting LCR (6) to a logic "0". The Break Control bit acts only on SOUT and has no effect on the transmitter logic. Break Control enables the CPU to alert a terminal in a computer communications system. If the following sequence is used, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all "0"s pad character in response to THRE.
2. Set break in response to the next THRE.
3. Wait for the transmitter to be idle (TEMT = 1, and clear break when normal transmission has to be restored.

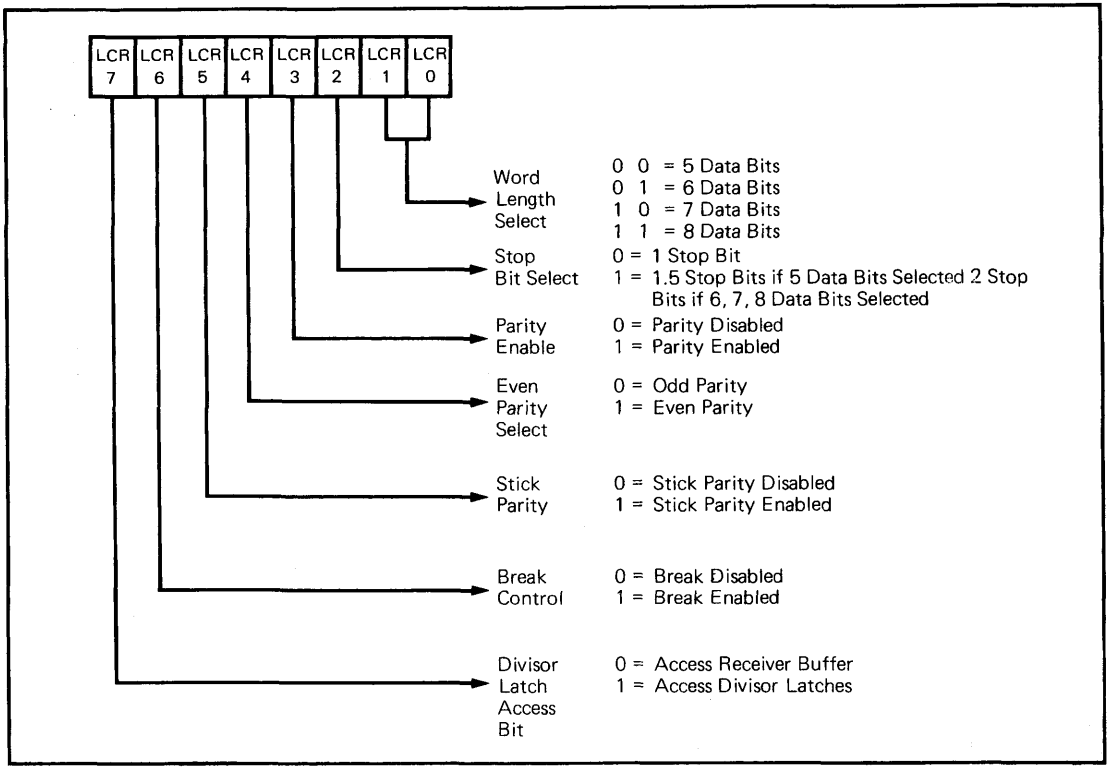


Figure 1. Line Control Register

LCR (7) Divisor Latch Access Bit (DLAB): LCR (7) must be set high (logic "1") to access the Divisor Latches DLL and DLM of the Baud Rate Generator during a read or write operation. LCR (7) must be input low to access the Receiver Buffer, the Transmitter Holding, or the Interrupt Enable Registers.

The Line Status Register (LSR) is a single register that provides status indications. The LSR is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of the serial channel of the UM82C451.

Three error flags OE, FE, and PE provide the status of any error conditions detected in the receiver circuitry. During reception of the stop bits, the error flags are set high by an error condition. The error flags are not reset by the absence of an error condition in the next received character. The flags reflect the last character only if no overrun occurred. The Overrun Error character in the Receiver Buffer Register has been over-written by a character from the Receiver Shift Register before being read by the CPU. The character is thereby lost. Framing Error (FE) indicates that the last character received contained incorrect (low) stop bits. This is caused by the absence of the required stop bit or by a stop bit too short to be detected. Parity Error (PE) indicates that the last character received had a parity error based on the programmed and calculated parity of the received character.

The Break Interrupt (BI) status bit indicates that the last character received was a break character. A break character is an invalid data character. However, it is an entire character, including parity and stop bits.

The Transmitter Holding Register Empty (THRE) bit indicates that the THR register is empty and may receive another character. The Transmission Shift Register Empty (TEMT) bit indicates that the Transmitter Shift Register is empty, and the serial channel has completed transmission of the last character to be sent. If the interrupt is enabled [IER (1)] an active THRE causes an interrupt (INTRPT).

The Data Ready (DR) bit indicates that the RBR has been loaded with a received character (including Break) and that the CPU may access this data.

Reading the LSR clears LSR (1) $\overline{\text{LSR}}$ (4). (OE, PE, FE, and BI.)

The contents of the Line Status Register shown in Table 2 are described as follows:

Table 2. Line Status Register Bits

LSR Bits	Logic 1	Logic 0
LSR (0) Data Ready (DR)	Ready	Not Ready
LSR (1) Overrun Error (OE)	Error	No Error
LSR (2) Parity Error (PE)	Error	No Error
LSR (3) Framing Error (FE)	Error	No Error
LSR (4) Break Interrupt (BI)	Break	No Break
LSR (5) Transmitter Holding Register Empty (THRE)	Empty	Not Empty
LSR (6) Transmitter Empty (TEMT)	Empty	Not Empty
LSR (7) Not Used		

LSR (0) Data Ready (DR): Data Ready is set high when an incoming character has been received and transferred into the Receiver Buffer Register. LSR (0) is reset low by a CPU read of the data in the Receiver Buffer Register.

LSR (1) Overrun Error (OE): Overrun Error indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, overwriting the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

LSR (2) Parity Error (PE): Parity Error indicates that the received data character does not have the correct even or odd parity, as selected by the Even Parity Select bit [LCR (4)]. The PE bit is set high upon detection of a parity error, and is reset low when the CPU reads the contents of the LSR.

LSR (3) Framing Error (FE): Framing Error indicates that the received character did not have a valid stop bit. LSR (3) is set high when the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is reset low when the CPU reads the contents of the LSR.

LSR (4) Break Interrupt (BI): Break Interrupt is set high when the received data input is held in the spacing (logic 0) state for longer than a full word transmission time (start bit + data bits + parity + stop bits). The BI indicator is reset when the CPU reads the contents of the Line Status Register.

LSR (1)-LSR (4) are the error conditions that produce a Receiver Line Status interrupt (priority 1 interrupt in the Interrupt Identification Register (IIR)) when any of the conditions are detected. This interrupt is enabled by setting IER (2) = 1 in the Interrupt Enable Register.

LSR (5) Transmitter Holding Register Empty (THRE): THRE indicates that the UM82C450 is ready to accept a new character for transmission. The THRE bit is set high when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. LSR (5) is reset low by the loading of the Transmitter Holding Register by the CPU. LSR (5) is not reset by a CPU read of the LSR.

When the THRE interrupt is enabled (IER (1) = 1). THRE causes a priority 3 interrupt in the IIR. If THRE is the interrupt source indicated in IIR, INTRPT is cleared by a read of the IIR.

LSR (6) Transmitter Empty (TEMT): TEMT is set high when the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. LSR (6) is reset low when a character is loaded into the THR and remains low until the character is transferred out of SOUT. TEMT is not reset low by a CPU read of the LSR.

LSR (7): This bit is always 0.

The Modem Control Register (MCR) controls the interface with the modem or data set as described in Table 3. MCR can be written and read. The $\overline{RTS}$ and $\overline{DTR}$ outputs are directly controlled by their control bits in this register. A high input asserts a low (true) at the output pins. MCR Bits 0, 1, 3, and 4 are shown below:

MCR (0): When MCR (0) is set high, the $\overline{DTR}$ output is forced low. When MCR (0) is reset low, the $\overline{DTR}$ output is forced high. The $\overline{DTR}$ output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

MCR (1): When MCR (1) is set high, the RTS output is forced low. When MCR (1) is reset low, the RTS output is forced high. The $\overline{RTS}$ output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

MCR (3): When MCR (3) is set high, the INT output is enabled.

MCR (4): MCR (4) provides a local loopback feature for diagnostic testing of the channel. When MCR (4) is set high, Serial Output (SOUT) is set to the marking (logic "1") state, and the receiver data input Serial Input (SIN) is disconnected. The output of the Transmitter Shift

Table 3. Modem Control Register Bits

MCR Bits	Logic 1	Logic 0
MCR (0) Data Terminal Ready (DTR)	$\overline{DTR}$ Output Low	$\overline{DTR}$ Output High
MCR (1) Request to Send (RTS)	$\overline{RTS}$ Output Low	$\overline{RTS}$ Output High
MCR (2) 0		
MCR (3) Interrupt (INT) Enable	INT Enabled	INT Disabled
MCR (4) Loop	Loop Enabled	Loop Disabled
MCR (5) 0		
MCR (6) 0		
MCS (7) 0		

Register is looped back into the Receiver Shift Register input. The three modem control inputs ($\overline{CTS}$, $\overline{DSR}$, and $\overline{RI}$) are disconnected. The modem control outputs ($\overline{DTR}$ and $\overline{RTS}$) are internally connected to the four modem control inputs. The modem control output pins are forced to their inactive state (high).

In the diagnostic mode, data transmitted is immediately received. This allows the processor to verify the transmit and receive data paths of the selected serial channel. Bits MCR (5)-MCR (7) are permanently set to logic 0.

The MSR provides the CPU with status of the modem input lines from the modem or peripheral devices. The MSR allows the CPU to read the serial channel modem signal inputs by accessing the data bus interface of the UM82C451. In addition to the current status information, four bits of the MSR indicate whether the modem inputs have changed since the last reading of the MSR. The delta status bits are set high when a control input from the modem changes state, and reset low when the CPU reads the MSR.

The modem input lines for each channel are $\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$ and $\overline{RLSD}$, $\overline{MSR}$ (4) $\overline{MSR}$ (7) are status indications of these lines. The status indications follow the status of the input lines. If the modem status interrupt in the Interrupt Enable Register is enabled [IER (3)], a change of state in modem input signals will be reflected by the modem status bits in the IIR register, and an interrupt (INTRPT) is generated. The MSR is a priority 4 interrupt. The contents of the Modem Status Register are described in Table 4. Note that the states (high or low) of the status bits are inverted versions of the actual input pins.

MSR (0) Delta Clear to Send (DCTS): DCTS indicates that the $\overline{CTS}$ input to the serial channel has changed state since the last time it was read by the CPU.

MSR (1) Delta Data Set Ready (DDSR): DDSR indicates

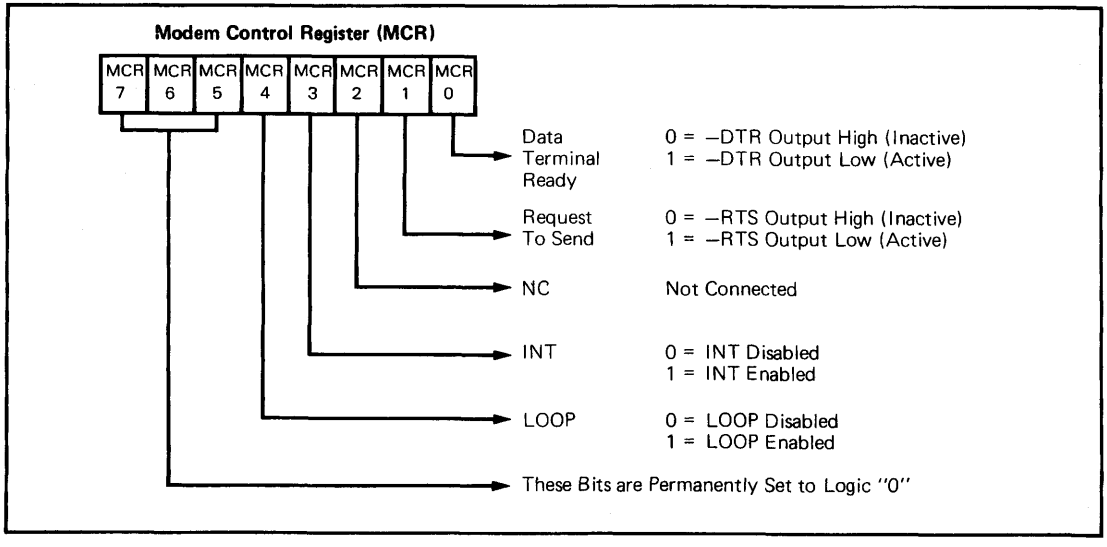


Figure 2. Modem Control Register

Table 4. Modem Status Register Bits

MSR Bit	Mnemonic	Description
MSR (1)	DDSR	Delta Data Set Ready
MSR (2)	TERI	Trailing Edge of Ring Indicator
MSR (0)	DCTS	Delta Clear to Send
MSR (3)	DRLSD	Delta Data Carrier Detect
MSR (4)	$\overline{CTS}$	Clear To Send
MSR (5)	$\overline{DSR}$	Data Set Ready
MSR (6)	$\overline{RI}$	Ring Indicator
MSR (7)	$\overline{RLSD}$	Receiver Line Signal Detect

that the $\overline{DSR}$ input to the serial channel has changed state since the last time it was read by the CPU.

MSR (2) Trailing Edge of Ring Indicator (TERI): TERI indicates that the $\overline{RI}$ input to the serial channel has changed state from high to low since the last time it was read by the CPU. Low to high transitions on $\overline{RI0}$ do not activate TERI.

MSR (3) Delta Data Carrier Detect (DRSLD): DRSLD indicates that the $\overline{RSLD}$ input to the serial channel has changed state since the last time it was read by the CPU.

MSR (4) Clear to Send (CTS): Clear to Send (CTS) is the status of the $\overline{CTS}$ input from the modem indicating to the serial channel that the modem is ready to receive data from the serial channel's transmitter, output (SOUT). If the serial channel is in loop mode [MSR (4) = 1]. MSR (4) is equivalent to $\overline{RTS}$ in the MCR.

MSR (5) Data Set Ready (DSR): Data Set Ready (DSR) is a status of the $\overline{DSR}$ input from the modem to the serial channel which indicates that the modem is ready to provide received data to the serial channel receiver circuitry. If the channel is in the loop mode [MCR (4) = 1], MSR (5) is equivalent to DTR in the MCR.

MSR (6) Ring Indicator: Indicates the status to the RI input (pin 39). If the channel is in the loop mode [MCR (4) = 1], MSR (6) is not connected in the MCR.

MSR (7) Receive Line Signal Detect: Receive Line Signal Detect indicates the status of the Receive Line Signal Detect ($\overline{RLSD}$) input. If the channel is in the loop mode [MCR (4) = 1], MSR (4) is equivalent to OUT2 of the MCR.

The modem status inputs ($\overline{RI}$, $\overline{RLSD}$, $\overline{DSR}$, and $\overline{CTS}$) reflect the modem input lines with any change of status. Reading the MSR register will clear the delta modem status indications but has no effect on the status bits. The status bits reflect the state of the input pins regardless of the mask control signals. If a DCTS, DDSR, TERI, or DRLSD are true, and a state change occurs during a read operation ($\overline{DISTR}$), the state change is not indicated in the MSR. If DCTS, DDSR, TERI, or DRLSD are false, and a state change occurs during a read operation, the state change is indicated after the read operation.

For LSR and MSR, the setting of status bits is inhibited during status register read $\overline{DISTR}$ operations. If a status condition is generated during a read DISTR operation, the status bit is not set until the trailing edge of the read $\overline{DISTR}$.

If a status bit is set during a read $\overline{DISTR}$ operation, and the same status condition occurs, that status bit will be cleared at the trailing edge of the read $\overline{DISTR}$ instead of being set again.

The UM82C451 serial channel contains a programmable Baud Rate Generator (BRG) that divides the clock (DC to 3.1 MHz) by any divisor from 1 to $2^{16}-1$ (see also BRG description). The output frequency of the Baud Generator is 16X the data rate [divisor # = clock + (baud rate x 16)]. Two 8-bit divisor latch registers store the divisor in a 16-bit binary format. These Divisor Latch registers must be loaded during initialization. Upon loading either of the Divisor latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load.

The receiver circuitry in each serial channel of the UM82C451 is programmable for 5, 6, 7, or 8 data bits per character. For words of less than 8 bits, the data is right justified to the least significant bit LSB = Data Bit 0 [RBR (0)]. Data Bit 0 of a data word [RBR (0)] is the first data bit received. The unused bits in a character less than 8 bits are output low to the parallel output by the serial channel.

Received data at the SIN input pin is shifted into the Receiver Shift Register by the 16X clock provided at the RCLK input. This clock is synchronized to the incoming data based on the position of the start bit. When a complete character is shifted into the Receiver Shift Register, the assembled data bits are parallel loaded into the Receiver Buffer Register. The DR flag in the LSR register is set.

Double buffering of the received data permits continuous reception of data without losing received data. While the Receiver Shift Register is shifting a new character into the serial channel, the Receiver Buffer Register is holding a previously received character for the CPU to read. Failure to read the data in the RBR before complete reception of the next character results in the loss of the data in the Receiver Register. The OE flag in the LSR register indicates the overrun condition.

RBR Bits 0 thru 7:

RBR (0)	Data Bit 0
RBR (1)	Data Bit 1
RBR (2)	Data Bit 2
RBR (3)	Data Bit 3

RBR (4)	Data Bit 4
RBR (5)	Data Bit 5
RBR (6)	Data Bit 6
RBR (7)	Data Bit 7

The Transmitter Holding Register (THR) holds parallel data from the data bus (D0-D7) until the Transmitter Shift Register is empty and ready to accept a new character for transmission. The transmitter and receiver word length and number of stop bits are the same. If the character is less than eight bits, unused bits at the microprocessor data bus are ignored by the transmitter.

Data Bit 0 [THR (0)] is the first serial data bit transmitted. The THRE flag [LSR (5)] reflects the status of the THR. The TEMT flag [LSR (5)] indicates if both the THR and TSR are empty.

THR Bits 0 thru 7

THR (0)	Data Bit 0
THR (1)	Data Bit 1
THR (2)	Data Bit 2
THR (3)	Data Bit 3
THR (4)	Data Bit 4
THR (5)	Data Bit 5
THR (6)	Data Bit 6
THR (7)	Data Bit 7

The Scratchpad Register is an 8-bit Read/Write register that has no effect on either channel in the UM82C451. It is intended to be used by the programmer to hold data temporarily.

SCR Bits 0 thru 7

SCR (0)	Data Bit 0
SCR (1)	Data Bit 1
SCR (2)	Data Bit 2
SCR (3)	Data Bit 3
SCR (4)	Data Bit 4
SCR (5)	Data Bit 5
SCR (6)	Data Bit 6
SCR (7)	Data Bit 7

Interrupts

The Interrupt Identification Register (IIR) in the serial channel of the UM82C451 has interrupt capability for interfacing to current microprocessors. In order to minimize software overhead during data character transfers, the serial channel prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows:

1. Receiver Line Status (priority 1)
2. Received Data Ready (priority 2)
3. Transmitter Holding Register Empty (priority 3)
4. Modem Status (priority 4)

Information indicating that a prioritized interrupt is pending and the type of interrupt is stored in the interrupt Identification Register (IIR). When addressed during chip select time, the IIR indicates the highest priority interrupt pending. No other interrupts are acknowledged until the interrupt is serviced by the CPU. The logic equivalent of the interrupt control circuit is shown in Figure 3. The contents of the IIR are indicated in Table 5 and are described below.

IIR (0): IIR (0) can be used in either a hard-wired prioritized or polled environment to indicate whether an interrupt is pending. When IIR (0) is low, an interrupt is pending, and IIR contents may be used as a pointer to the appropriate interrupt service routine. When IIR (0) is high, no interrupt is pending.

IIR (1) and IIR (2) are used to identify the highest priority interrupt pending as indicated in Table 5.

IIR (3)-IIR (7): These five bits of the IIR are logic 0.

The Interrupt Enable Register (IER) is a Write register used to independently enable the four serial channel interupts which activate the interrupt (INTRPT) output. All interrupts are disabled by resetting IER (0)-IER (3) of the Interrupt Enable Register. Interrupts are enabled by setting the appropriate bits of the IER high. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers. The content of the Interrupt Enable Register is described in Table 6 and below.

IER (0): When programmed high [IER (0) = Logic 1], IER (0) enables Received Data Available Interrupt.

IER (1): When programmed high [IER (1) = Logic 1], IER (1) enables the Transmitter Holding Register Empty interrupt.

IER (2): When programmed high [IER (2) = Logic 1], IER (2) enables the Receiver Line Status interrupt.

IER (3): When programmed high [IER (3) = Logic 1], IER (3) enables the Modem Status Interrupt.

IER (4)-IER (7): These four bits of the IER are logic 0.

Transmitter

The serial transmitter section consists of a Transmitter Holding Register (THR), Transmitter Shift Register (TSR), and associated control logic. The Transmitter Holding Register Empty (THRE) and Transmitter Shift Register Empty (TEMT) are two bits in the Line Status Register which indicate the status of THR and TSR.

Table 5. Interrupt Identification Register

Interrupt Identification				Interrupt Set and Reset Functions		
Bit 2	**Bit 1**	**Bit 0**	**Priority Level**	**Interrupt Flag**	**Interrupt Source**	**Interrupt Reset Control**
X	X	1		None	None	
1	1	0	First	Receiver Line Status	OE, PE FE, or BI	LSR Read
1	0	0	Second	Received Data Available	Received Data Available	RBR Read
0	1	0	Third	THRE	THRE	IIR Read if THRE is the Interrupt Source or THR Write
0	0	0	Fourth	Modem Status	–CTS, –DSR –RI, –RSLD	MSR Read

X = Not Defined.

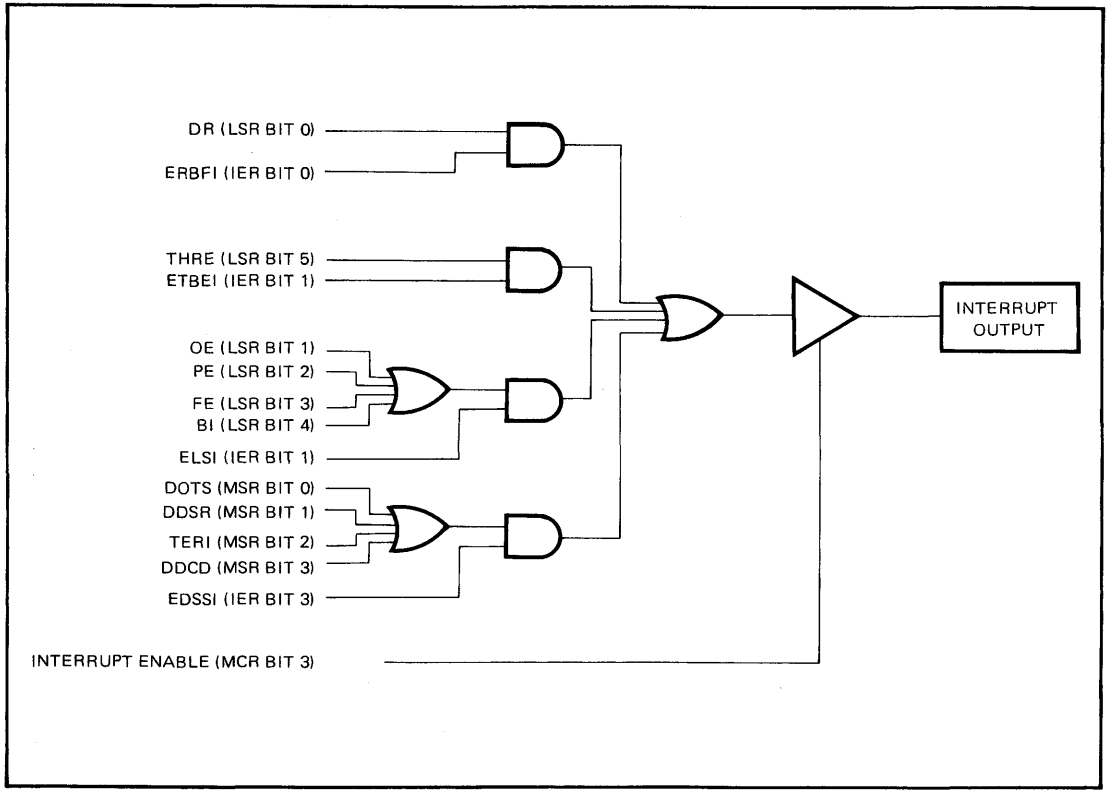


Figure 3. Interrupt Control Logic

Table 6. Serial Channel Accessible Registers

Register Mnemonic	Register Bit Number							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
RBR (Read Only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)*
THR (Write Only)	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
IER	0	0	0	0	(EDSSI) Enable Modem Status Interrupt	(ELSI) Enable Receiver Line Status Interrupt	(ETBEI) Enable Transmitter Holding Register Empty Interrupt	(ERBFI) Enable Received Data Available Interrupt
IIR (Read Only)	0	0	0	0	0	Interrupt ID Bit (1)	Interrupt ID Bit (0)	"0" 1F Interrupt Pending
LCR	(DLAB) Divisor Latch Access Bit	Set Break	Stick Parity	(EPS) Even Parity Select	(PEN) Parity Enable	(STB) Number of Stop Bits	(WLSB1) Word Length Select Bit 1	(WLSB0) Word Length Select Bit 0
MCR	0	0	0	Loop	Out 2	Out 1	(RTS) Request To Send	(DTR) Data Terminal Ready
LSR	0	(TEMT) Transmitter Empty	(THRE) Transmitter Holding Register Empty	(BI) Break Interrupt	(FE) Framing Error	(PE) Parity Error	(OE) Overrun Error	(DR) Data Ready
MSR	(DCD) Data Carrier Detect	(RI) Ring Indicator	(DSR) Data Ready Set	(CTS) Clear to Send	(DRSLD) Delta Receive Line Signal Detect	(TERI) Trailing Edge Ring Indicator	(DDSR) Delta Data Set Ready	(DCTS) Delta Clear to Send
SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

*LSB Data Bit 0 is the first bit transmitted or received.

To transmit a 5 to 8-bit word, the word is written through D0-D7 to the THR. The microprocessor should perform a write operation only if THRE is high. The THRE is set high when the word is automatically transferred from the THR to the TSR during the transmission of the start bit.

When the transmitter is idle, THRE and TEMT are high. The last word written causes THRE to be reset to 0. After the transfer, THRE returns high. TEMT remains low for at least the duration of the transmission of the data word. If a second character is transmitted to the THR, the THRE is reset low. Since the data word cannot be transferred from the THR to the TSR until the TSR is empty, THRE remains low until the TSR has completed sending the word. When the last word has been transmitted out of the TSR, TEMT is set high. THRE is set high one THR to TSE transfer time later.

Receiver

Serial asynchronous data is input into the SIN pin. The idle state of the line providing the input into SIN is high. A start bit detect circuit continually searches for a high to low transition from the idle state. When the transition is detected, a counter is reset, and counts the 16X clock to 7½, which is the center of the start bit. The start bit is valid if the SIN is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the SIN input.

The Line Control Register determines the number of data bits in a character (LCR (0), LCR (1)), number of stop bits LCR (2), if parity is used LCR (3), and the polarity of parity LCR (4). If Status for the receiver is provided in the Line Status Register to the Receiver Buffer Register when the Data Received indication in LSR (0) is set high, the CPU reads the Receiver Buffer Register through D0-D7. This read resets LSR (0). If D0-D7 are not read prior to a new character transfer from the RSR to the RBR, the overrun error status indication is set in LSR (1). The parity check tests for even or odd parity on the parity bit, which precedes the first stop bit. If there is a parity error, the parity error is set in LSR (2). There is circuitry which tests whether the stop bit is high. If it is not, a framing error indication is generated in LSR (3).

The center of the start bit is defined as clock count 7½. If the data into SIN is a symmetrical square wave, the center of the data cells will occur within ±3.125% of the actual center, providing an error margin of 46.875%. The start bit can begin as much as one 16X clock cycle prior to being detected.

Baud Rate Generator (BRG)

The BRG generates the clocking for the UART function, providing standard ANSI/CCITT bit rates. The oscillator driving the BRG is provided by an external clock into CLK.

The data rate is determined by the Divisor Latch registers DLL and DLM and the external frequency. The bit rate is selected by programming the two divisor latches, Divisor Latch Most Significant Byte and Divisor Latch Least Significant Byte. Setting DLL = 1 and DLM = 0 selects the divisor to divide by 1 (divide by 1 gives the maximum baud rate for a given input frequency at the CLK input).

The BRG can use any of three different popular frequencies to provide standard baud rates. These frequencies are 1.8432 MHz, 2.4576 MHz, and 3.072 MHz. With these frequencies, standard bit rates from 50 to 38.5 kbps are available. Tables 7, 8, and 9 illustrate the divisors needed to obtain standard rates using these three crystal frequencies.

Reset

After power up, the UM82C451 $\overline{\text{RESET}}$ input should be held low for 500 ns to reset the UM82C451 circuits to an idle mode until initialization. A low on $\overline{\text{RESET}}$ causes the following:

1. Initializes the transmitter and receiver internal clock counters.
2. Clears the Line Status Register (LSR), except for Transmitter Shift Register Empty (TEMT) and Transmit Holding Register Empty (THRE), which are set. The Modem Control Register (MCR) is also cleared. All of the discrete lines, memory elements and miscellaneous logic associated with these register bits are also cleared or turned off. The Line Control Register (LCR), Divisor Latches, Receiver Buffer Register, Transmitter Buffer Register are not affected.

Following removal of the reset condition (Reset high), the UM82C451 remains in the idle mode until programmed.

A hardware reset of the UM82C451 sets the THRE and TEMT status bit in the LSR. When interrupts are subsequently enabled, an interrupt occurs due to THRE.

A summary of the effect of a reset on the UM82C451 is given in Table 10.

Programming

Each serial channel of the UM82C451 is programmed by the control registers LCR, IER, DLL and DLM, and MCR. These control words define the character length, number of stop bits, parity, baud rate, and modem interface. While the control register can be written in any order, the IER should be written to last because it controls the interrupt enables. Once a serial channel is programmed and operational, these registers can be updated any time the UM82C451 serial channel is not transmitting or receiving data.

The control signals required to access each serial channel's internal registers are shown below.

Software Reset

A software reset of the serial channel is a useful method for returning to a completely known state without a system reset. Such a reset consists of writing to the LCR, Divisor Latches, and MCR registers. The LSR and RBR registers should be read prior to enabling interrupts in order to clear out any residual data or status bits which may be invalid for subsequent operation.

Clock Input Operation

The maximum input frequency of the external clock of the UM82C451 is 3.1 MHz.

Table 7. Baud Rates (1.8432 MHz Clock)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	2304	–
75	1536	–
110	1047	0.026
134.5	857	0.058
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.69
2400	48	–
3600	32	–
4800	24	–
7200	16	–
9600	12	–
19200	6	–
38400	3	–
56000	2	2.86

Table 8. Baud Rates (2.4576 MHz Clock)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	3072	–
75	2048	–
110	1396	0.026
134.5	1142	0.0007
150	1024	–
300	512	–
600	256	–
1200	128	–
1800	85	0.392
2000	77	0.260
2400	64	–
3600	43	0.775
4800	32	–
7200	21	1.587
9600	16	–
19200	8	–
38400	4	–

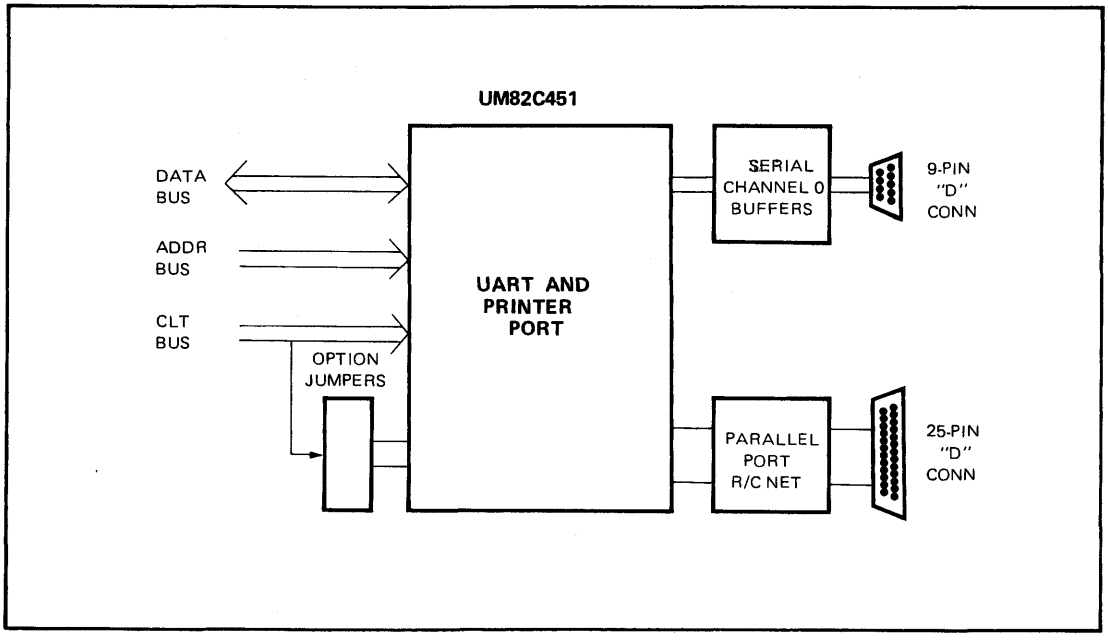
Table 9. Baud Rates (3.072 MHz Clock)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	3840	–
75	2560	–
110	1745	0.026
134.5	1428	0.034
150	1280	–
300	640	–
600	320	–
1200	160	–
1800	107	0.312
2000	96	–
2400	80	–
3600	53	0.628
4800	40	–
7200	27	1.23
9600	20	–
19200	10	–
38400	5	–

Table 10. Reset Control of Register and Pinout Signals

Register/Signal	Reset Control	Reset Status
Interrupt Enable Register	Reset	All Bits low
Interrupt Identification Register	Reset	Bit 0 is high and Bits 1-7 are low
Line Control Register	Reset	All Bits low
Modem Control Register	Reset	All Bits low
Line Status Register	Reset	Bits 5, 6 are high, others are low
Modem Status Register	Reset	Bits 0-3 are low, Bits 4-7 are input signals
SOUT0,	Reset	High
$\overline{RTS0}$, $\overline{DTR0}$	Reset	High
INT0, INT2	Reset	High-Impedance
$\overline{STB}$, $\overline{AFD}$, $\overline{SLIN}$,	Reset	High
$\overline{INIT}$	Reset	Low

Device Application



Functional Description:

Parallel Port Register

The UM82C451's parallel port interfaces the device to a Centronics-style printer. When Chip Select 2 ($\overline{CS2}$) is low, ($\overline{IOR}$) and write ($\overline{IOW}$) pins are as shown. The Read Data Register allows the microprocessor to read the information on the parallel bus. The Read Status Register allows the microprocessor to read the status of the printer in the five most significant bits. The status bits are Printer Busy ($\overline{BUSY}$), acknowledge ($\overline{ACK}$), which is a handshake function, Paper Empty (PE), Printer Selected (SLCT), and Error. ($\overline{ERROR}$). The Read Control Register allows the state of the control lines to be read. The Write Control Register sets the state of the control lines.

They are Interrupt Enable (IRQ ENB), Select In ($\overline{SLIN}$), Initialize the Printer ($\overline{INIT}$), Autofeed the Paper ($\overline{AUTOFD}$), and Strobe ($\overline{STROBE}$), which informs the printer of the presence of a valid byte on the parallel bus. The Write Data Register allows the microprocessor to write a byte to the parallel bus.

The parallel port is completely compatible with the parallel port implementation used in the IBM Serial/Parallel Adaptor.

Table 12. Parallel Port Register Select

Control Pins					Register Selected
–IOR	–IOW	–CS2	A1	A0	
0	1	0	0	0	Read Data
0	1	0	0	1	Read Status
0	1	0	1	0	Read Control
0	1	0	1	1	Invalid
1	0	0	0	0	Write Data
1	0	0	0	1	Invalid
1	0	0	1	0	Write Control
1	0	0	1	1	Invalid

Table 11. Parallel Port Registers

Register	Register Bits							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Read Status	$\overline{BUSY}$	$\overline{ACK}$	PE	SLCT	$\overline{ERROR}$	1	1	1
Read Control	1	1	1	IRQ ENB	SLIN	$\overline{INIT}$	$\overline{AUTOFD}$	$\overline{STROBE}$
Write Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Write Control	1	1	1	IRQ ENB	$\overline{SLIN}$	$\overline{INIT}$	$\overline{AUTOFD}$	$\overline{STROBE}$

AC Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$ (Notes 1, 5)

Serial

Symbol	Parameter	Min	Max	Unit	Conditions
t_{DIW}	$\overline{DISTR}$ Strobe Width	125		ns	
RC	Read Cycle	360		ns	
t_{DDD}	Delay from $\overline{DISTR}$ to Data		125	ns	100 pF Load
t_{HZ}	$\overline{DISTR}$ to Floating Data Delay	0	100	ns	100 pF Load, Note 4
t_{DOW}	$\overline{DOSTR}$ Strobe Width	100		ns	
WC	Write Cycle	360		ns	
t_{DS}	Data Setup Time	40		ns	
t_{DH}	Data Hold Time	40		ns	
t_{RA}	Address Hold Time from $\overline{DISTR}$	20		ns	Note 2
t_{RCS}	Chip Select Hold Time from $\overline{DISTR}$	20		ns	Note 2
tAR	$\overline{DISTR}$ Delay from Address	60		ns	Note 2

AC Characteristics (Continued)

Symbol	Parameter	Min	Max	Unit	Conditions
t_{CSR}	$\overline{DISTR}$ Delay from Chip Select	50		ns	Note 2
t_{WA}	Address Hold Time from $\overline{DOSTR}$	20		ns	Note 2
t_{WCS}	Chip Select Hold Time from $\overline{DOSTR}$	20		ns	Note 2
t_{AW}	$\overline{DOSTR}$ Delay from Address	60		ns	Note 2
t_{CSW}	$\overline{DOSTR}$ Delay from Select	50		ns	Note 2
t_{RW}	Reset Pulse Width	5		μs	
t_{XH}	Duration of Clock High Pulse	140		ns	External Clock
t_{XL}	Duration of Clock Low Pulse	140		ns	External Clock
Transmitter					
t_{HR1}	Delay from Rising Edge of $\overline{DOSTR}$ (WR THR) To Reset Interrupt		175	ns	100 pF Load
t_{IRS}	Delay from Initial INTR Reset to Transmit Start	8	24	CLK cycles	Note 3
t_{SI}	Delay from Initial Write to Interrupt	16	32	CLK cycles	Note 3
t_{STI}	Delay from Stop to Interrupt (THRE)	8	8	CLK cycles	Note 3
t_{IR}	Delay from $\overline{DISTR}$ (RD IIR) to Reset Interrupt (THRE)		250	ns	100 pF Load
Modem Control					
t_{MDO}	Delay from $\overline{DISTR}$ (WR MCR) to Output		200	ns	100 pF Load
t_{SIM}	Delay to Set Interrupt from MODEM Input		200	ns	100 pF Load
t_{RIM}	Delay to Reset Interrupt from $\overline{DISTR}$ (RS MSR)		250	ns	100 pF Load
Receiver					
t_{SINT}	Delay from Stop to Set Interrupt	1	1	CLK cycles	Note 3
t_{RINT}	Delay from $\overline{DOSTR}$ (RD RBR/RDLSR) to Reset Interrupt		1	μs	100 pF Load

Parallel Port

WRITE

Symbol	Parameter	Min.	Max.	Unit	
T_{WW}	Write Pulse Width	200	–	ns	
T_{AW}	Address to $\overline{IOW}$ Set-up Time	20	–	ns	
T_{WA}	Address Hold Time after $\overline{IOW}$	20	–	ns	
T_{DW}	Data to $\overline{IOW}$ Set-up Time	70	–	ns	
T_{WD}	Data Hold Time after $\overline{IOW}$	30	–	ns	
T_{WOL}	$\overline{IOW}$ = 1 to Data Latched	–	90	ns	

READ

Symbol	Parameter	Min.	Max.	Unit
T_{RR}	Read Pulse Width	300	–	ns
T_{AR}	Address to $\overline{IOR}$ Set-up Time	20	–	ns
T_{RA}	Address Hold Time after $\overline{IOR}$	20	–	ns
T_{PR}	Printer Bus to $\overline{IOR}$ Set-up Time	0	–	ns
T_{RP}	Printer Bus Hold Time after $\overline{IOR}$	0	–	ns
T_{RDS}	$\overline{IOR}$ to D0 – D7 Output	–	70	ns
T_{RDR}	D0 – D7 Released after $\overline{IOR}$	–	30	ns

*Note: When the CPU reads the printer's status, output data may change if the printer signals are unstable.

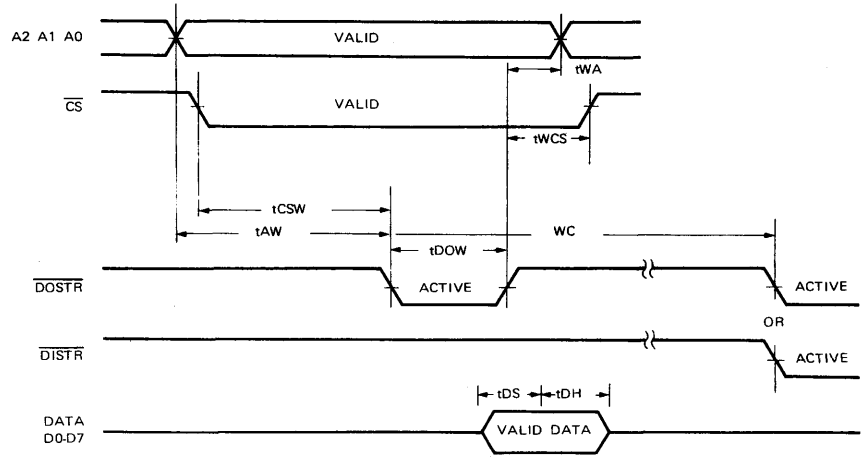
OTHERS

Symbol	Parameter	Min.	Max.	Unit
T_{RSW}	Reset Pulse Width	40	–	ns
T_{RSCH}	Reset to Control Bus = 1 ($\overline{STROB}$, $\overline{AUTOFD}$, $\overline{SLCT}$) Propagation Delay	–	90	ns
T_{RSIN1}	Reset to Control Bus $\overline{INIT}$ = 0 Propagation Delay	–	60	ns
T_{ID}	$\overline{ACK}$ to IRQ Propagation Delay	–	45	ns

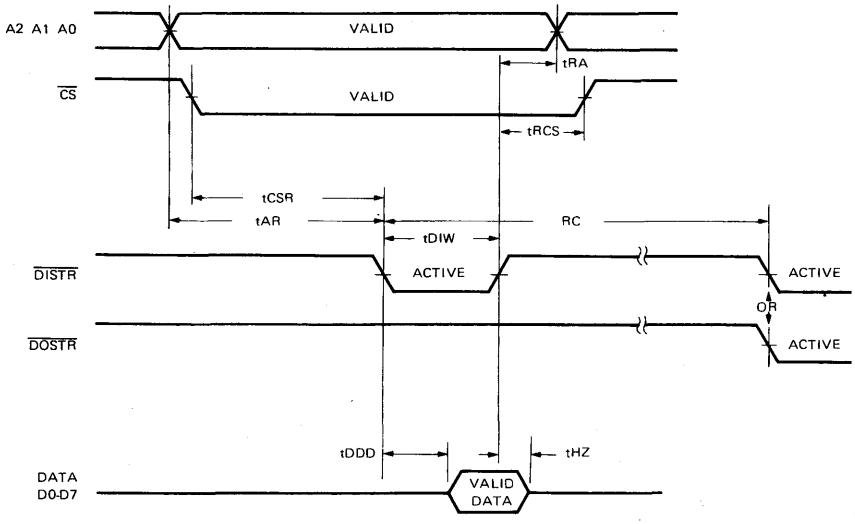
Notes: 1. All timing specifications apply to pins to both serial channels (e. g. Ri refers to both R10 and R11).
2. The internal address strobe is always active.
3. RCLK = t_{XH} and t_{XL}.
4. Charge and discharge time is determined by VOL, VOH, and the external loading.
5. All timings are referenced to valid 0 and valid 1 (see AC TEST POINTS).

Serial Port Timing:

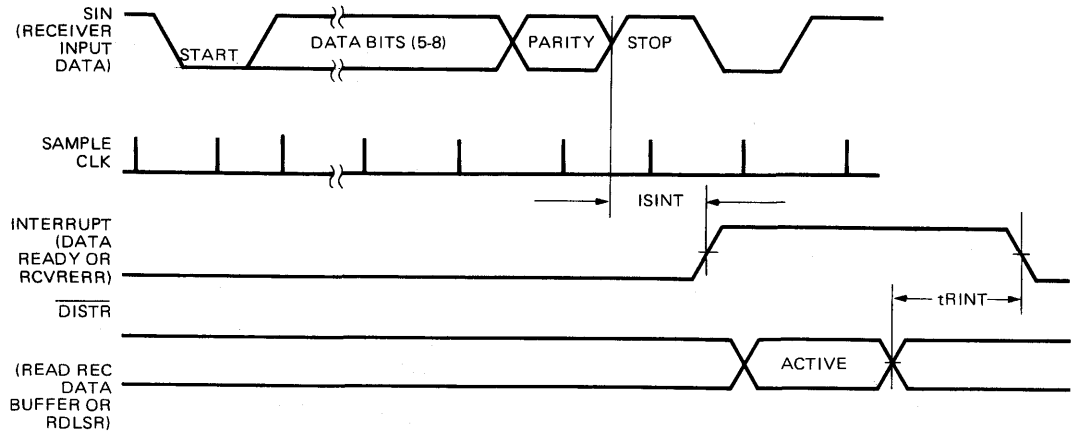
Write Cycle Timing



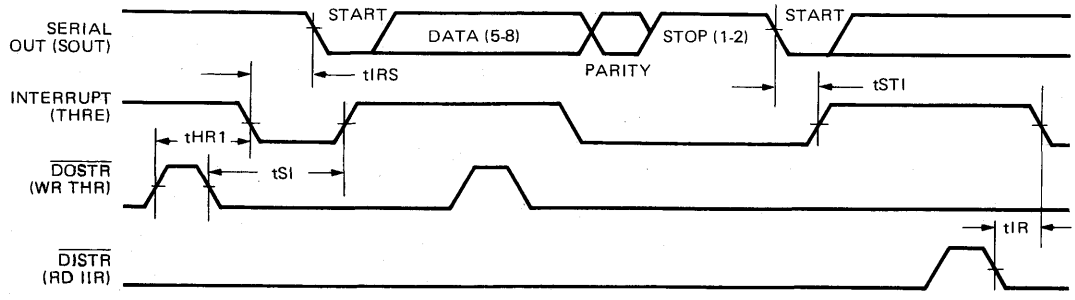
Read Cycle Timing



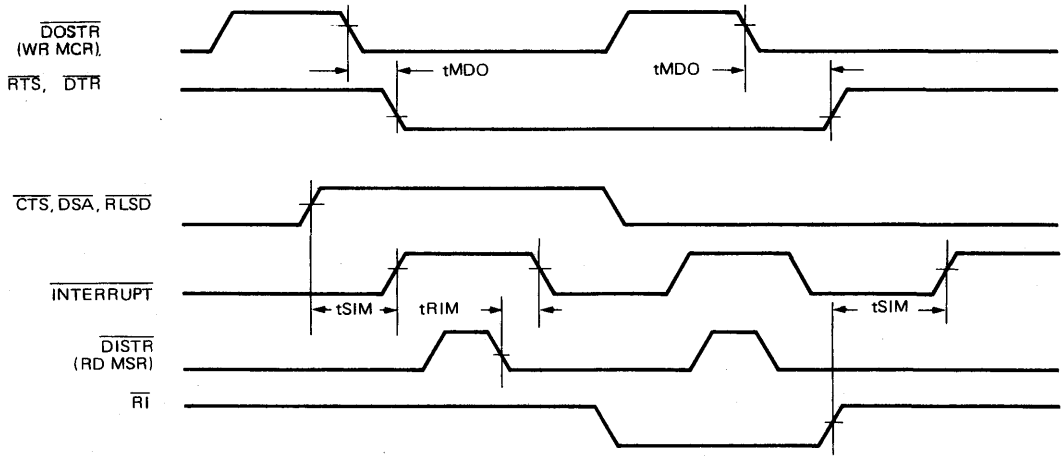
Receiver Timing



Transmitter Timing

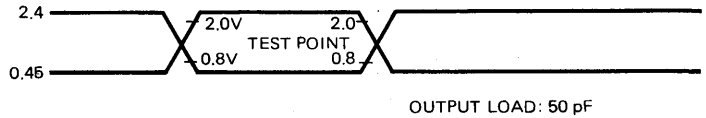


Modem Timing



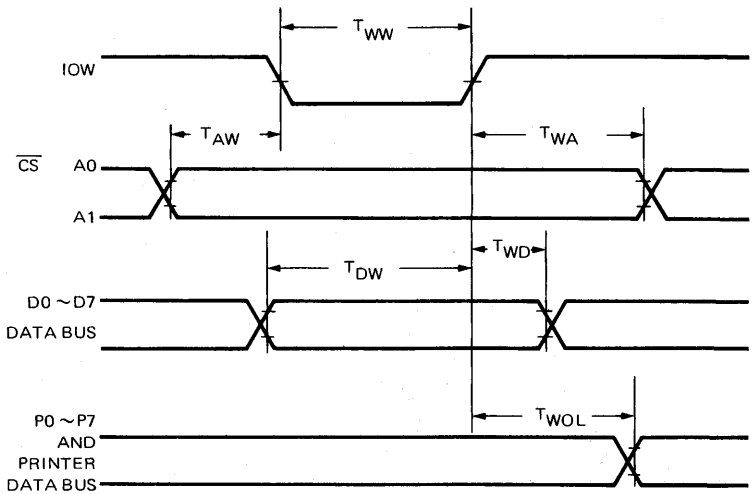
Parallel Port Timing:

AC Testing Input Waveform



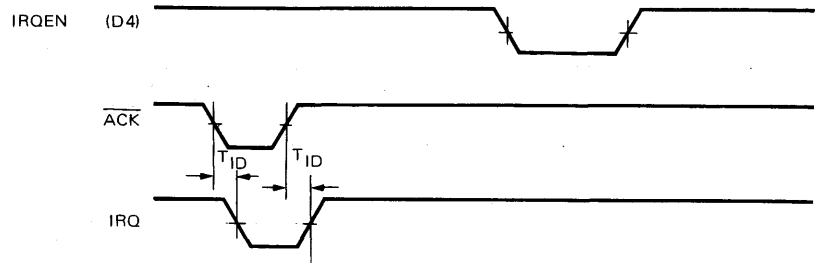
OUTPUT LOAD: 50 pF

Write Cycle Waveform

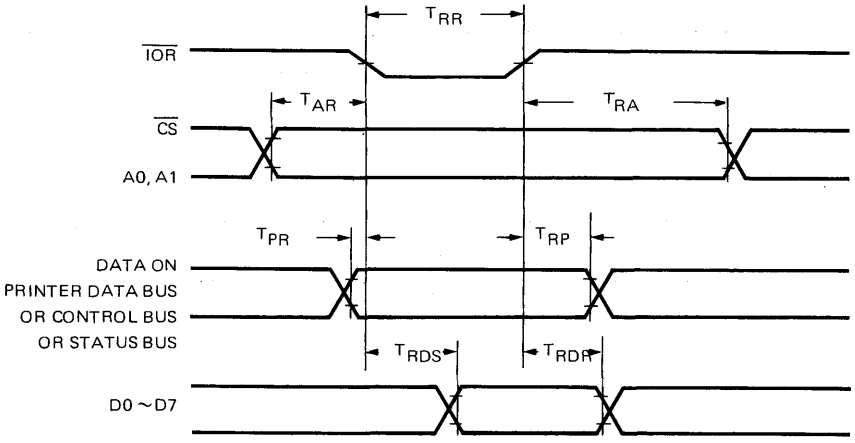


I/O And Peripherals

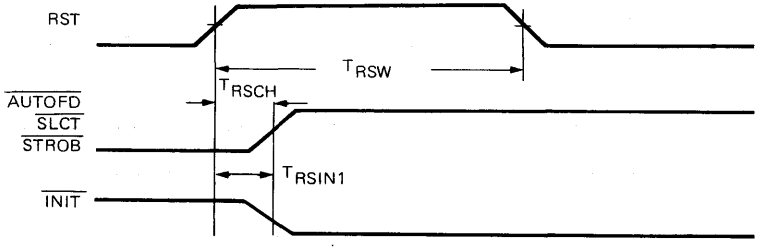
Interrupt Request Waveform



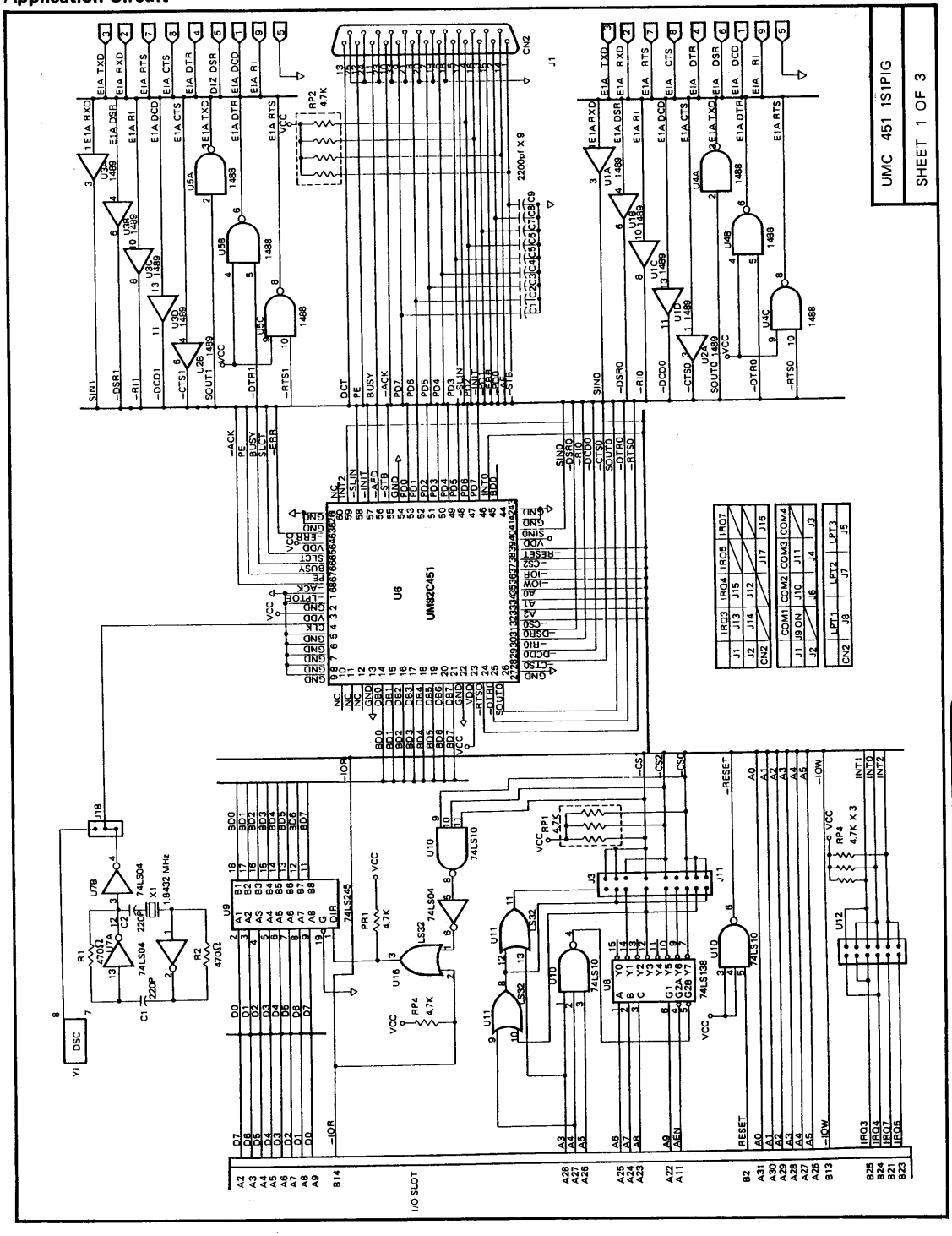
Read Cycle Waveform



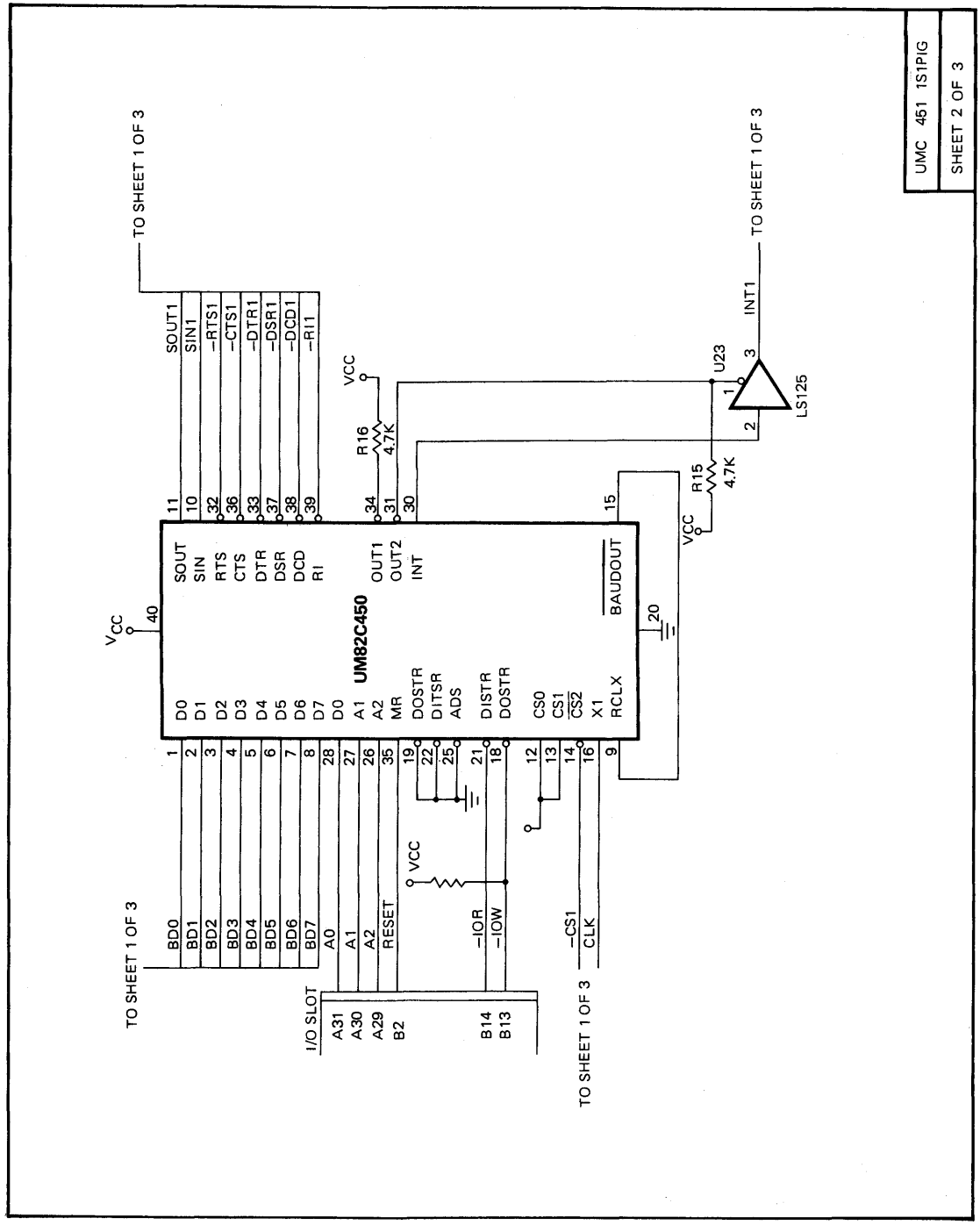
Reset Waveform



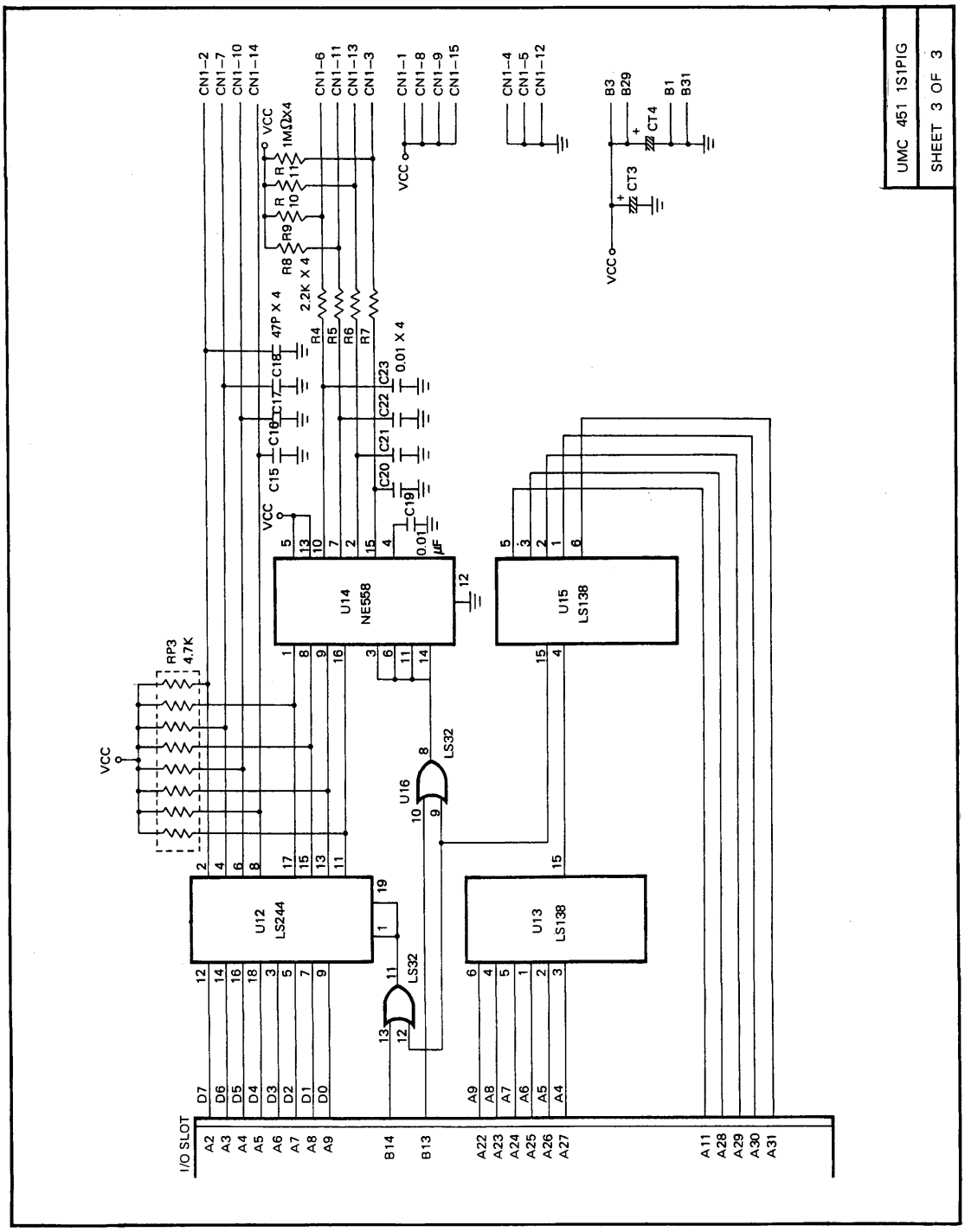
Application Circuit



Application Circuit



Application Circuit



Absolute Maximum Ratings *

Ambient Operating Temperature . . . . . −10°C to +70°C
Storage Temperature . . . . . −65°C to +150°C
Supply Voltage to Ground
Potential . . . . . −0.5V to V_{CC} + 0.3V
Applied Output Voltage . . . . . −0.5V to V_{CC} + 0.3V
Applied Input Voltage . . . . . −0.5V to + 7.0V
Power Dissipation . . . . . 500 mW

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 5%)

Symbol	Parameter	Min.	Max.	Unit	Conditions
V_{ILX}	Clock Input Low Voltage	−0.5	0.8	V	
V_{IHX}	Clock Input High Voltage	2.0	V_{CC}	V	
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 4.0 mA on DB0-DB7, I_{OL} = 12 mA on PD0-PD7, I_{OL} = 10 mA on −INIT, −AFD, −STB, and −SLIN (see Note 1), I_{OL} = 2.0 mA on all other outputs
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −0.4 mA on DB0-DB7, I_{OH} = −2.0 mA on PD0-PD7, I_{OH} = −0.2 mA on −INIT, −AFD, −STB, and −SLIN, I_{OH} = −0.2 mA on all other outputs
I_{CC}	Power Supply Current		40	mA	V_{CC} = 5.25 V, No loads on SIN0, 1; −DISTR0, 1; −RLSD0, 1; −CTS0, 1; −RI0, −RI1 = 2.0V. Other = 0.8V, Baud rate generator = 4 MHz. Baud rate = 56K
I_{IL}	Input Leakage		10	μA	V_{CC} = 5.25 V, GND = 0V All other pins floating
I_{CL}	Clock Leakage		10	μA	V_{IN} = 0 V, 5.25V
I_{OZ}	3-State Leakage		20	μA	V_{CC} = 5.25V, GND = 0V, VOUT = 0V, 5.25V 1) Chip deselected 2) Chip and write mode selected
V_{IL} (RES)	Reset Schmitt V_{IL}		0.8	V	
V_{IH} (RES)	Reset Schmitt V_{IH}	2.0		V	

Note 1. $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$, and $\overline{SLIN}$ are open collector output pins that each have an internal pull-up resistor (2.5 kΩ 3.5 kΩ) to V_{CC}. This will generate a maximum of 2.0 mA of internal I_{OL}. In addition to this internal current, each pin will sink at least 10 mA, while maintaining the V_{OL} specification of 0.4V Max.

UMC

UM82C452

Single Chip Multi-I/O

Features

- IBM PC/AT Compatible
- Centronics printer interface
- Dual channel version of UM82C450
- Independent control of transmit, receive, line status and modem status interrupts on each channel
- Individual modem control signals for each channel
- Programmable serial interface characteristics for each channel:
  5-, 6-, 7- or 8-bit characters
  Even-, odd-or no-parity bit generation and detection
  1, 1 1/2 or 2 stop bit generation
- Three-state TTL drive capabilities for bidirectional data bus and control bus for each channel

Description

The UM82C452 is an enhanced dual channel version of the popular UM82C450 asynchronous communication element (ACE). The device services two serial input/output interfaces simultaneously in microcomputer or microprocessor based systems. Each channel performs serial-to-parallel conversion on data characters received from peripheral devices or modems, and parallel-to-serial conversion on data characters transmitted by the CPU. The complete status of each channel of the dual ACE can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the transfer operations being performed, and error conditions.

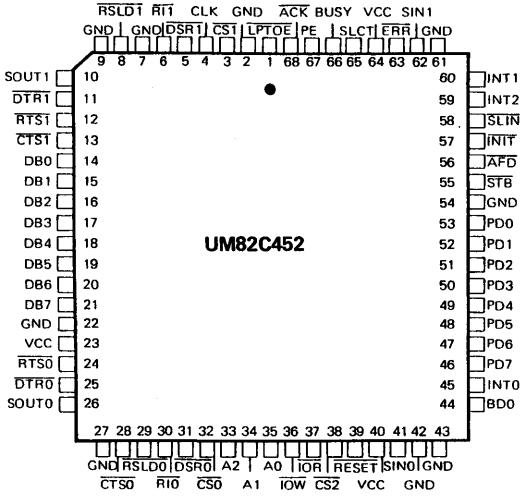
In addition to its dual communications interface capabilities, the UM82C452 provides the user with a fully bidirectional parallel data port that fully supports the parallel Centronics type printer. This port allows data transmitted by the CPU to be printed. The parallel port, together with the two serial ports, provide IBM PC/AT compatible computers with a single device to serve the three functions.

A programmable baud rate generator is included that can divide the timing reference clock input by a divisor between 1 and $(2^{16}-1)$.

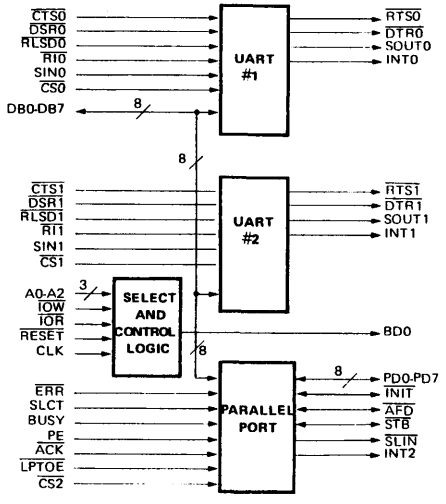
The UM82C452 is packaged in a 68-pin plastic leaded chip carrier.

I/O And Peripherals

Pin Configuration



Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description
37	$\overline{IOR}$	I	Input/Output Read strobe: This is an active Low input signal used to cause the selected channel to output data to data bus (DB0-DB7).
36	$\overline{IOW}$	I	Input/Output Write strobe: This is an active Low input signal used to cause data input from data bus (DB0-DB7) to the channel selected.
33-35	A2-A0	I	Address lines A2-A0: The address lines are used to select the internal register in selected channels during the CPU cycle.
32, 3, 38	$\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$	I	Chip Selects: Each chip select input acts as an enable of each channel during read and write. $\overline{CS0}$ selects Serial Channel 0, $\overline{CS1}$ selects Serial Channel 1 and $\overline{CS2}$ selects Parallel Port.
44	BDO	O	Bus Buffer Output: This active high output is asserted when any channel is selected. This output can be used to control the system bus driver device (74LS245).
14-21	DB0-DB7	I/O	Data Bit DB0-DB7: The data bus provides eight three-state I/O lines for the transfer of data, control and status information between CPU and UM82C452. These lines are normally in a high-impedance state except during read operation. D0 is the least significant bit (LSB) and is the first serial bit to be transmitted or received.
39	$\overline{RESET}$	I	Reset: When low, the reset input forces the UM82C452 into an idle state in which all serial data activities are suspended. The Registers and signals of the UM82C452 are all cleared to the state as indicated in Table 1.
26, 10	SOUT0, SOUT1	O	Serial Data Outputs: These lines are the serial data outputs of UARTs, used to transmit serial data to the communication link. Each SOUT is held in marking (logic 1) state when the transmitter is disabled,reset, the Transmitter Register is empty, or when in the loop mode.
41, 62	SIN0, SIN1	I	Serial Data Inputs: These lines are used to receive serial data from the communication line or modem into the UARTs. Data on serial data inputs is disabled during loop mode.
24, 12	$\overline{RTS0}$, $\overline{RTS1}$	O	Request To Send Outputs: This signal is an active low output for each UART. When active, it informs the Modem or data set that the controller is ready to send data. This signal is set low by writing logic 1 to MCR (1) and reset to high by Reset.
25, 11	$\overline{DTR0}$, $\overline{DTR1}$	O	Data Terminal Ready Lines: This signal is an active low output for each UART. When active, it informs the modem or data set that the controller is ready to communicate. This signal is set low by writing logic 1 to MCR (0) and reset to high by Reset.

Pin Description (Continued)

Pin No.	Symbol	I/O	Description
28, 13	$\overline{CTS0}$, $\overline{CTS1}$	I	Clear to send Inputs: This signal is an active low input for each UART. The logic state of this signal is reflected in MSR (4) and any change of state in either $\overline{CTS}$ pin will set DCTS bit MSR (0) of each Modem Status Register. When active, it informs that the Modem or data set is ready to receive data.
31, 5	$\overline{DSR0}$ $\overline{DSR1}$	I	Data Set Ready: This signal is an active low input for each UART. The logic state of this signal is reflected in MSR (5) and any change of state in either $\overline{DSR}$ pin will set DDSR bit MSR (1) of each Modem Status Register. When active, it informs that the Modem or data set is ready to establish communication.
29,8	$\overline{RLSD0}$ $\overline{RLSD1}$	I	Receive Line Signal Detect: This is an active low input for each UART. The logic state of this signal is reflected in MSR (7) and any change of state in either $\overline{RLSD}$ pin will set DRLSD bit MSR (3) of each Modem Status Register. When active, it informs that the data carrier has been detected by Modem or data set.
30, 6	RI0 RI1	I	Ring Indicator: This signal is an active low input for each UART. The logic state of this signal is reflected in MSR (6) and TERI bit MSR (2) will be set when the state of either RI pin is changed from Low to high.
4	CLK	I	Clock Input: The external clock input from a crystal oscillator.
1	$\overline{LPTOE}$	I	Line Printer Output Enable: This input signal enables the data outputs of the parallel line printer when it is low. When it is high, the data pins of the line printer are held in a high-impedance state. This pin may be tied to ground for normal line printer operation.
53-46	PD0-PD7	O	Parallel Data Bus: This bus provides a byte-wide input or output port to the system. The eight lines are held in a high-impedance state when the port is not selected.
68	$\overline{ACK}$	I	Acknowledge: This signal goes low to indicate that the printer has already received a character and is ready to accept another.
67	PE	I	Paper Empty: This signal goes high when the line printer has run out of paper.
66	BUSY	I	Busy: This signal goes high when the line printer has a local operation in progress and cannot accept data.
65	SLCT	I	Selected: This signal goes high when the line printer has been selected.

Pin Description (Continued)

Pin No.	Symbol	I/O	Description
63	$\overline{ERR}$	I	Error: This signal goes low when the line printer has encountered an error condition.
58	$\overline{SLIN}$	I/O	Line Printer Select: This signal is used to select the printer when it is low.
57	$\overline{INIT}$	I/O	Line Printer Initialize: When this signal goes low, it will allow the line printer initialization routine to be started.
56	$\overline{AFD}$	I/O	Line Printer Autofeed: When this signal goes low, it will cause the printer to line-feed after a line is printed.
55	$\overline{STB}$	I/O	Line Printer Strobe: When this signal is low, it provides the line printer a signal to latch the data currently on the parallel port. This signal should keep low at least 0.5 μs to ensure the completion of data latch.
45, 60	INT0 INT1	O	Serial Channel Interrupts: Each Serial channel interrupt goes high when one of the following interrupts has an active condition and is enabled by the IER of its associated channel: Receiver Error Flag, Receiver Data Available, Transmitter Holding Register Empty, and Modem Status. The interrupt is reset to low upon appropriate service. This pin will be held in a high-impedance state if the MCR (3) of each associated channel is programmed low (logic 0).
59	INT2	O	Line Printer Interrupt: This interrupt goes low when ACK goes low. This signal is enabled by Bit 4 of the Printer Control Register and will be held in a high-impedance state if Bit 4 of the printer Control Register is programmed low.
23, 40, 64	V_{CC}	I	Power Supply: +5V
2,7,9,22, 27, 42,43,54,61	GND		Ground: 0V

Functional Description:

Serial Channel Registers:

Three types of internal registers are used in each serial channel of the UM82C452. They are used in the operation of the device, and are the control, status, and data registers. The control registers are the Baud Rate Select Register DLL (Divisor Latch LSB) and DLM (Divisor Latch MSB), Line Control Register. Interrupt Enable Register, and the Modem Control register. The status registers are the Line Status Registers and the Modem Status Register. The data registers are the Receiver Buffer Register and the Transmitter Holding Register. Address, Read, and Write inputs are used in conjunction with the Divisor Latch Access Bit (DLAB) in the Line Control Register LCR (7) to select the register to be written or read (see Table 1). Individual bits within these registers are referred to by the register mnemonic and the bit number in parenthesis. An example, LCR (7) refers to Line Control Register Bit 7.

The Transmitter Buffer Register and Receiver Buffer Register are data registers holding from five to eight bits of data. If less than eight data bits are transmitted, data is right justified to the LSB. Bit 0 of a data word is always the first serial data bit received and transmitted. The UM82C452 data registers are double-buffered so that read and write operations can be performed at the same time the UART is performing the parallel-to-serial and serial-to-parallel conversion.

The format of the data character is controlled by the Line Control Register. The contents of the LCR may be read, eliminating the need for separate storage of the line characteristics in system memory. The contents of the LCR are described below.

LCR (0) Word Length Select Bit 0 (WLS0)
LCR (1) Word Length Select Bit 1 (WLS1)
LCR (2) Stop Bit Select (STB)
LCR (3) Parity Enable (PEN)

Table 1. Serial Channel Internal Registers

DLAB	A2	A1	A0	Mnemonic	Register
0	0	0	0	RBR	Receiver Buffer Register (read only)
0	0	0	0	THR	Transmitter Holding Register (write only)
0	0	0	1	IER	Interrupt Enable Register
X	0	1	0	IIR	Interrupt Identification Register (read only)
X	0	1	1	LCR	Line Control Register
X	1	0	0	MCR	Modem Control Register
X	1	0	1	LSR	Line Status Register
X	1	1	0	MSR	Modem Status Register
X	1	1	1	SCR	Scratch Register
1	0	0	0	DLL	Divisor Latch (LSB)
1	0	0	1	DLM	Divisor Latch (MSB)

X = "Don't Care" 0 = Logic Low 1 = Logic High

Note: Serial Channel 0 is accessed when $\overline{CS0}$ is low; Serial Channel 1 is accessed when $\overline{CS1}$ is low. Selecting both channels simultaneously is an invalid condition.

LCR (4) Even Parity Select (EPS)
LCR (5) Stick Parity
LCR (6) Set Break
LCR (7) Divisor Latch Access Bit (DLAB)

LCR (0) and LCR (1) word length select bit 1: The number of bits in each serial character is programmed as shown in the following chart:

LCR (1)	LCR (0)	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

LCR (2) Stop Bit Select: LCR (2) specifies the number of stop bits in each transmitted character. If LCR (2) is a logic 0, one stop bit is generated in the transmitted data. If LCR (2) is a logic 1 when a 5-bit word length is selected, 1.5 stop bits are generated. If LCR (2) is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two stop bits are generated. The receiver checks for two stop bits if programmed.

LCR (3) Parity Enable: When LCR (3) is high, a parity bit between the last data word bit and stop bit is generated and checked.

LCR (4) Even Parity Select: When parity is enabled (LCR (3) = 1). LCR (4)-0 selects odd parity, and LCR (4) = 1 selects even parity.

LCR (5) Stick Parity: When parity is enabled (LCR (3) = 1), LCR (5) = 1 causes the transmission and reception of a parity bit to be in the opposite state from that indicated by LCR (4). This allows the user to force parity to a known state and for the receiver to check the parity bit in a known state.

LCR (6) Break Control: When LCR (6) is set to a logic "1", the serial output (SOUT) is forced to the spacing (logic 0) state. The break is disabled by setting LCR (6) to a logic "0". The Break Control bit acts only on SOUT and has no effect on the transmitter logic. Break Control enables the CPU to alert a terminal in a computer communications system. If the following sequence is used, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all "0"s pad character in response to THRE.
2. Set break in response to the next THRE.
3. Wait for the transmitter to be idle (TEMT = 1), and clear break when normal transmission has to be restored.

LCR (7) Divisor Latch Access Bit (DLAB): LCR (7) must be set high (logic "1") to access the Divisor Latches DLL and DLM of the Baud Rate Generator during a read or write operation. LCR (7) must be input low to access the Receiver Buffer, the Transmitter Holding, or the Interrupt Enable Registers.

The Line Status Register (LSR) is a single register that provides status indications. The LSR is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of each serial channel of the UM82C452.

Three error flags OE, FE, and PE provide the status of

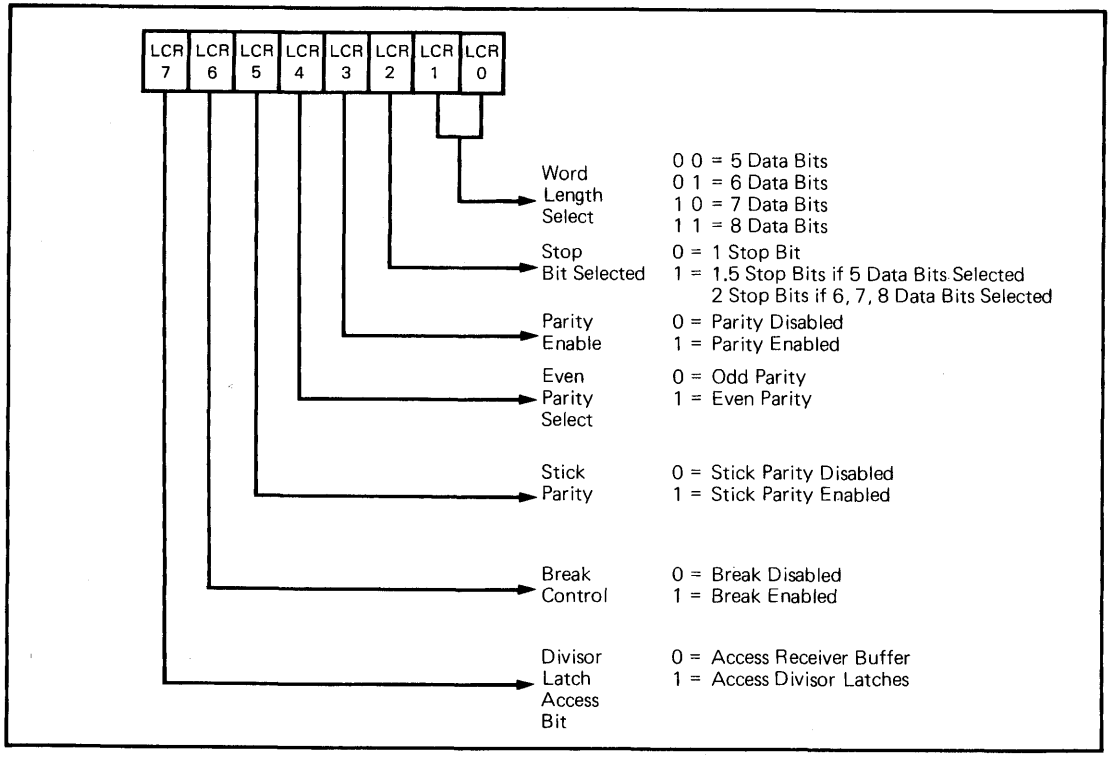


Figure 1. Line Control Register

any error conditions detected in the receiver circuitry. During reception of the stop bits, the error flags are set high by an error condition. The error flags are not reset by the absence of an error condition in the next received character. The flags reflect the last character only if no overrun occurred. The Overrun Error (OE) indicates that a character in the Receiver Buffer Register has been overwritten by a character from the Receiver Shift Register before being read by the CPU. The character is thereby lost. Framing Error (FE) indicates that the last character received contained incorrect (low) stop bits. This is caused by the absence of the required stop bit or by a stop bit too short to be detected. Parity Error (PE) indicates that the last character received had a parity error based on the programmed and calculated parity of the received character.

The Break Interrupt (BI) status bit indicates that the last character received was a break character. A break character is an invalid data character. However, it is an entire character, including parity and stop bits.

The Transmitter Holding Register Empty (THRE) bit indicates that the THR register is empty and may receive another character. The Transmission Shift Register Empty (TEMT) bit indicates that the Transmitter Shift Register is empty, and the serial channel has completed transmission of the last character to be sent. If the interrupt is enabled [IER (1)], an active THRE causes an interrupt (INTRPT).

The Data Ready (DR) bit indicates that the RBR has been loaded with a received character (including Break) and that the CPU may access this data.

Reading the LSR clears LSR (1)-LSR (4). (OE, PE, FE, and BI.)

The contents of the Line Status Register shown in Table 2 are described below:

LSR (0) Data Ready (DR): Data Ready is set high when an incoming character has been received and transferred into the Receiver Buffer Register. LSR (0) is reset low by a CPU read of the data in the Receiver Buffer Register.

LSR (1) Overrun Error (OE): Overrun Error indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, overwriting the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

Table 2. Line Status Register Bits

LSR Bits	Logic 1	Logic 0
LSR (0) Data Ready (DR)	Ready	Not Ready
LSR (1) Overrun Error (OE)	Error	No Error
LSR (2) Parity Error (PE)	Error	No Error
LSR (3) Framing Error (FE)	Error	No Error
LSR (4) Break Interrupt (BI)	Break	No Break
LSR (5) Transmitter Holding Register Empty (THRE)	Empty	Not Empty
LSR (6) Transmitter Empty (TEMT)	Empty	Not Empty
LSR (7) Not Used		

LSR (2) Parity Error (PE): Parity Error indicates that the received data character does not have the correct even or odd parity, as selected by the Even Parity Select bit [LCR (4)]. The PE bit is set high upon detection of a parity error, and is reset low when the CPU reads the contents of the LSR.

LSR (3) Framing Error (FE): Framing Error indicates that the received character did not have a valid stop bit. LSR (3) is set high when the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is reset low when the CPU reads the contents of the LSR.

LSR (4) Break Interrupt (BI): Break Interrupt is set high when the received data input is held in the spacing (logic 0) state for longer than a full word transmission time (start bit + data bits + parity + stop bits). The BI indicator is reset when the CPU reads the contents of the Line Status Register.

LSR (1) $\overline{\text{LSR}}$ (4) are the error conditions that produce a Receiver Line Status interrupt (priority 1 interrupt in the Interrupt Identification Register (IIR)) when any of the conditions are detected. This interrupt is enabled by setting IER (2) = 1 in the Interrupt Enable Register.

LSR (5) Transmitter Holding Register Empty (THRE): THRE indicates that the UM82C450 is ready to accept a new character for transmission. The THRE bit is set high when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. LSR (5) is reset low by the loading of the Transmitter Holding Register by the CPU. LSR (5) is not reset by a CPU read of the LSR.

When the THRE interrupt is enabled (IER (1) = 1). THRE causes a priority 3 interrupt in the IIR. If THRE is the interrupt source indicated in IIR, INTRPT is cleared by a read of the IIR.

LSR (6) Transmitter Empty (TEMT): TEMT is set high when the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. LSR (6) is reset low when a character is loaded into the THR and remains low until the character is transferred out of SOUT. TEMT is not reset low by a CPU read of the LSR.

LSR (7): This bit is always 0.

The Modem Control Register (MCR) controls the interface with the modem or data set as described in Table 3. The MCR can be written and read. The $\overline{\text{RTS}}$ and $\overline{\text{DTR}}$ outputs are directly controlled by their control bits in this register. A high input asserts a low (true) at the output pins. MCR Bits 0, 1, 3, and 4 are shown below:

MCR (0): When MCR (0) is set high, the $\overline{\text{DTR}}$ output is forced low. When MCR (0) is reset low, the $\overline{\text{DTR}}$ output is forced high. The $\overline{\text{DTR}}$ output of the serial channel may be input into an inverting line driver in order to

Table 3. Modem Control Register Bits

MCR Bits	Logic 1	Logic 0
MCR (0) Data Terminal Ready (DTR)	$\overline{\text{DTR}}$ Output Low	$\overline{\text{DTR}}$ Output High
MCR (1) Request to Send (RTS)	$\overline{\text{RTS}}$ Output Low	$\overline{\text{RTS}}$ Output High
MCR (2) 0		
MCR (3) Interrupt (INT) Enable	INT Enabled	INT Disabled
MCR (4) Loop	Loop Enabled	Loop Disabled
MCR (5) 0		
MCR (6) 0		
MCS (7) 0		

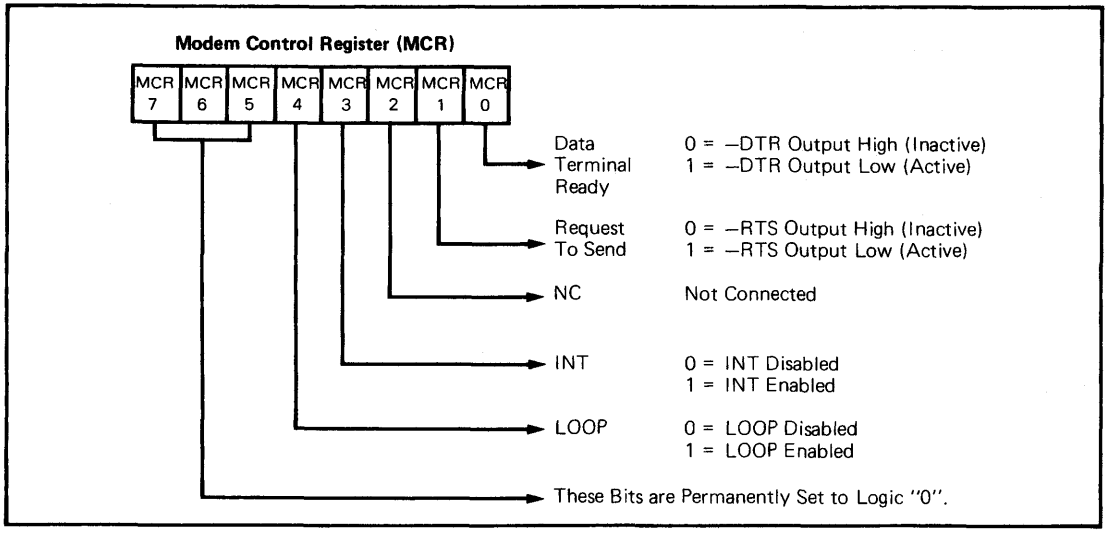


Figure 2. Modem Control Register

obtain the proper polarity input at the modem or data set.

MCR (1): When MCR (1) is set high, the $\overline{RTS}$ output is forced low. When MCR (1) is reset low, the $\overline{RTS}$ output is forced high. The $\overline{RTS}$ output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

MCR (3): When MCR (3) is set high, the INT output is enabled.

MCR (4): MCR (4) provides a local loopback feature for diagnostic testing of the channel. When MCR (4) is set high, Serial Output (SOUT) is set to the marking (logic "1") state, and the receiver data input Serial Input (SIN) is disconnected. The output of the Transmitter Shift Register is looped back into the Receiver Shift Register input. The three modem control inputs ($\overline{CTS}$, $\overline{DSR}$, and $\overline{RI}$) are disconnected. The modem control outputs ($\overline{DTR}$ and $\overline{RTS}$) are internally connected to the four modem control inputs. The modem control output pins are forced to their inactive state (high).

In the diagnostic mode, data transmitted is immediately received. This allows the processor to verify the transmit and receive data paths of the selected serial channel. Bits MCR(5)–MCR(7) are permanently set to logic 0.

The MSR provides the CPU with status of the modem input lines from the modem or peripheral devices. The MSR allows the CPU to read each of the several channel modem signal inputs by accessing the data bus interface of the UM82C452. In addition to the current status information, four bits of the MSR indicate whether the modem inputs have changed since the last reading of the MSR. The delta status bits are set high when a control input from the modem changes state, and reset low when the CPU reads the MSR.

The modem input lines for each channel are $\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$ and $\overline{RLSD}$. MSR (4) $\overline{MSR}$ (7) are status indications of these lines. The status indications follow the status of the input lines. If the modem status interrupt in the Interrupt Enable Register is enabled [IER (3)], a change of state in modem input signals will be reflected by the modem status bits in the IIR register, and an interrupt (INTRPT) is generated. The MSR is a priority 4 interrupt. The contents of the Modem Status Register are described in Table 4. Note that the states (high or low) of the status bits are inverted versions of the actual input pins.

MSR (0) Delta Clear to Send (DCTS): DCTS indicates that the CTS input to the serial channel has changed state since the last time it was read by the CPU.

MSR (1) Delta Data Set Ready (DDSR): DDSR indicates that the DSR input to the serial channel has changed state since the last time it was read by the CPU.

MSR (2) Trailing Edge of Ring Indicator (TERI): TERI indicates that the RI input to the serial channel has changed state from high to low since the last time it was read by the CPU. Low to high transitions on RI do not activate TERI.

MSR (3) Delta Data Carrier Detect (DRSLD): DRSLD indicates that the RSLD input to the serial channel has changed state since the last time it was read by the CPU.

Table 4. Modem Status Register Bits

MSR Bit	Mnemonic	Description
MSR (1)	DDSR	Delta Data Set Ready
MSR (2)	TERI	Trailing Edge of Ring Indicator
MSR (0)	DCTS	Delta Clear to Send
MSR (3)	DRLSD	Delta Data Carrier Detect
MSR (4)	$\overline{CTS}$	Clear To Send
MSR (5)	$\overline{DSR}$	Data Set Ready
MSR (6)	$\overline{RI}$	Ring Indicator
MSR (7)	$\overline{RLSD}$	Receiver Line Signal Detect

MSR (4) Clear to Send (CTS): Clear to Send (CTS) is the status of the CTS input from the modem indicating to the serial channel that the modem is ready to receive data from the serial channel's transmitter output (SOUT). If the serial channel is in loop mode [MSR (4) = 1]. MSR (4) is equivalent to $\overline{RTS}$ in the MCR.

MSR (5) Data Set Ready (DSR): Data Set Ready (DSR) is a status of the DSR input from the modem to the serial channel which indicates that the modem is ready to provide received data to the serial channel receiver circuitry. If the channel is in the loop mode [MCR (4) = 1], MSR (5) is equivalent to DTR in the MCR.

MSR (6) Ring Indicator: Indicates the status to the RI input (pin 39). If the channel is in the loop mode [MCR (4) = 1], MSR (6) is not connected in the MCR.

MSR (7) Receive Line Signal Detect: Receive Line Signal Detect indicates the status of the Receive Line Signal Detect ($\overline{RLSD}$) input. If the channel is in the loop mode [MCR (4) = 1], MSR (4) is equivalent to OUT2 of the MCR.

The modem status inputs ($\overline{RI}$, $\overline{RLSD}$, $\overline{DSR}$, and $\overline{CTS}$) reflect the modem input lines with any change of status. Reading the MSR register will clear the delta modem status indications but has no effect on the status bits. The status bits reflect the state of the input pins regardless of the mask control signals. If DCTS, DDSR, TERI, or DRLSD are true, and a state change occurs during a read operation ($\overline{DISTR}$), the state change is not indicated in the MSR. If DCTS, DDSR, TERI, or DRLSD are false, and a state change occurs during a read operation, the state change is indicated after the read operation.

For LSR and MSR, the setting of status bits is inhibited during status register read $\overline{DISTR}$ operations. If a status condition is generated during a read $\overline{DISTR}$ operation, the status bit is not set until the trailing edge of the read $\overline{DISTR}$.

If a status bit is set during a read $\overline{DISTR}$ operation, and the same status condition occurs, that status bit will be cleared at the trailing edge of the read $\overline{DISTR}$ instead of being set again.

Each UM82C452 serial channel contains a programmable Baud Rate Generator (BRG) that divides the clock (DC to 3.1 MHz) by any divisor from 1 to $2^{16}-1$ (see also BRG description). The output frequency of the Baud Generator is 16X the data rate [divisor # = clock ÷ (baud rate x 16)]. Two 8-bit divisor latch registers store the divisor in a 16-bit binary format. These Divisor Latch registers must be loaded during initialization. Upon loading either of the Divisor latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load.

The receiver circuitry in each serial channel of the UM82C452 is programmable for 5, 6, 7, or 8 data bits per character. For words of less than 8 bits, the data is right justified to the least significant bit LSB = Data Bit 0 [RBR (0)]. Data Bit 0 of a data word [RBR (0)] is the first data bit received. The unused bits in a character less than 8 bits are output low to the parallel output by the serial channel.

Received data at the SIN input pin is shifted into the Receiver Shift Register by the 16X clock provided at the RCLK input. This clock is synchronized to the incoming data based on the position of the start bit. When a complete character is shifted into the Receiver Shift Register, the assembled data bits are parallel loaded into the Receiver Buffer Register. The DR flag in the LSR register is set.

Double buffering of the received data permits continuous reception of data without losing received data. While the Receiver Shift Register is shifting a new character into the serial channel, the Receiver Buffer Register is holding a previously received character for the CPU to read. Failure to read the data in the RBR before complete reception of the next character result in the low of the data in the Receiver Register. The OE flag in the LSR register indicates the overrun condition.

RBR Bits 0 thru 7:

RBR (0)	Data Bit 0
RBR (1)	Data Bit 1
RBR (2)	Data Bit 2
RBR (3)	Data Bit 3
RBR (4)	Data Bit 4
RBR (5)	Data Bit 5
RBR (6)	Data Bit 6
RBR (7)	Data Bit 7

The Transmitter Holding Register (THR) holds parallel data from the data bus (D0-D7) until the Transmitter Shift Register is empty and ready to accept a new character for transmission. The transmitter and receiver word length and number of stop bits are the same. If the character is less than eight bits, unused bits at the microprocessor

data bus are ignored by the transmitter.

Data Bit 0 [THR (0)] is the first serial data bit transmitted. The THRE flag [LSR (5)] reflect the status of the THR. The TEMT flag [LSR (5)] indicates if both the THR and TSR are empty.

THR Bits 0 thru 7

THR (0)	Data Bit 0
THR (1)	Data Bit 1
THR (2)	Data Bit 2
THR (3)	Data Bit 3
THR (4)	Data Bit 4
THR (5)	Data Bit 5
THR (6)	Data Bit 6
THR (7)	Data Bit 7

The Scratchpad Register is an 8-bit Read/Write register that has no effect on either channel in the UM82C452. It is intended to be used by the programmer to hold data temporarily.

SCR Bits 0 thru 7

SCR (0)	Data Bit 0
SCR (1)	Data Bit 1
SCR (2)	Data Bit 2
SCR (3)	Data Bit 3
SCR (4)	Data Bit 4
SCR (5)	Data Bit 5
SCR (6)	Data Bit 6
SCR (7)	Data Bit 7

Interrupts

The Interrupt Identification Register (IIR) of each serial channel of the UM82C452 has interrupt capability for interfacing to current microprocessors. In order to minimize software overhead during data character transfers, the serial channel prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows:

1. Receiver Line Status (priority 1)
2. Received Data Ready (priority 2)
3. Transmitter Holding Register Empty (priority 3)
4. Modem Status (priority 4)

Information indicating that a prioritized interrupt is pending and the type of interrupt is stored in the Interrupt Identification Register (IIR). When addressed during chip select time, the IIR indicates the highest priority interrupt pending. No other interrupts are acknowledged until the interrupt is serviced by the CPU. The logic equivalent of the interrupt control circuit is shown in Figure 3. The contents of the IIR are indicated in Table 5 and are described below.

IIR (0): IIR (0) can be used in either a hard-wired prioritized or polled environment to indicate whether an interrupt is pending. When IIR (0) is low, an interrupt is pending, and IIR contents may be used as a pointer to the appropriate interrupt service routine. When IIR(0) is high, no interrupt is pending.

IIR (1) and IIR (2) are used to identify the highest priority interrupt pending as indicated in Table 5.

IIR (3)-IIR (7): These five bits of the IIR are logic 0.

The Interrupt Enable Register (IER) is a Write register used to independently enable the four serial channel interrupts which activate the interrupt (INTRPT) output. All interrupts are disabled by resetting IER (0)-IER (3) of the Interrupt Enable Register. Interrupts are enabled by setting the appropriate bits of the IER high. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers. The contents of the Interrupt Enable Register are indicated in Table 6 and are described below.

IER (0): When programmed high [IER (0) = Logic 1], IER (0) enables Received Data Available Interrupt.

IER (1): When programmed high [IER (1) = Logic 1], IER (1) enables the Transmitter Holding Register Empty interrupt.

IER (2): When programmed high [IER (2) = Logic 1], IER (2) enables the Receiver Line Status interrupt.

IER (3): When programmed high [IER (3) = Logic 1], IER (3) enables the Modem Status Interrupt.

IER (4)-IER (7): These four bits of the IER are logic 0.

Transmitter

The serial transmitter section consists of a Transmitter Holding Register (THR), Transmitter Shift Register (TSR), and associated control logic. The Transmitter Holding Register Empty (THRE) and Transmitter Shift Register Empty (TEMT) are two bits in the Line Status Register which indicate the status of THR and TSR. To transmit a 5- to 8-bit word, the word is written through D0-D7 to the THR. The microprocessor should perform a write operation only if THRE is high. The THRE is set high when the word is automatically transferred from the THR to the TSR during the transmission of the start bit.

Table 5. Interrupt Identification Register

Interrupt Identification				Interrupt Set and Reset Functions		
Bit 2	**Bit 1**	**Bit 0**	**Priority Level**	**Interrupt Flag**	**Interrupt Source**	**Interrupt Reset Control**
X	X	1		None	None	
1	1	0	First	Receiver Line Status	OE, PE FE, or BI	LSR Read.
1	0	0	Second	Received Data Available	Received Data Available	RBR Read
0	1	0	Third	THRE	THRE	IIR Read if THRE is the Interrupt Source or THR Write
0	0	0	Fourth	Modem Status	–CTS, –DSR –RI, –RSLD	MSR Read

X = Not Defined.

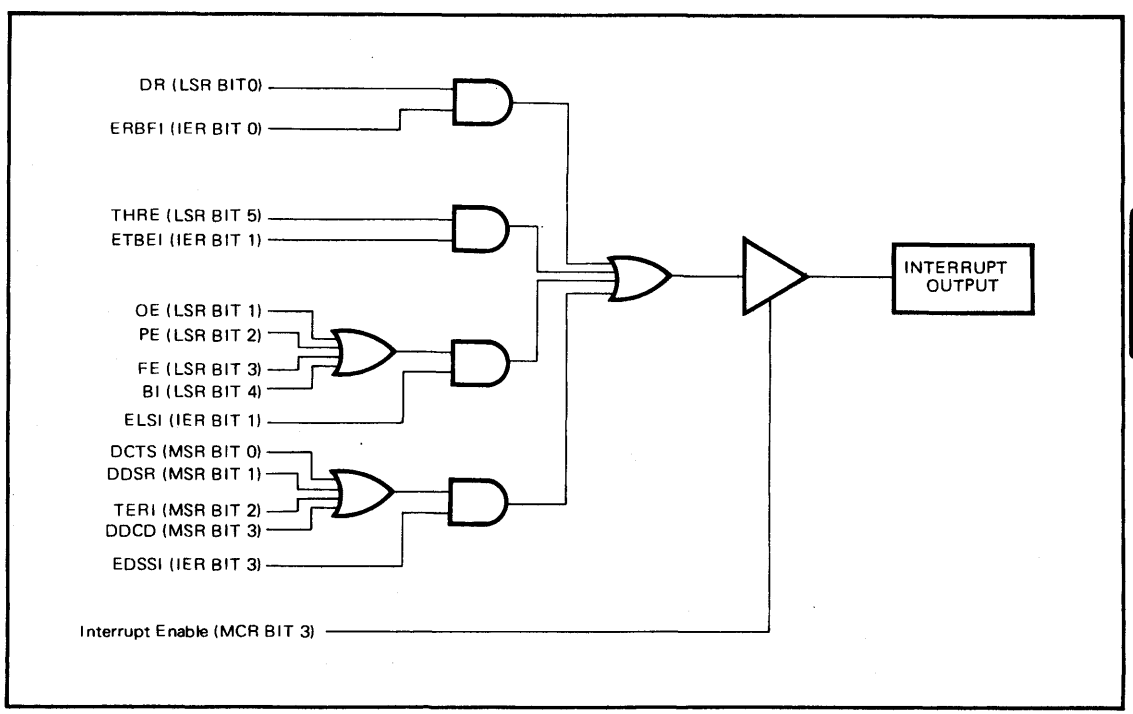


Figure 3. Interrupt Control Logic

Table 6. Serial Channel Accessible Registers

Register Mnemonic	Register Bit Number							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
RBR (Read Only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)*
THR (Write Only)	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
IER	0	0	0	0	(EDSSI) Enable Modem Status Interrupt	(ELSI) Enable Receiver Line Status Interrupt	(ETBEI) Enable Transmitter Holding Register Empty Interrupt	(ERBFI) Enable Received Data Available Interrupt
IIR (Read Only)	0	0	0	0	0	Interrupt ID Bit (1)	Interrupt ID Bit (0)	"0" If Interrupt Pending
LCR	(DLAB) Divisor Latch Access Bit	Set Break	Stick Parity	(EPS) Even Parity Select	(PEN) Parity Enable	(STB) Number of Stop Bits	(WLSB1) Word Length Select Bit 1	(WLSB0) Word Length Select Bit 0
MCR	0	0	0	Loop	Out 2	Out 1	(RTS) Request To Send	(DTR) Data Terminal Ready
LSR	0	(TEMT) Transmitter Empty	(THRE) Transmitter Holding Register Empty	(BI) Break Interrupt	(FE) Framing Error	(PE) Parity Error	(OE) Overrun Error	(DR) Data Ready
MSR	(DCD) Data Carrier Detect	(RI) Ring Indicator	(DSR) Data Ready Set	(CTS) Clear to Send	(DRSLD) Delta Receive Line Signal Detect	(TERI) Trailing Edge Ring Indicator	(DDSR) Delta Data Set Ready	(DCTS) Delta Clear to Send
SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

*LSB Data Bit 0 is the first bit transmitted or received.

0. After completion of the transfer, THRE returns high. TEMT remains low for at least the duration of the transmission of the data word. If a second character is transmitted to the THR, the THRE is reset low. Since the data word cannot be transferred from the THR to the TSR until the TSR is empty. THRE remains low until the TSR has completed transmission of the word. When the last word has been transmitted out of the TSR, TEMT is set high. THRE is set high one THR to TSR transfer time later.

Receiver

Serial asynchronous data is input into the SIN pin. The idle state of the line providing the input into SIN is high. A start bit detect circuit continually searches for a high to low transition from the idle state. When the transition is detected, a counter is reset, and counts the 16X clock to 71/2, which is the center of the start bit. The start bit is valid if the SIN is still low at the midbit sample of the start bit. Verifying the start bit prevents the receiver from assembling an incorrect data character due to a low going noise spike on the SIN input.

The Line Control Register determines the number of data bits in a character (LCR (0), LCR (1)), number of stop bits LCR (2), if parity is used LCR (3), and the polarity of parity LCR (4). If Status information for the receiver is provided in the Line Status Register to the Receiver Buffer Register, the Data Received indication in LSR (0) is set high, the CPU reads the Receiver Buffer Register through D0-D7. This read resets LSR (0). If D0-D7 are not read prior to a new character transfer from the RSR to the RBR, the overrun error status indication is set in LSR (1). The parity check tests for even or odd parity on the parity bit, which precedes the first stop bit. If there is a parity error, the parity error is set in LSR (2). There is circuitry which tests whether the stop bit is high. If it is not, a framing error indication is generated in LSR (3).

The center of the start bit is defined as clock count 7 1/2. If the data into SIN is a symmetrical square wave, the center of the data cells will occur within ±3.125% of the actual center, providing an error margin of 46.875%. The start bit can begin as much as one 16X clock cycle prior to being detected.

Baud Rate Generator (BRG)

The BRG generates the clocking for the UART function, providing standard ANSI/CCITT bit rates. The oscillator driving the BRG is provided by an external clock into CLK.

The bit rate is selected by programming the two divisor latches, Divisor Latch Most Significant Byte and Divisor Latch Least Significant Byte. Setting DLL=1 and DLM=0 selects the divisor to divide by 1 (divide by 1 gives maximum baud rate for a given input frequency at the CLK input).

The BRG can use any of three different popular frequencies to provide standard baud rates. These frequencies are 1.8432 MHz, 2.4576 MHz, and 3.072 MHz. With these frequencies, standard bit rates from 50 to 38.5 kbps are available. Tables 7, 8, and 9 illustrate the divisors needed to obtain standard rates using these three crystal frequencies.

Reset

After power up, the UM82C452 $\overline{\text{RESET}}$ input (MR) should be held low for 500 ns to reset the UM82C452 circuits to an idle mode until initialization. A low on $\overline{\text{RESET}}$ causes the following:

1. Initializes the transmitter and receiver internal clock counters.
2. Clears the Line Status Register (LSR), except for Transmitter Shift Register Empty (TEMT) and Transmit Holding Register Empty (THRE), which are set. The Modem Control Register (MCR) is also cleared. All of the discrete lines, memory elements and logic associated with these register bits are also cleared or turned off. The Line Control Register (LCR), Divisor Latches, Receiver Buffer Register, Transmitter Buffer Register are not affected.

Following removal of the reset condition (Reset high), the UM82C452 remains in the idle mode until programmed.

A hardware reset of the UM82C452 sets the THRE and TEMT status bit in the LSR. When interrupts are subsequently enabled, an interrupt occurs due to THRE.

A summary of the effect of a reset on the UM82C452 is given in Table 10.

Programming

Each serial channel of the UM82C452 is programmed by the control registers LCR, IER, DLL and DLM, and MCR. These control words define the character length, number of stop bits, parity, baud rate, and modem interface. While the control register can be written in any order, the IER should be written to last because it controls the interrupt enables. Once a serial channel is programmed and operational, these registers can be updated any time the UM82C452 serial channel is not transmitting or receiving data.

The control signals required to access each serial channel's internal registers are shown below.

Software Reset

A software reset of the serial channel is a useful method for returning to a completely known state without a system reset. Such a reset consists of writing to the LCR, Divisor Latches, and MCR registers. The LSR and RBR registers should be read prior to enabling interrupts in order to clear out any residual data or status bits which may be invalid for subsequent operation.

Clock Input Operation

The maximum input frequency of the external clock of the UM82C452 is 3.1 MHz.

Table 7. Baud Rates (1.8432 MHz Clock)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	2304	–
75	1536	–
110	1047	0.026
134.5	857	0.058
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.69
2400	48	–
3600	32	–
4800	24	–
7200	16	–
9600	12	–
19200	6	–
38400	3	–
56000	2	2.86

Table 8. Baud Rates (2.4576 MHz Clock)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	3072	–
75	2048	–
110	1396	0.026
134.5	1142	0.0007
150	1024	–
300	512	–
600	256	–
1200	128	–
1800	85	0.392
2000	77	0.260
2400	64	–
3600	43	0.775
4800	32	–
7200	21	1.587
9600	16	–
19200	8	–
38400	4	–

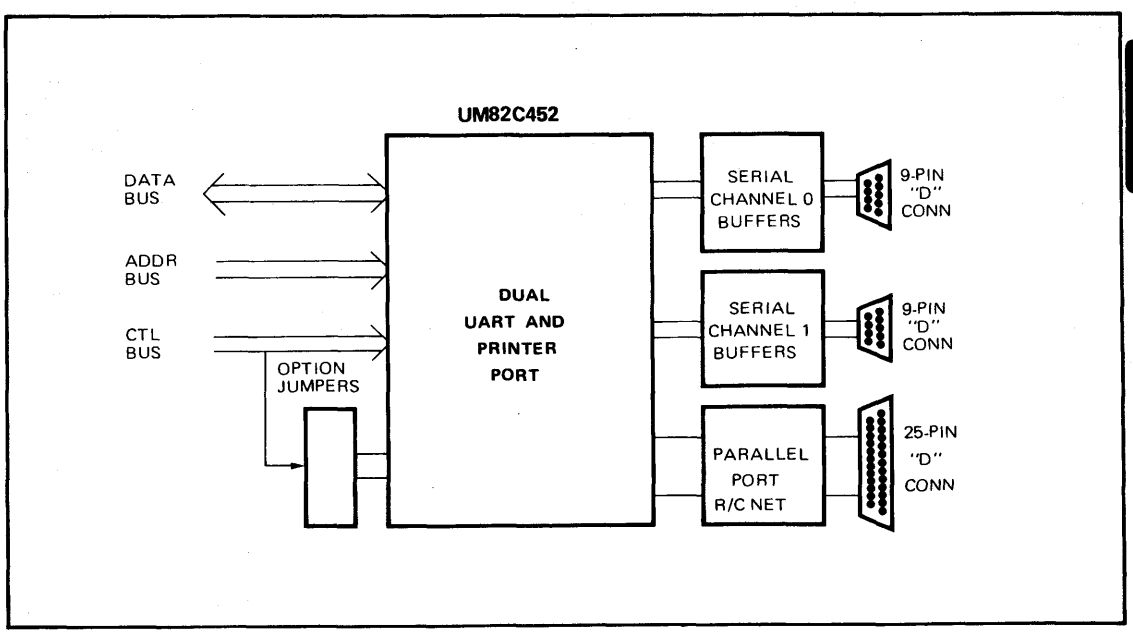
Table 9. Baud Rates (3.072 MHz Clock)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	3840	–
75	2560	–
110	1745	0.026
134.5	1428	0.034
150	1280	–
300	640	–
600	320	–
1200	160	–
1800	107	0.312
2000	96	–
2400	80	–
3600	53	0.628
4800	40	–
7200	27	1.23
9600	20	–
19200	10	–
38400	5	–

Table 10. Reset Control of Register and Pinout Signals

Register/Signal	Reset Control	Reset Status
Interrupt Enable Register	Reset	All Bits low
Interrupt Identification Register	Reset	Bit 0 is high and Bits 1-7 are low
Line Control Register	Reset	All Bits low
Line Status Register	Reset	Bits 5,6 are high, others are low
Modem Status Register	Reset	Bits 0-3 are low, Bits 4-7 are input signals
SOUT0, SOUT1	Reset	High
$\overline{RTS0}$, $\overline{RTS1}$, $\overline{DTR0}$, $\overline{DTR1}$	Reset	High
INT0, INT1, INT2	Reset	High-Impedance
$\overline{STB}$, $\overline{AFD}$, $\overline{SLIN}$ $\overline{INIT}$	Reset Reset	High, Low

Device Application



Functional Description:

Parallel Port Registers

The UM82C452 parallel port interfaces the device to a Centronics-style printer. When Chip Select 2 ($\overline{CS2}$) is low, the parallel port is selected. Table 11 shows the registers associated with this parallel port. The read or write function of the register is controlled by the states of the read ($\overline{IOR}$) and write ($\overline{IOW}$) pins as shown. The top four registers are read-only registers, and the bottom four are write-only registers.

Since the parallel port is bidirectional, the first register (READ PORT) allows the microprocessor to read the information on the parallel bus. The second register (READ STATUS) allows the microprocessor to read the status of the printer in the five most significant bits. The status bits are Printer Busy (BUSY), Acknowledge ($\overline{ACK}$), which is a handshake function, Paper Empty (PE), Printer Selected (SLCT), and Error ($\overline{ERROR}$). The third register (READ CONTROL functions are duplicated in the sixth register (WRITE CONTROL).

The control bits are found in the five least significant bits of these registers,. They are Interrupt Enable (IRQ ENB), Select In ($\overline{SLIN}$), Initialize the Printer ($\overline{INIT}$), Autofeed the Paper ($\overline{AUTOFD}$), and Strobe ($\overline{STROBE}$), which informs the printer of the presence of a valid byte on the parallel bus. The fifth register (WRITE PORT) allows the microprocessor to write a byte to the printer.

The parallel port is completely compatible with the parallel port implementation used in the IBM Serial/Parallel Adaptor.

Table 12. Parallel Port Register Select

Control Pins					Register Selected
–IOR	–IOW	–CS2	A1	A0	
0	1	0	0	0	Read Port
0	1	0	0	1	Read Status
0	1	0	1	0	Read Control
0	1	0	1	1	Invalid
1	0	0	0	0	Write port
1	0	0	0	1	Invalid
1	0	0	1	0	Write Control
1	0	0	1	1	Invalid

Table 11. Parallel Port Registers

Register	Register Bits							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read Port	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Read Status	BUSY	$\overline{ACK}$	PE	SLCT	$\overline{ERROR}$	1	1	1
Read Control	1	1	1	IRQ ENB	$\overline{SLIN}$	$\overline{INIT}$	$\overline{AUTOFD}$	$\overline{STROBE}$
Write Port	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Write Control	1	1	1	IRQ ENB	$\overline{SLIN}$	$\overline{INIT}$	$\overline{AUTOFD}$	$\overline{STROBE}$

AC Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$ (Notes 1, 5)

Serial

Symbol	Parameter	Min	Max	Unit	Condition
t_{DIW}	$\overline{DISTR}$ to Floating Data Delay	125		ns	
RC	Read Cycle	360		ns	
t_{DDD}	Delay from $\overline{DISTR}$ to Data		125	ns	100 pF Load
t_{HZ}	$\overline{DISTR}$ to Floating Data Delay	0	100	ns	100 pF Load, Note 4
t_{DOW}	$\overline{DOSTR}$ Strobe Width	100		ns	
WC	Write Cycle	360		ns	
t_{DS}	Data Setup Time	40		ns	
t_{DH}	Data Hold Time	40		ns	
t_{RA}	Address Hold Time from $\overline{DISTR}$	20		ns	Note 2
t_{RCS}	Chip Select Hold Time for $\overline{DISTR}$	20		ns	Note 2
t_{AR}	$\overline{DISTR}$ Delay from Address	60		ns	Note 2

AC Characteristics (Continued)

Symbol	Parameter	Min	Max	Unit	Conditions
t_{CSR}	$\overline{DISTR}$ Delay from Chip Select	50		ns	Note 2
t_{WA}	Address Hold Time from $\overline{DOSTR}$	20		ns	Note 2
t_{WCS}	Chip Select Hold Time from $\overline{DOSTR}$	20		ns	Note 2
t_{AW}	$\overline{DOSTR}$ Delay from Address	60		ns	Note 2
t_{CSW}	$\overline{DOSTR}$ Delay from Select	50		ns	Note 2
t_{RW}	Reset Pulse Width	5		μs	
t_{XH}	Duration of Clock High Pulse	140		ns	External Clock
t_{XL}	Duration of Clock Low Pulse	140		ns	External Clock
Transmitter					
t_{HR1}	Delay from Rising Edge of $\overline{DOSTR}$ (WR THR) To Reset Interrupt		175	ns	100 pF Load
t_{IRS}	Delay from Initial INTR Reset to Transmit Start	8	24	CLK Cycles	Note 3
t_{SI}	Delay from Initial Write to Interrupt	16	32	CLK Cycles	Note 3
t_{STI}	Delay from Stop to Interrupt (THRE)	8	8	CLK Cycles	Note 3
t_{IR}	Delay from $\overline{DISTR}$ (RD IIR) to Reset Interrupt (THRE)		250	ns	100 pF Load
Modem Control					
t_{MDO}	Delay from DOSTR (WR MCR) to Output		200	ns	100 pF Load
t_{SIM}	Delay to Set Interrupt from MODEM Input		200	ns	100 pF Load
t_{RIM}	Delay to Reset Interrupt from $\overline{DISTR}$ (RS MSR)		250	ns	100 pF Load
Receiver					
t_{SINT}	Delay from Stop to Set Interrupt	1	1	CLK Cycles	Note 3
t_{RINT}	Delay from $\overline{DISTR}$ (RD RBR/RDLSR) to Reset Interrupt		1	μs	100 pF Load

Parallel Port

WRITE					
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**	
T_{WW}	Write Pulse Width	200	–	ns	
T_{AW}	Address to $\overline{IOW}$ Set-up Time	20	–	ns	
T_{WA}	Address Hold Time after $\overline{IOW}$	20	–	ns	
T_{DW}	Data to $\overline{IOW}$ Set-up Time	70	–	ns	
T_{WD}	Data Hold Time after $\overline{IOW}$	30	–	ns	
T_{WOL}	$\overline{IOW}$ = 1 to Data Latched	–	90	ns	

I/O And Peripherals

READ

Symbol	Parameter	Min.	Max.	Unit
T_{RR}	Read Pulse Width	300	–	ns
T_{AR}	Address to $\overline{IOR}$ Set-up Time	20	–	ns
T_{RA}	Address Hold Time after $\overline{IOR}$	20	–	ns
T_{PR}	Printer Bus to $\overline{IOR}$ Set-up Time	0	–	ns
T_{RP}	Printer Bus Hold Time after $\overline{IOR}$	0	–	ns
T_{RDS}	$\overline{IOR}$ to D0 – D7 Output	–	70	ns
T_{RDR}	D0 – D7 Released after $\overline{IOR}$	–	30	ns

*Note: When the CPU reads the printer's status, output data may change if the printer signals are unstable.

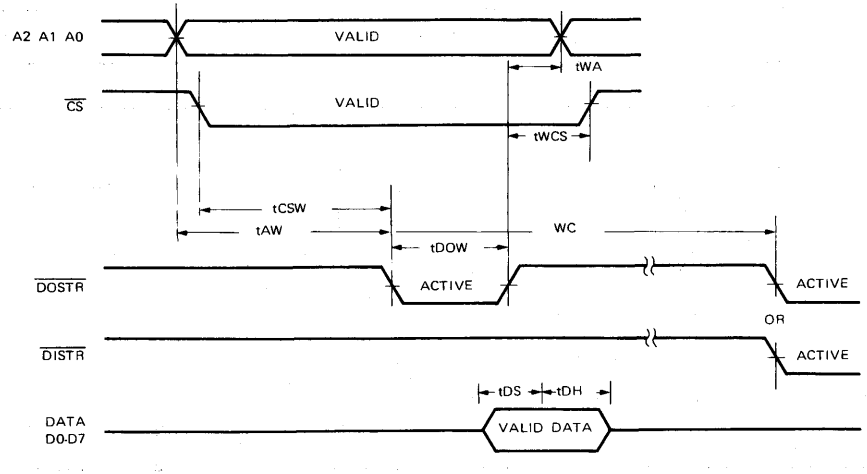
OTHERS

Symbol	Parameter	Min.	Max.	Unit
T_{RSW}	Reset Pulse Width	40	–	ns
T_{RSCH}	Reset to Control Bus = 1 ($\overline{STROB}$, $\overline{AUTOFD}$, $\overline{SLCT}$) Propagation Delay	–	90	ns
T_{RSIN1}	Reset to Control Bus $\overline{INIT}$ = 0 Propagation Delay	–	60	ns
T_{ID}	$\overline{ACK}$ to IRQ Propagation Delay	–	45	ns

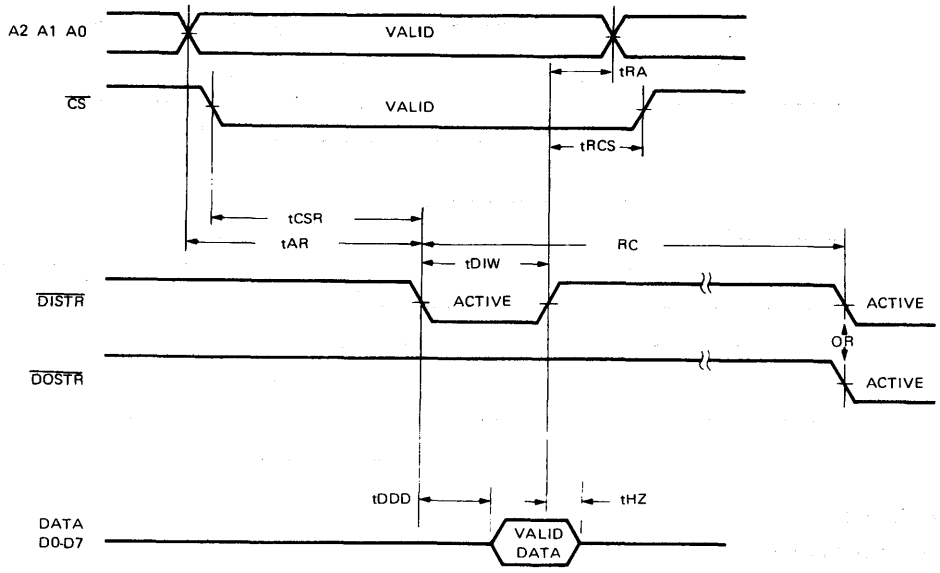
Notes: 1. All timing specifications apply to pins to both serial channels (e. g. Ri refers to both R10 and R11).
2. The internal address strobe is always active.
3. RCLK = t_{XH} and t_{XL}.
4. Charge and discharge time is determined by VOL, VOH and the external loading.
5. All timings are referenced to valid 0 and valid 1 (see AC TEST POINTS).

Serial Port Timing:

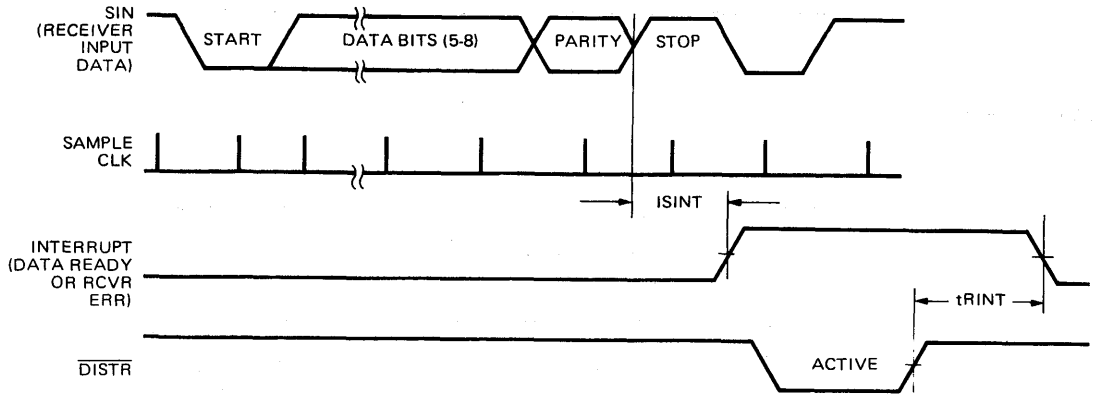
Write Cycle Timing



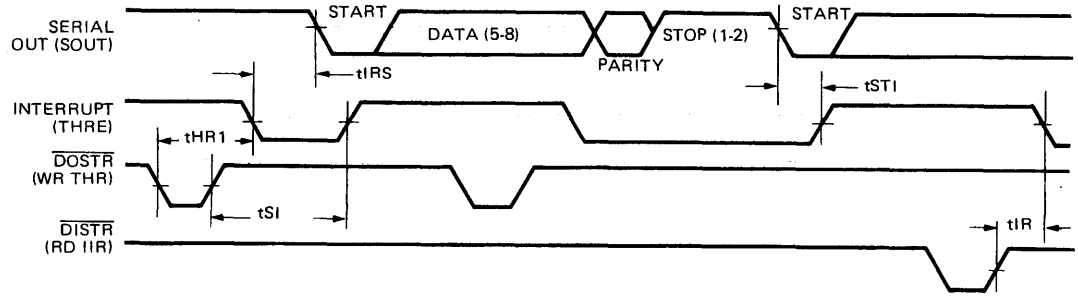
Read Cycle Timing



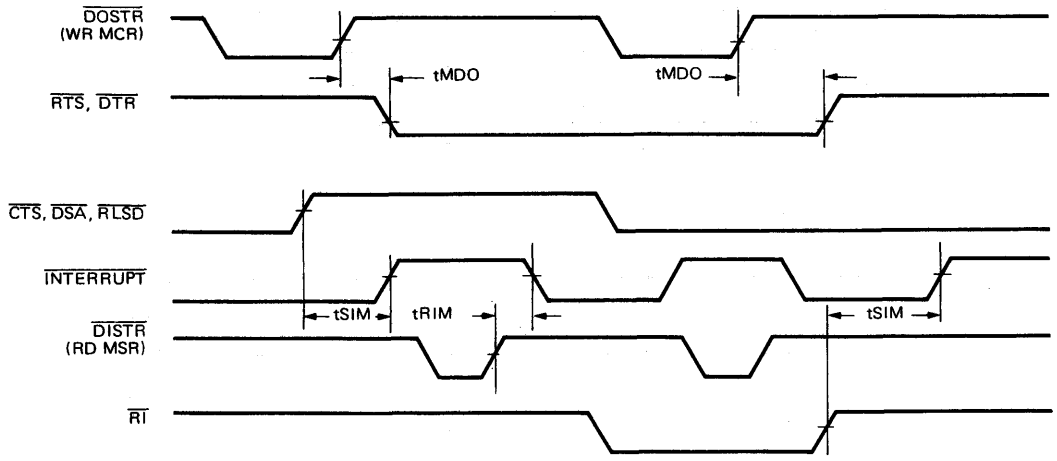
Receiver Timing



Transmitter Timing

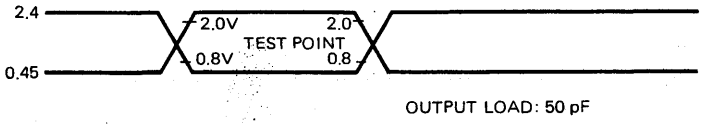


Modem Timing



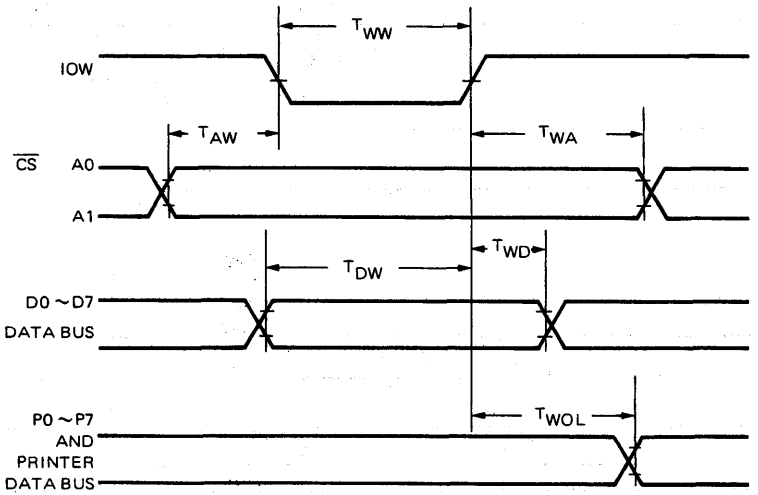
Parallel Port Timing:

A.C. Testing Input Waveform

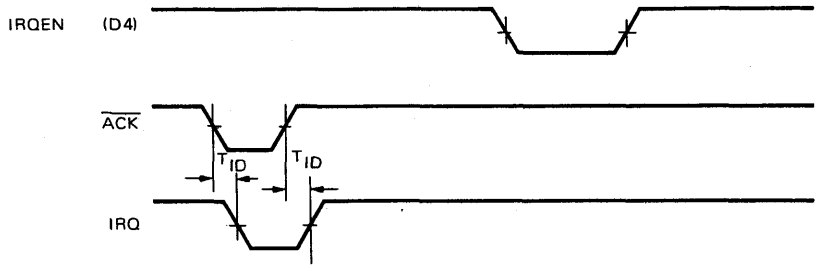


OUTPUT LOAD: 50 pF

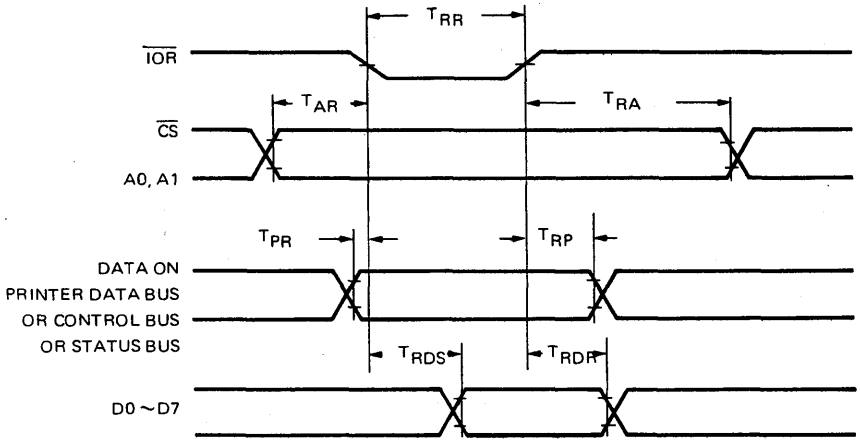
Write Cycle Waveform



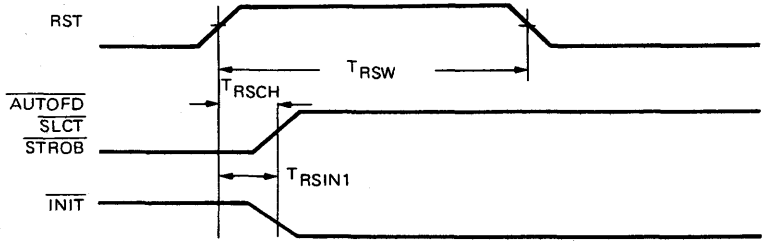
Interrupt Request Waveform



Read Cycle Waveform



Reset Waveform



Absolute Maximum Ratings *

Ambient Operating Temperature . . . . . −10°C to +70°C
Storage Temperature . . . . . −65°C to +150°C
Supply Voltage to Ground Potential . . . . . −0.5V to V_{CC} + 0.3V
Applied Output Voltage . . . . . −0.5V to V_{CC} + 0.3V
Applied Input Voltage . . . . . −0.5V to + 7.0V
Power Dissipation . . . . . 500 mW

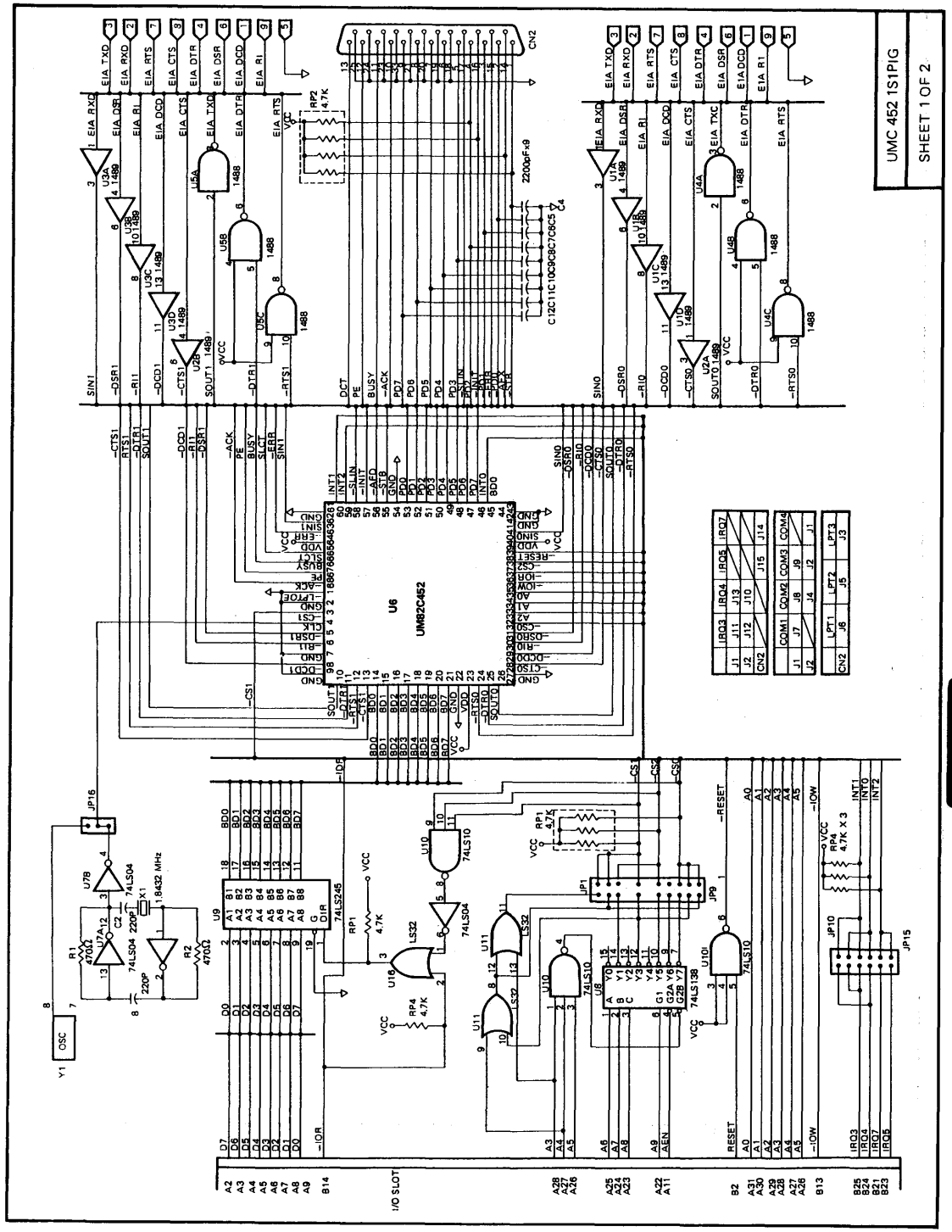
*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ± 5%)

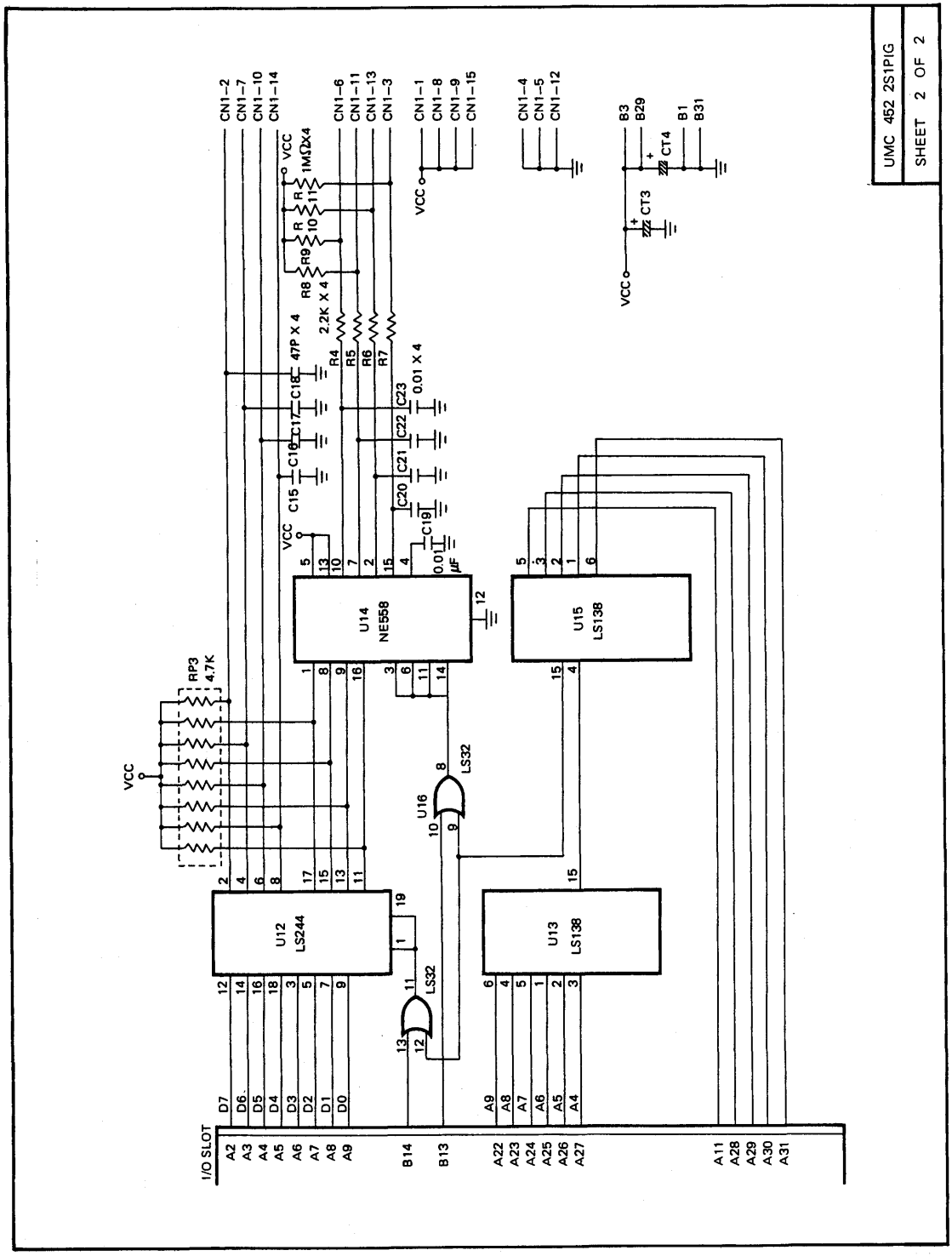
Symbol	Parameter	Min	Max	Unit	Conditions
V_{ILX}	Clock Input Low Voltage	−0.5	0.8	V	
V_{IHX}	Clock Input High Voltage	2.0	V_{CC}	V	
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 4.0 mA on DB0-DB7, 12 mA on PD0-PD7, 2 mA on all other outputs
V_{OH}	Output High Voltage	2.4		V	I_{OH}=−0.4 mA on DB0-DB7, −0.2 mA on PD0-PD7, −0.2 mA on all other outputs
I_{CC}	Power Supply Current		40	mA	V_{CC} = 5.25V, No loads on SIN0, 1;−DSR0, 1;−RLSD0, 1;−CTS0, 1. RI0, RI1 = 0 2.0V. Other inputs = 0.8V. Baud rate generator = 4 MHz, Baud rate = 56K
I_{IL}	Input Leakage		10	μA	V_{CC} = 5.25V, GND = 0V. All other pins floating.
I_{CL}	Clock Leakage		10	μA	V_{IN} = 0V, 5.25V
I_{OZ}	3-State Leakage		20	μA	V_{CC} = 5.25V, GND = 0V. VOUT = 0V, 5.25V 1) Chip deselected 2) Chip and write mode selected
V_{IL} (RES)	Reset Schmitt V_{IL}		0.8	V	
V_{IH} (RES)	Reset Schmitt V_{IH}	2.0		V	

Application Circuit



I/O And Peripherals

Application Circuit (Continued)



UMC

UM82C550

Asynchronous Communications Element with FIFOs

Features:

- Capable of running all existing UM82C450 software
- Pin for pin compatible with the existing UM82C450 except for CSOUT (24) and NC (29). The former CSOUT and NC pins will be TXRDY and RXRDY, respectively
- After reset, all registers are identical to the UM82C450 register set
- In the FIFO mode, transmitter and receiver are each buffered with 16 byte FIFO's to reduce the number of interrupts presented to the CPU.
- Adds or deletes standard asynchronous communication bits (start, stop, and parity) to or from the serial data
- Full double buffering in the CHARACTER mode eliminates need for precise synchronization
- Independently controlled transmit, receive, line status, and data set interrupts.
- Programmable baud generator divides any input clock by 1 to $(2^{16} - 1)$ and generates the 16x clock
- Independent receiver clock input
- MODEM control functions (CTS, RTS, DSR, DTR, RI, and DCD)
- Fully progrmmable serial-interface characteristics:
  - 5-, 6-, 7-, or 8-bit characters
  - Even, odd, or no-parity bit generation and detection
  - 1-, 1½-, or 2-stop bit generation
  - Baud generation (DC to 256K baud)
- False start bit detection
- Complete status reporting capabilities
- TRI-STATE TTL drive for the data and control buses
- Line break generation and detection
- Internal diagnostic capabilities:
  - Loopback controls for communications link fault isolation
  - Break parity overrun framing error simulation
- Fully prioritized interrupt system controls

General Description

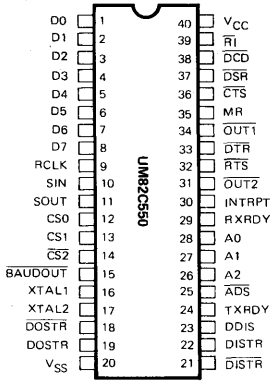
The UM82C550 is an improved version of the UM82C450 Asynchronous Communications Element (ACE). The improved specifications ensure compatibility with any of state-of-the-art CPUs. Functionally identical to the UM82C450 on power up (CHARACTER mode) the UM82C550 can be put into an alternate mode (FIFO mode) to relieve the CPU of excessive overhead when the data rate is high. In this mode internal FIFOs are activated allowing 16 bytes (plus 3 bits per byte of error data in the RCVR FIFO) to be stored in both receive and transmit modes. All the logic is on chip to minimize system overhead and maximize system efficiency. Two pin functions have been added to allow signalling of DMA transfers.

The ACE performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the ACE at any time during the functional operation. Status information reported includes the type and condition of the transfer operations being performed by the ACE, as well as any error conditions (parity, overrun, framing, or break interrupt).

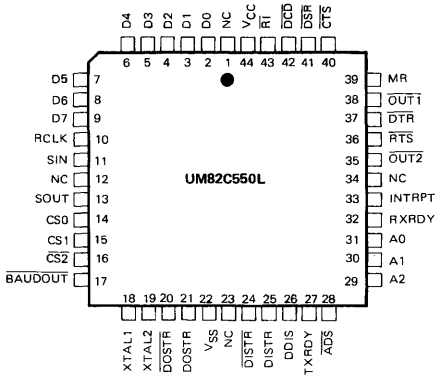
The ACE includes a programmable baud rate generator that is capable of dividing the timing reference clock input by divisors of 1 to $(2^{16} - 1)$, and producing a 16x clock for driving the internal transmitter logic. Provisions are also included to use this 16 x clock to drive the receiver logic. The ACE has complete MODEM-control capability, and a processor-interrupt system that may be software tailored to the user's requirements, minimizing the computing required to handle the communications link.

Pin Configurations

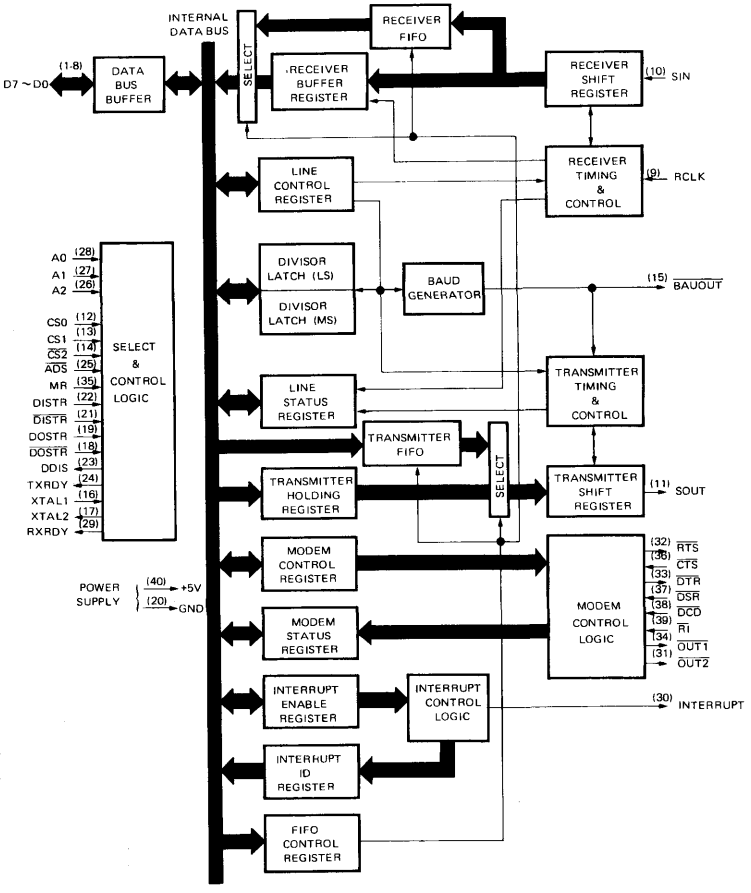
Dual-In-Line Package



Chip Carrier Package



Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description
1 ~ 8	Data Bus D0 ~ D7	I/O	This bus comprises eight TRI-STATE input/output lines. The bus provides bidirectional communications between the ACE and the CPU. Data control words, and status information are transferred via the D0 ~ D7 Data Bus.
9	RCLK	I	This input is the 16X baud rate clock for the receiver section of the chip.
10	SIN	I	Serial data input forms the communications link (peripheral device, MODEM, or data set).
11	SOUT	O	Composite serial data output to the communications link (perherial, MODEM or data set). The SOUT signal is set to the Marking (logic 1) state upon a Master Reset operation.
12 ~ 14	CS0 ~ $\overline{CS2}$	I	When CS0 and CS1 are high and $\overline{CS2}$ is low, the chip is selected. Chip selection is complete when the decoded chip select signal is latched with an active (low) Address Strobe ($\overline{ADS}$) input. This enables communication between the ACE and the CPU.
15	$\overline{BAUDOUT}$	O	16X clock signal for the transmitter section of the ACE. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches. The $\overline{BAUDOUT}$ may also be used for the receiver section by tying this output to the RCLK input of the chip.
16 ~ 17	XTAL1 XTAL2	I O	These two pins connect the main timing reference (crystal or signal clock) to the ACE.
18	$\overline{DOSTR}$ DOSTR	I I	When DISTR is high or $\overline{DISTR}$ is low while the chip is selected, it allows the CPU to write data or control words into a selected register of the ACE. Note: Only an active DOSTR or $\overline{DOSTR}$ input is required to transfer data to the ACE during a write operation. Therefore tie either the DOSTR input permanently low or the $\overline{DOSTR}$ input permanently high if not used.
20	GND		Ground
21 22	$\overline{DISTR}$ DISTR	I I	When DISTR is high or $\overline{DISTR}$ is low while the chip is selected, it allows the CPU to read status information or data from a selected register of the ACE. Note: Only an active DISTR or $\overline{DISTR}$ input is required to transfer data to the ACE during a read operation. Therefore tie either the DISTR input permanently low or the $\overline{DOSTR}$ input permanently high if not used.
23	DDIS	O	Goes low whenever the CPU is reading data from the ACE. A high-level DDIS output can be used to disable an external transceiver (if used between the CPU and ACE on the D7 ~ D0 Data Bus at all times except when the CPU is reading data.)

Pin Description (Continued)

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>24</td><td>TXRDY</td><td>O</td><td>Transmitter DMA signalling is available through this pin. When operating in the FIFO mode, one of two types of DMA signalling per pin can be selected via FCR3 when operating as in the Character Mode only DMA mode 0 is allowed. Mode 0 supports interleaved DMA where a transfer is made between CPU bus cycles. Mode 1 supports burst DMA where multiple transfers are made continuously until the XMIT FIFO has been filled.
TXRDY Mode 0: In the Character Mode (FCR0 = 0) or in the FIFO Mode (FCR0 = 1, FCR3 = 0) and there are no characters in the XMIT FIFO or XMIT holding register, the TXRDY pin (24) will be low active. Once It is activated the TXRDY pin will go inactive after the first character is loaded into the XMIT FIFO.
TXRDY Mode 1: In the FIFO Mode (FCR0 = 1) when FCR3 = 1 and there is at least one unfilled position in the XMIT FIFO. It will go low active. This pin will become inactive when the XMIT FIFO is completely full.</td></tr>
<tr><td>25</td><td>$\overline{ADS}$</td><td>I</td><td>When low, provides latching for the Register Select (A0, A1, A2) and Chip Select (CS0, CS1, $\overline{CS2}$) signals.
Note: An active $\overline{ADS}$ input is required when the Register Select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If not required tie the $\overline{ADS}$ input permanently low.</td></tr>
<tr><td>26 ~ 28</td><td>A0 ~ A2</td><td>I</td><td>These three inputs are used during a read or write operation to select an ACE register to read from or write into as indicated in the table below. Note that the state of the Divisor Latch Access Bit (DLAB), which is the most significant bit of the Line Control Register, affects the selection of certain ACE registers. The DLAB must be set high by the system software to access the Baud Generator Divisor Latches.
<table>
<tr><th>DLAB</th><th>A2</th><th>A1</th><th>A0</th><th>Register</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Receiver Buffer (read)
Transmitter Holding
Register (write)</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Interrupt Enable</td></tr>
<tr><td>X</td><td>0</td><td>1</td><td>0</td><td>Interrupt Identification (read)</td></tr>
<tr><td>X</td><td>0</td><td>1</td><td>0</td><td>FIFO Control (write)</td></tr>
<tr><td>X</td><td>0</td><td>1</td><td>1</td><td>Line Control</td></tr>
<tr><td>X</td><td>1</td><td>0</td><td>0</td><td>MODEM Control</td></tr>
<tr><td>X</td><td>1</td><td>0</td><td>1</td><td>Line Status</td></tr>
<tr><td>X</td><td>1</td><td>1</td><td>0</td><td>MODEM Status</td></tr>
<tr><td>X</td><td>1</td><td>1</td><td>1</td><td>Scratch</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Divisor Latch
(least significant byte)</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Divisor Latch
(most significant byte)</td></tr>
</table>
</td></tr>
</table>

Pin Description (Continued)

Pin No.	Symbol	I/O	Description
29	RXRDY	O	Receiver DMA signalling is available through this pin. When operating in the FIFO mode, one of two types of DMA signalling can be selected via FCR3. When operating as in the Character Mode only DMA mode 0 is allowed. Mode 0 supports interleaved DMA where a transfer is made between CPU bus cycles. Mode 1 supports burst DMA where multiple transfers are made continuously until the RCVR FIFO has been emptied. RXRDY Mode 0: When in the Character Mode (FCR0 = 0) or in the FIFO Mode (FCR0 = 1, FCR3 = 1) and there is at least 1 character in the RCVR FIFO or RCVR HOLD register, the RXRDY pin (29) will be low active. Once it is activated the RXRDY pin will go inactive when there are no more characters in the FIFO or HOLD register. RXRDY Mode 1: In the FIFO Mode (FCR0 = 1) when the FCR3 = 1 and the trigger level or the timeout has been reached, the RXRDY pin will go low active. Once it is activated it will go inactive when there are no more characters in the FIFO or hold register.
30	INTRPT	O	Goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER: Receiver Error Flag; Received Data Available timeout (FIFO Mode only), Transmitter Holding Register Empty and MODEM Status. The INTRPT signal is reset low upon the appropriate interrupt service or a master Reset operation.
31	$\overline{\text{OUT 2}}$	O	User-designated output that can be set to an active low by programming bit 3 (OUT 2) of the MODEM Control Register to high level. The $\overline{\text{OUT 2}}$ signal is set high upon a Master Reset Operation. The $\overline{\text{OUT 2}}$ signal is forced to its inactive state (high) during loop mode operation.
32	$\overline{\text{RTS}}$	O	When low, informs the MODEM or data set that the ACE is ready to transmit data. The $\overline{\text{RTS}}$ output signal can be set to an active low by programming bit 1 (RTS) of the MODEM Control Register. The $\overline{\text{RTS}}$ signal is set high upon a Master Reset operation. The $\overline{\text{RTS}}$ signal is forced to its inactive state (high) during loop mode operation.
33	$\overline{\text{DTR}}$	O	When low, informs the MODEM or data set that the ACE is ready to communicate. The $\overline{\text{DTR}}$ output signal can be set to an active low by programming bit 0 (DTR) of the MODEM Control Register to a high level. The $\overline{\text{DTR}}$ signal is set high upon a Master Reset operation. The $\overline{\text{DTR}}$ signal is forced to its inactive state (high) during loop mode operation.
34	$\overline{\text{OUT 1}}$	O	User-designated output that can be set to an active low by programming bit 2 (OUT 1) of the MODEM Control Register to high level. The $\overline{\text{OUT 1}}$ signal is set high upon a Master Reset Operation. The $\overline{\text{OUT 1}}$ signal is forced to its inactive state (high) during loop mode operation.

Pin Description (Continued)

Pin No.	Symbol	I/O	Description
35	MR	I	This input is buffered with a TTL-compatible Schmitt Trigger with 0.5V typical hysteresis when high, it clears all the registers and FIFOs (except the Receiver Buffer, Transmitter Holding, Scratch Pad Register and Divisor Latches), and the control logic of the ACE. Also the state of various output signals (SOUT, INTRPT, $\overline{OUT\ 1}$, $\overline{OUT\ 2}$, $\overline{RTS}$, $\overline{DTR}$) are affected by an active MR input (Refer to Table 1)
36	$\overline{CTS}$	I	The $\overline{CTS}$ signal is a MODEM control function input whose conditions can be tested by the CPU by reading bit 4 (CTS) of the MODEM Status Register. Bit 0 (DCTS) of the MODEM Status Register indicates whether the $\overline{CTS}$ input has changed state since the previous reading of the MODEM Status Register. $\overline{CTS}$ has no effect on the Transmitter. Note: Whenever the $\overline{CTS}$ bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status interrupt is enabled.
37	$\overline{DSR}$	I	When low, this indicates that the MODEM or data set is ready to establish the communications link and transfer data with the ACE, the $\overline{DSR}$ signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 5 (DSR) of the MODEM Status Register. Bit 1 (DDSR) of the MODEM Status Register indicates whether the $\overline{DSR}$ input has changed state since the previous reading of the MODEM Status Register. Note: Whenever the DSR bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status interrupt is enabled.
38	$\overline{DCD}$	I	When low, indicates that the data carrier has been detected by the MODEM or data set. The $\overline{DCD}$ signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 7 (DCD) of the MODEM Status Register. Bit 3 (DDCD) of the MODEM Status Register indicates whether the $\overline{DCD}$ input has changed state since the previous reading of the MODEM Status Register. $\overline{DCD}$ has no effect on the receiver. Note: Whenever the $\overline{DCD}$ bit of the MODEM Status Register changes state, an interrupt is generated if the Modem Status interrupt is enabled.
39	$\overline{RI}$	I	When low, indicates that a telephone ringing signal has been received by the MODEM or data set. The $\overline{RI}$ signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 6 (RI) of the MODEM Status Register. Bit 2 (TERI) of the MODEM Status Register indicates whether the $\overline{RI}$ input has changed from a low to a high state since the previous reading of the MODEM Status Register. Note: Whenever the RI bit of the MODEM Status Register changes from a high to a low state, an interrupt is generated if the MODEM Status Register is enabled.
40	V_{CC}		+5V Power Supply.

Table I. ACE Reset Functions

Register/Signal	Reset Control	Reset State
Interrupt Enable Register	Master Reset	All Bits Low (0–3 forced and 4–7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High, Bits 1–3, 7 forced low Bits 4–6 are Permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low, Except Bits 5 & 6 are High
MODEM Status Register	Master Reset	Bits 0 – 3 Low Bits 4–7 – Input Signal
SOUT	Master Reset	High
INTRPT (RCVR Errs)	Read LSR/MR	Low
INTRPT (RCVR Data Ready)	Read RBR/MR	Low
INTRPT (THRE)	Read IIR/Write THR/MR	Low
INTRPT (Modem Status Changes)	Read MSR/MR	Low
$\overline{OUT\ 2}$	Master Reset	High
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
$\overline{OUT\ 1}$	Master Reset	High
RCVR FIFO	MR/FCR1 • FCR0/ΔFCR0	All Bits Low
XMIT FIFO	MR/FCR1 • FCR0/ΔFCR0	All Bits Low
FIFO Control	Master Reset	All Bits Low

Register Descriptions

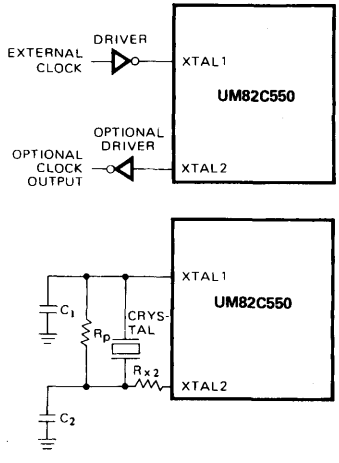
The system programmer may access or control any of the ACE registers summarized in Table II via the CPU. These registers are used to control ACE operations and to transmit and receive data.

Programmable Baud Generator

The ACE contains a programmable Baud Generator that is capable of taking any clock input (DC to 8.0 MHz) and dividing it by any divisor from 2 to $2^{16} - 1$). 4 MHz is the highest input clock frequency recommended when the divisor = 1. The output frequency of the Baud Generator is 16 x the Baud [divisor # = (frequency input) ÷ (baud rate x 16)]. Two 8-bit latches store the divisor in a 16-digit binary format. These Divisor Latches must be loaded during initialization in order to ensure desired operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables III, IV and V illustrate the divisors for use with crystal frequencies of 1.8432 MHz, 3.072 MHz and 8 MHz, respectively. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen.

Typical Oscillator Applications



Typical Crystal Oscillator Network

Crystal	R_p	R_{x2}	C_1	C_2
3.1 MHz	1 MΩ	1.5K	10-30 pF	40-60 pF
1.8 MHz	1 MΩ	1.5K	10-30 pF	40-60 pF

Bit No.	Register Address											
	0 DLAB = 0	0 DLAB = 0	1 DLAB = 0	2	2	3	4	5	6	7	0 DLAB = 1	1 DLAB = 1
	Receiver Buffer Register (Read Only)	**Transmitter Holding Register (Write Only)**	**Interrupt Enable Register**	**Interrupt Ident Register (Read Only)**	**FIFO Control Register (Write Only)**	**Line Control Register**	**MODEM Control Register**	**Line Status Register**	**MODEM Status Register**	**Scratch Register**	**Divisor Latch (LS)**	**Divisor Latch (MS)**
	RBR	THR	IER	IIR	FCR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Data Bit 0 (Note 1)	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" If Interrupt Pending	FIFO Enable	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to send (DCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	RCVR FIFO Reset	Word Length Select Bit 1 (WLSI)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (I)	XMIT FIFO Reset	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	Interrupt ID Bit (2) (Note 2)	DMA Mode Select	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Data Carrier Detect (DDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	RCVR Trigger (LSB)	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	FIFO Enable (Note 2)	RCVR Trigger (MSB)	Divisor Latch Access Bit (DLAB)	0	Error In RCVR FIFO (Note 2)	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

Note 1: Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Note 2: These bits are always 0 in the Character mode.

Table 11 Summary of Registers

Table III. Baud Rates Using 1.8432 MHz Crystal

Desired Baud Rate	Divisor Used to Generate 16 x Clock	Percent Error Difference Between Desired and Actual
50	2304	–
75	1536	–
110	1047	0.026
134.5	857	0.058
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.69
2400	48	–
3600	32	–
4800	24	–
7200	16	–
9600	12	–
19200	6	–
38400	3	–
56000	2	2.86

Table IV. Baud Rates Using 3.072 MHz Crystal

Desired Baud Rate	Divisor Used to Generate 16 x Clock	Percent Error Difference Between Desired and Actual
50	3840	–
75	2560	–
110	1745	0.026
134.5	1428	0.034
150	1280	–
300	640	–
600	320	–
1200	160	–
1800	107	0.312
2000	96	–
2400	80	–
3600	53	0.628
4800	40	–
7200	27	1.23
9600	20	–
19200	10	–
38400	5	–

Table V. Baud Rates Using 8 MHz Crystal

Desired Baud Rate	Divisor Used to Generate 16 x Clock	Percent Error Difference Between Desired and Actual
50	10000	–
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	3333	0.010
300	1667	0.020
600	833	0.040
1200	417	0.080
1800	277	0.080
2000	250	–
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
	2	2.344

Interrupt Enable Register

This 8-bit register enables the four types of interrupts of the ACE to separately activate the chip interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are indicated in Table II and are described below.

Bit 0: This bit enables the Received Data Available Interrupt (and timeout interrupts in the FIFO mode) when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

MODEM Control Register

This 8-bit register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in Table II and are described below.

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.

Bit 1: This bit controls the Request to Send $\overline{RTS}$ output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the Output 1 ($\overline{OUT\ 1}$) signal, which is an auxiliary user-designated output. Bit 2 affects the $\overline{OUT\ 1}$ output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the Output 2 ($\overline{OUT\ 2}$) signal, which is an auxiliary user-desigated output. Bit 3 affects the $\overline{OUT\ 2}$ output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a local loopback feature for diagnostic testing of the ACE. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to the Marking (logic 1) state: the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$) are disconnected; and the four MODEM Control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT\ 1}$, and $\overline{OUT\ 2}$) are internally connected to the four MODEM Control inputs, and the MODEM Control output pins are forced to their inactive state (high). In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit- and received-data paths of the ACE.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. Their sources are external to the part. The MODEM Control Interrupts are also operational, but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

Bit 5 through 7: These bits are permanently set to logic 0.

Interrupt Identification Register

The ACE has an on-chip interrupt capability that allows for flexibility in interfacing popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the ACE prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2): Timeout (priority 2, FIFO Mode only); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending and the type of that interrupt is stored in the Interrupt Identification Register (IIR). When addressed during chip-select time the IIR freezes the highest priority interrupt pending and no other interrupts change the IIR even though they are recorded, until that particular interrupt is serviced by the CPU. The contents of the IIR are indicated in Table II and are described below.

Bit 0: This bit can be used in either a prioritized interrupt or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table VI.

Bit 3: In the Character mode this bit is 0. In the FIFO mode this bit is set along with bit 2 when a timeout interrupt is pending.

Bits 4 through 6: These three bits of the IIR are always logic 0.

Bit 7: This bit is set when FCR0 = 1.

Table VI. Interrupt Control Functions

FIFO Mode Only	Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 3	Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	0	1	–	None	None	–
0	1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available or Trigger Level Reached	Reading the Receiver Buffer Register or the FIFO Drops Below the Trigger Level
1	1	0	0	Second	Character Timeout Indication	No Characters Have Been Removed From or Input to the RCVR FIFO During the Last 4 Char. Times and There is at Least 1 Char. in it During This Time	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (If source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

Line Status Register

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of the Line Status Register are indicated in Table II and are described below.

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register or the FIFO. Bit 0 is reset to a logic 0 by reading all of the data in the Receiver Buffer Register or the FIFO.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register. If the FIFO mode data continues to fill the FIFO beyond the trigger level an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. OE is indicated to the CPU as soon as it happens. The character in the shift register is overwritten, but it is not transferred to the FIFO.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level). The FE indicator is reset whenever the CPU reads the contents of the Line Status indicator. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO.

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits). The BI indicator is reset whenever the CPU reads the contents of the Line Status indicator. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO. When break occurs only one zero character is loaded into the FIFO. The next character transfer is enabled after SIN goes to the marking state and receives the next valid start bit.

Note: Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the ACE is ready to accept a new character for transmission. In addition, this bit causes the ACE to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU. In the FIFO mode this bit is set when the XMIT FIFO is empty, it is cleared when at least 1 byte is written to the XMIT FIFO.

Bit 6: This bit is the Transmitter Empty (TEMT) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty, it is reset to a logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode this bit is set to one whenever the transmitter FIFO and shift register are both empty.

Bit 7: In the Character mode this is a 0. In the FIFO mode LSR7 is set when there is at least one parity error framing error or break indication in the FIFO LSR7 is cleared when the CPU reads the LSR, if there are no subsequent errors in the FIFO.

FIFO Control Register

This is a write only register at the same location as the IIR the IIR is a read only register. This register is used to enable the FIFOs, clear the FIFOs, set the RCVR FIFO trigger level, and select the type of DMA signalling.

Bit 0: Writing a 1 to FCR0 enables both the XMIT and RCVR FIFOs. Resetting FCR0 will clear all bytes in both FIFOs. When changing from FIFO Mode to Character Mode and vice versa data is automatically cleared from the FIFOs. This bit must be a 1 when other FCR bits are written to or they will not be programmed.

Bit 1: Writing a 1 to FCR1 clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.

Bit 2: Writing a 1 to FCR2 clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.

Bit 3: Setting FCR3 to a 1 will cause the RXRDY and TXRDY pins to change from mode 0 to mode 1 if FCR0 = 1 (see description of RXRDY and TXRDY pins.)

Bit 4, 5: FCR4 to FCR5 are reserved for future use.

Bit 6, 7: FCR6 and FCR7 are used to set the trigger level for the RCVR FIFO interrupt.

7	6	RCVR FIFO Trigger Level (Bytes)
0	0	01
0	1	04
1	0	08
1	1	14

Line Control Register

The system programmer specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format, the programmer may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. The contents

of the Line Control Register are indicated in Table II and are described below.

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits in each transmitted character. If bit 2 is a logic 0, one Stop bit is generated in the transmitted data. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one and a half stop bits are generated. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two Stop bits are generated. The Receiver checks the first Stop-bit only, regardless of the number of Stop bits selected.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) on checked (received data) between the last data word bit and Stop bit of the serial data (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1s is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bits 3, 4 and 5 are logic 1 the Parity bit is transmitted and checked by the receiver as a logic 0. If bits 3 and 5 are 1 and bit 4 is a logic 0 then the Parity bit is transmitted and checked as a logic 1.

Bit 6: This bit is the Break Control bit. When it is set to a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state. The break is disabled by setting bit 6 to a logic 0. The Break Control bit acts only on SOUT and has no effect on the transmitter logic.

Note: This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break.

1. Load in all Os. a pad character in response to THRE.
2. Set break after the next THRE.
3. Wait for the transmitter to be idle. (TEMT = 1), and clear break when normal transmission has to be restored.

During the break the Transmitter can be used as a character timer to accurately establish the break duration.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Generater during a Read or write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

Modem Status Register

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in Table II and described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from a low to a high state.

Bit 3: This bit is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the $\overline{DCD}$ input to the chip has changed state.

Note: Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send ($\overline{CTS}$) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.

Bit 5: This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to DTR in the MCR.

Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to $\overline{OUT\ 1}$ in the MCR.

Bit 7: This bit is the complement of the Data Carrier Detect ($\overline{DCD}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 2 of the MCR.

Scratchpad Register

This 8-bit Read/Write Register does not control the ACE in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

FIFO Interrupt Mode Operation

When the RCVR FIFO and receiver interrupts are enabled (FCR0 = 1, IER0 = 1) RCVR interrupts will occur as follows:

A. The receive data available interrupt will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.
B. The IIR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.
C. The receiver line status interrupt (IIR = 06), as before, has higher priority than the received data available (IIR = 04) interrupt.
D. The data ready bit (LSR0) is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

When the XMIT FIFO and transmitter interrupts are enabled (FCR0 = 1, IER1 = 1). XMIT interrupts will occur as follows:

A. The transmitter holding register interrupt (02) occurs when the XMIT FIFO is empty; it is cleared as soon as the transmitter holding register is written to (1 to 16 characters may be written to the XMIT FIFO while servicing this interrupt) or the IIR is read.
B. The transmitter FIFO empty indications will be delayed character time minus the last stop bit time whenever the following occurs. THRE = 1 and there have not been at least two bytes at the same time in the transmit FIFO since the last THRE = 1. The first transmitter interrupt after changing FCR0 will be immediate, if it is enabled.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts will occur as follows:

A. A FIFO timeout interrupt will occur, if the following conditions exist
   - at least one character is in the FIFO
   - the most recent character received was longer than 4 continuous character times ago (if 2 stop bits are programmed the second one is included in this time delay)
   - the most recent CPU read of the FIFO was longer than 4 continuous character times ago.

This will cause a maximum character received to interrupt issued delay of 16 ms at 300 BAUD with a 12 bit character.

B. Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baud rate).
C. When a timeout interrupt has occurred it is cleared and the time reset when the CPU reads one character from the RCVR FIFO.
D. When a timeout interrupt has not occurred the timeout timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

FIFO Polled Mode Operation

With FCR0 = 1 resetting IER0, IER1, IER2, IER3 or all to zero puts the ACE in the FIFO Polled Mode of operation. Since the RCVR and XMITTER are controlled separately either one or both can be in the polled mode of operation.

In this mode the user's program will check RCVR and XMITTER status via the LSR as stated previously.

LSR0 will be set as long as there is one byte in the RCVR FIFO.
LSR1 to LSR4 will specify which error(s) has occured.
Character error status is handled the same way as when in the interrupt mode, the IIR is not affected since IER2 = 0.
LSR5 will indicate when the XMIT FIFO is empty.
LSR6 will indicate that both the XMIT FIFO and shift register are empty.
LSR7 will indicate whether there are any errors in the RCVR FIFO.

There is no trigger level reached or timeout condition indicated in the FIFO Polled Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

Absolute Maximum Ratings*

Temperature Under Bias . . . . . 0°C to +70°C
Storage Temperature . . . . . -65°C to +150°C
All input or Output Voltages with Respect to V_{SS}
. . . . . -0.5 V to +7.0 V
Power Dissipation . . . . . 60 mW

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = 0°C to +70°C, V_{CC} = +5V ± 5%, V_{SS} = 0 V, unless otherwise specified.)

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{ILX}	Clock Input Low Voltage		-0.5	0.8	V
V_{IHX}	Clock Input High Voltage		2.0	V_{CC}	V
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{IH}	Clock Input High Voltage		2.0	V_{CC}	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA on all*		0.4	V
V_{OH}	Output High Voltage	I_{OL} = -1.0 mA*	2.4		V
I_{CC} (AV)	Avg Power Supply Current (V_{CC})	V_{CC} = 5.25V, T_A = 25°C No Loads on output SIN, DSR, RLSD, CTS, RI = 2.0V All other inputs = 0.8 V		10	mA
I_{IL}	Input Leakage	V_{CC} = 5.25V, V_{SS} = 0V All other pins floating. VIN = 0V, 5.25V		± 10	μA
I_{CL}	Clock Leakage			± 10	μA
I_{OZ}	TRI-STATE Leakage	V_{CC} = 5.25V, V_{SS} = 0V V_{OUT} = 0V, 5.25V !) Chip deselected 2) WRITE Mode, chip selected		± 20	μA
V_{ILMR}	MR Schmitt V_{IL}			0.8	V
V_{IHMR}	MR Schmitt V_{IH}		2.0		V

*Does not apply to XTAL 2

Capacitance (T_A = 25°C, V_{CC} = V_{SS} = 0V)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C_{XTAL2}	Clock Input Capacitance	f_c = 1 MHz Unmeasured pins returned to V_{SS}		15	20	pF
C_{XTAL1}	Clock Output Capacitance			20	30	pF
C_{IN}	Input Capacitance			6	10	pF
C_{OUT}	Output Capacitance			10	20	pF

AC Characteristics (T_A = 0°C to –70°C, V_{CC} = +5V ± 5%)

Symbol	Parameter	Conditions	Min.	Max.	Unit
t_{AH}	Address Hold Time		0		ns
t_{AR}	$\overline{DISTR}$/DISTR Delay from Address	(Note 1)	30		ns
t_{AS}	Address Setup Time		60		ns
t_{AW}	Address Strobe Width		60		ns
t_{CH}	Chip Select Hold Time		0		ns
t_{CS}	Chip Select Setup Time		60		ns
t_{CSR}	$\overline{DISTR}$/DISTR Delay from Chip Select	(Note 1)	50		ns
t_{CSW}	$\overline{DOSTR}$/DOSTR Delay from Select	(Note 1)	50		ns
t_{DD}	$\overline{DISTR}$/DISTR to Driver Enable/Disable	@100 pF loading (Note 3)		60	ns
t_{DDA}	$\overline{DOSTR}$/DOSTR Delay from Address	(Note 1)	30		ns
t_{DDD}	Delay from $\overline{DISTR}$/DISTR to Data	@100 pF loading		125	ns
t_{DH}	Data Hold Time		30		ns
t_{DIW}	$\overline{DISTR}$/DISTR Strobe Width		125		ns
t_{DOW}	DOSTR/DOSTR Strobe Width		100		ns
t_{DS}	Data Setup Time		30		ns
t_{HZ}	DISTR/DISTR to Floating Data Delay	@100 pF loading (Note 3)	0	100	ns
t_{MRW}	Master Reset Pulse Width		5		μs
t_{RA}	Address Hold Time from $\overline{DISTR}$/DISTR	(Note 1)	20		ns
t_{RC}	Read Cycle Delay		125		ns
t_{RCS}	Chip Select Hold Time from $\overline{DISTR}$/DISTR	(Note 1)	20		ns
t_{WA}	Address Hold Time from $\overline{DOSTR}$/DOSTR	(Note 1)	20		ns
t_{WC}	Write Cycle Delay		150		ns
t_{WCS}	Chip Select Hold Time from $\overline{DOSTR}$/DOSTR	(Note 1)	20		ns
t_{XH}	Duration of Clock High Pulse	External Clock (8.0 MHz Max.)	55		ns
t_{XL}	Duration of Clock Low Pulse	External Clock (8.0 MHz Max.)	55		ns
RC	Read Cycle = $t_{AR} + t_{DIW} + t_{RC}$		280		ns
WC	Write Cycle = $t_{DDA} + t_{DOW} + t_{WC}$		280		ns
Baud Generator					
N	Baud Divisor		1	$2^{16}-1$	
t_{BHD}	Baud Output Positive Edge Delay	100 pF Load		175	ns

Note 1: Applicable only when $\overline{ADS}$ is tied low.

AC Characteristics (Continued)

Symbol	Parameter	Conditions	Min.	Max.	Unit
t_{BLD}	Baud Output Negative Edge Delay	100 pF Load		175	ns
t_{HW}	Baud Output Up Time	f_x = 8.0MHz ÷ 2,100pF Load	75		ns
t_{LW}	Baud Output Down Time	f_x = 8.0MHz ÷ 2,100pF Load	100		ns
Receiver					
t_{RINT}	Delay from $\overline{DISTR}$/DISTR (RD RBR/RDLSR) to Reset Interrupt	100 pF Load		1	μs
t_{SCD}	Delay from RCLK to Sample Time			2	μs
t_{SINT}	Delay from Stop to Set Interrupt	(Note 2)	1	1	RCLK Cycles
Transmitter					
t_{HR}	Delay from $\overline{DOSTR}$/DOSTR (WR THR) to Reset Interrupt	100 pF Load		175	ns
t_{IR}	Delay from $\overline{DISTR}$/DISTR (RD IIR) to Reset Interrupt (THRE)	100 pF Load		250	ns
t_{IRS}	Delay from Initial INTR Reset to Transmit Start		8	24	RCLK Cycles
t_{SI}	Delay from Initial Write to Interrupt	(Note 4)	16	32	RCLK Cycles
t_{STI}	Delay from Stop to Interrupt (THRE)	(Note 4)	8	8	RCLK Cycles
t_{SXA}	Delay from Start to TXRDY active	100 pF Load		8	RCLK Cycles
t_{WXI}	Delay from Write to TXRDY inactive	100 pF Load		195	ns
Modem Control					
t_{MDO}	Delay from $\overline{DOSTR}$/DOSTR (WR MCR) to Output	100 pF Load		200	ns
t_{RIM}	Delay to Reset Interrupt from $\overline{DISTR}$/ DISTR (RD MSR)	100 pF Load		250	ns
t_{SIM}	Delay to Set Interrupt from MODEM Input	100 pF Load		250	ns

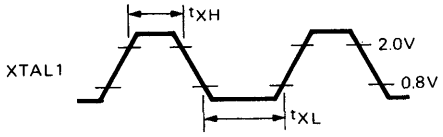
Note 2: In the FIFO mode (FCR0 = 1) the trigger level and timeout interrupts, the receiver data available indication, the active RXRDY indication and the overrun error indication will be delayed 9 RCLKs. Status indicators (PE, FE, BI) will be delayed 9 RCLKs after the first byte has been received. For subsequently received bytes these indicators will be updated immediately after RDRBR goes inactive.

Notes 3: Charge and discharge time is determined by V_{OL}, V_{OH} and the external loading.

Note 4: This delay will be lengthened by 1 character time, minus the last stop bit time if the transmitter interrupt delay circuit is active. (See FIFO Interrupt Mode Operation).

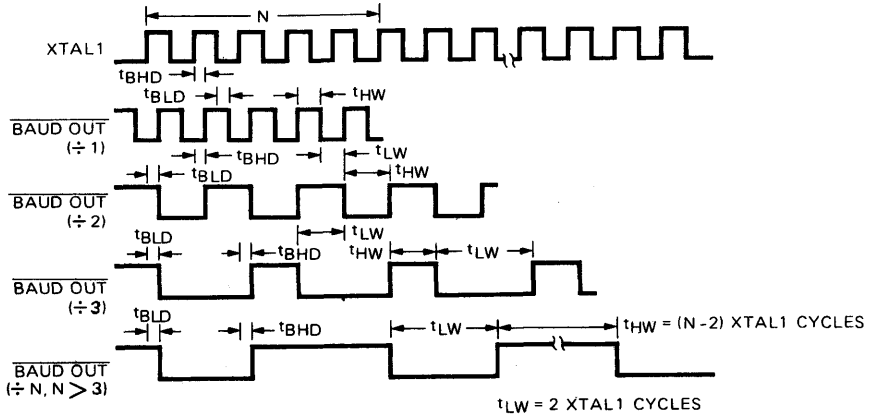
Timing Waveforms

EXTERNAL CLOCK INPUT (8.0 MHz MAX.)

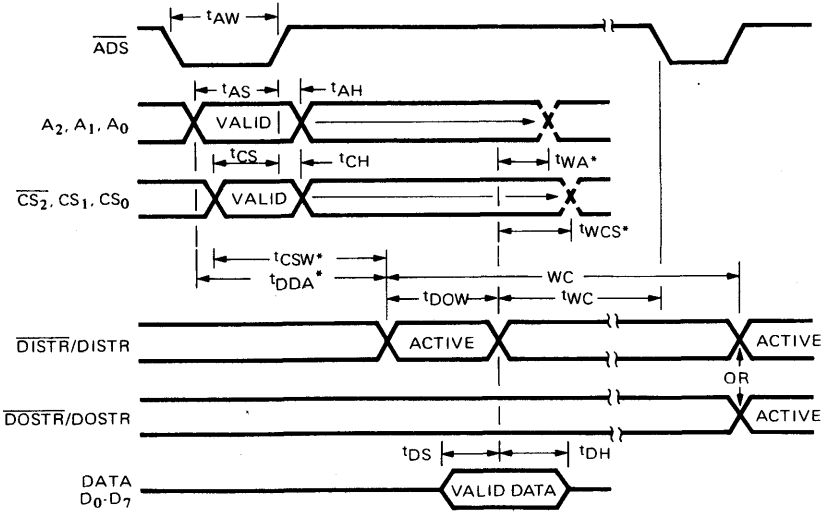


AC TEST POINTS

$\overline{\text{BAUDOUT}}$ TIMING



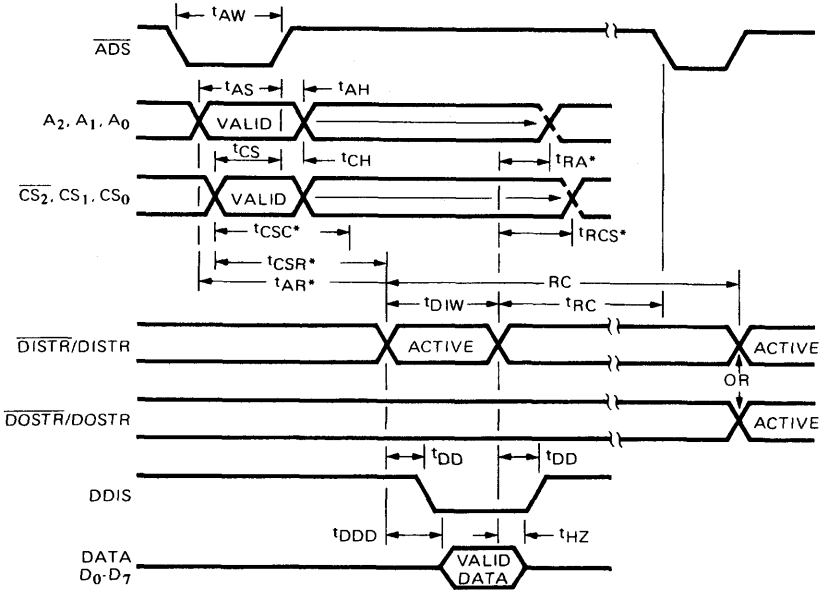
WRITE CYCLE



* Applicable Only When $\overline{\text{ADS}}$ is Tied Low.

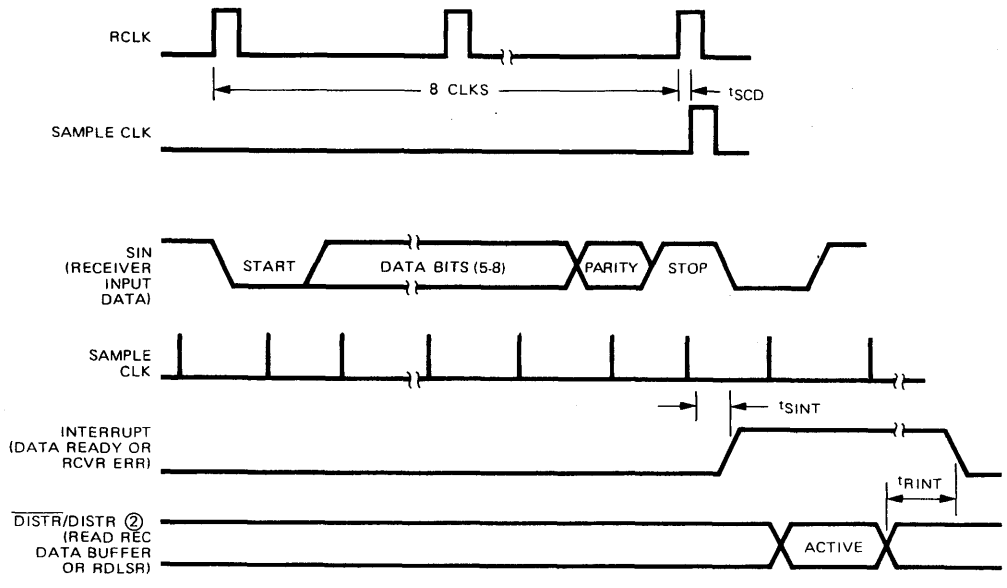
Timing Waveforms (Continued)

READ CYCLE



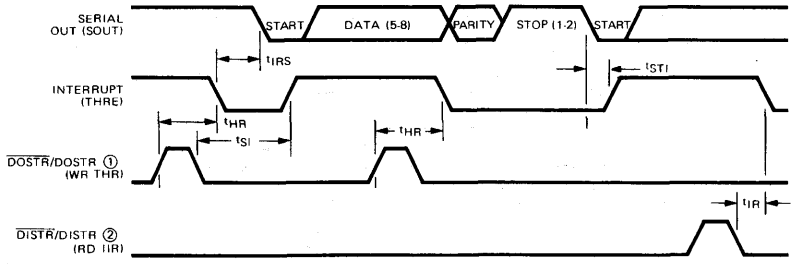
* Applicable Only When $\overline{ADS}$ is Tied Low.

RECEIVER TIMING

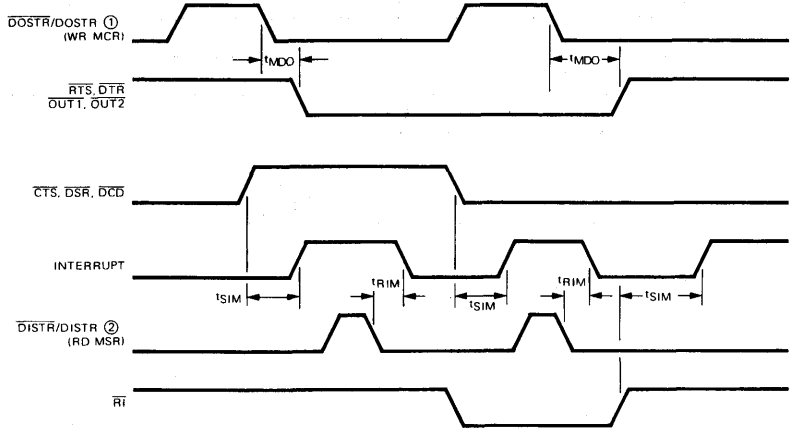


Timing Waveforms (Continued)

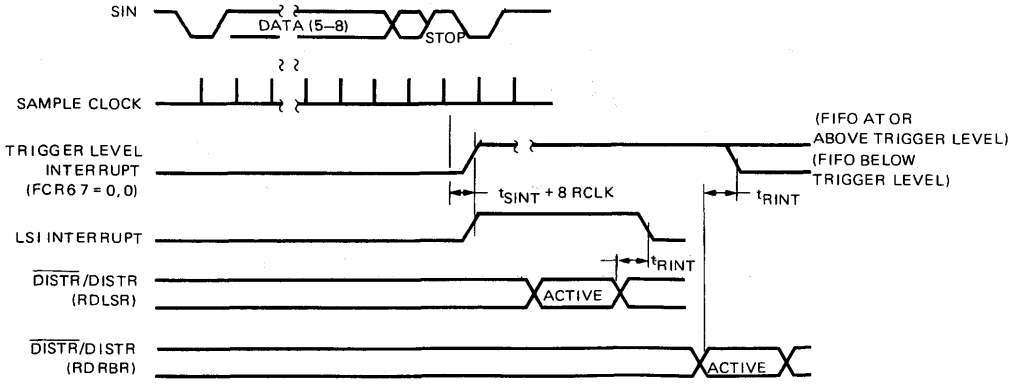
TRANSMITTER TIMING



MODEM CONTROL TIMING

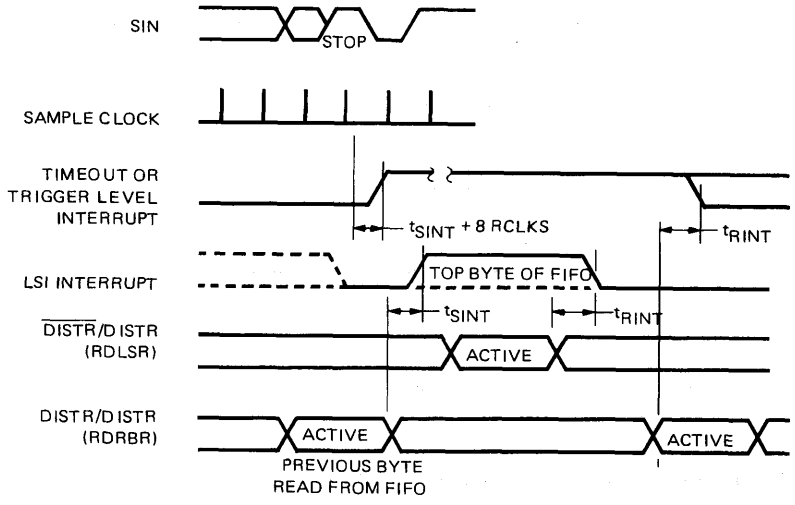


RCVR FIFO First Byte (This Sets RDR)

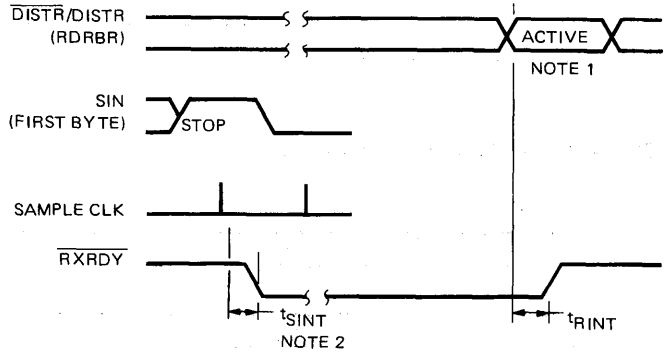


Timing Waveforms (Continued)

RCVR FIFO Bytes Other Than The First Byte (RDR is Already Set)



Receiver Ready (Pin 29) FCR0 = 0 or FCR0 = 1 and FCR3 = 0 (Mode 0)

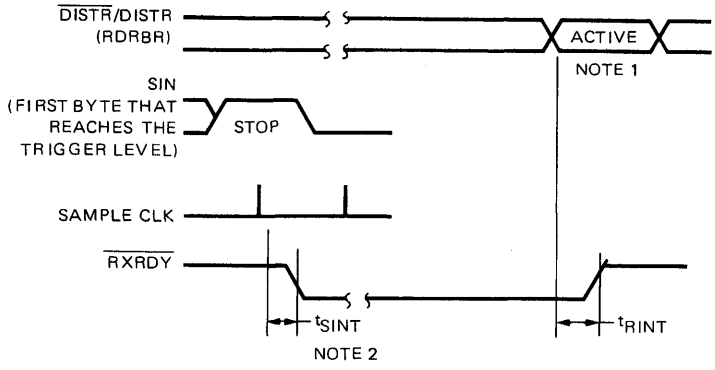


Note 1: This is the reading of the last byte in the FIFO.

Note 2: If FCR0 = 1, t_{SINT} = 8 RCLKs

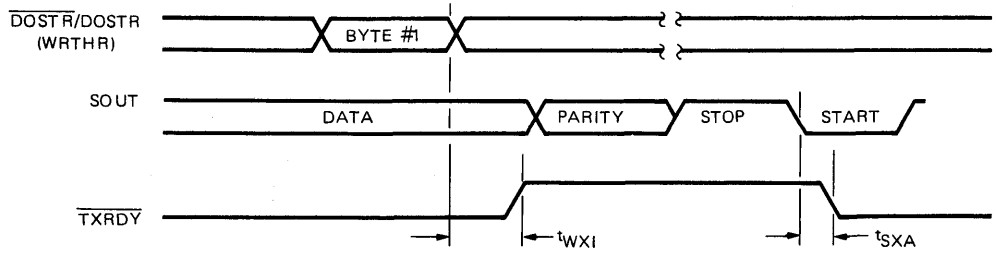
Timing Waveforms (Continued)

Receiver Ready (Pin 29) FCR0 = 1 and FCR3 = 1 (Mode 1)

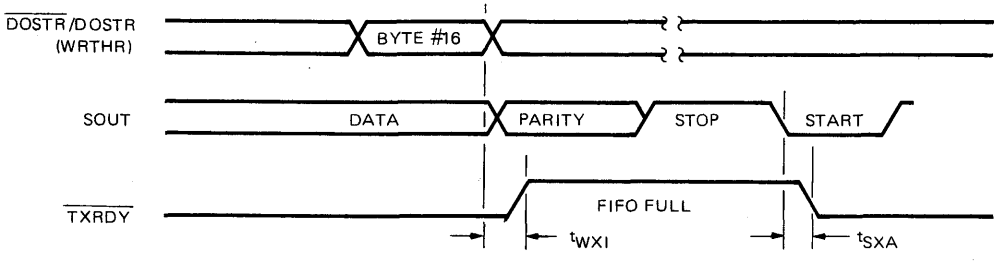


Note 1: This is the reading of the last byte in the FIFO.
Note 2: If FCR0 = 1, t_{SINT} = 9 RCLKS

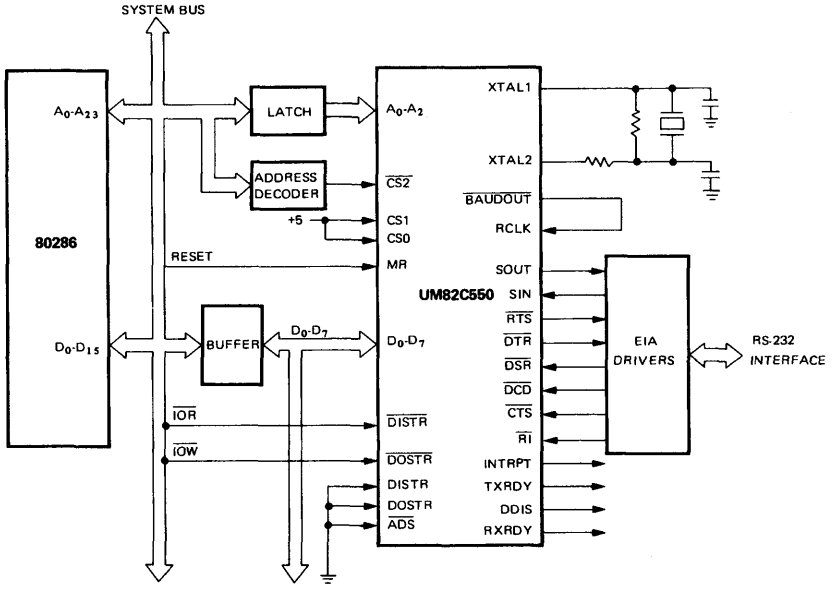
Transmitter Ready (Pin 24) FCR0 = 0 or FCR0 = 1 and FCR3 = 0 (Mode 0)



Transmitter Ready (Pin 24) FCR0 = 1 and FCR3 = 1 (Mode 1)



Application Circuit



Ordering Information

Part Number	Package
UM82C550	40L DIP
UM82C550L	44L PLCC

UM82C8167

Real-Time Clock(RTC)

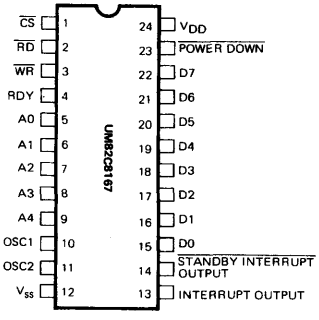
Features

- Microprocessor compatible (8-bit data bus)
- Milliseconds through month counters
- 56 bits of RAM with comparator to compare the real time counter to the RAM data
- 2 INTERRUPT OUTPUTS with 8 possible interrupt signals
- Single +5V power supply
- POWER DOWN input that disables all inputs and outputs except for one of the interrupts
- Status bit to indicate rollover during a read
- 32,768 Hz crystal oscillator
- Four-year calendar (no leap year)
- 24-hour clock
- 24 pin dual-in-line package

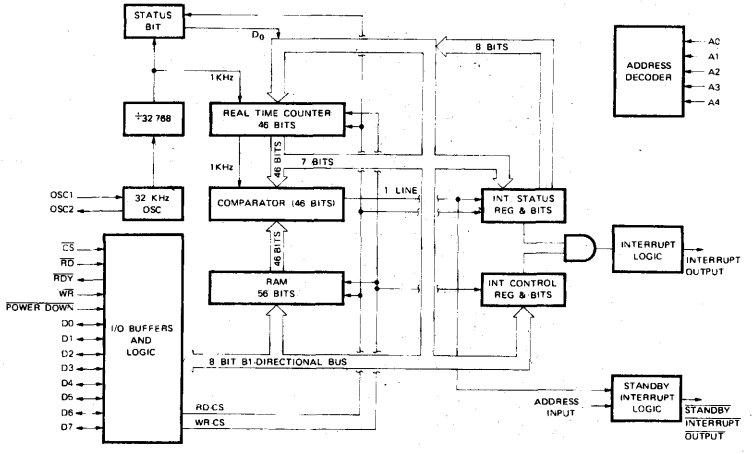
General Description

The UM82C8167 is a Si-gate CMOS LSI used as a real time clock in microprocessor systems. This product includes an addressable real time counter, 56 bits of static RAM and two interrupt outputs. User can disable the chip from the rest of the system for standby low power operation by use of a POWER DOWN input. With an on chip oscillator circuit, it can generate the 32,768 Hz time base.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Voltage at All Inputs and Outputs

. . . . . V_{DD} +0.3 to V_{SS} −0.3

Operating Temperature. . . . . −25°C to +85°C

Storage Temperature . . . . . −65°C to +150°C

$V_{DD} - V_{SS}$ 6V

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(T_A = −25°C to +85°C, V_{SS} = 0V)

Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage V_{DD} V_{DD} (Note 1)	 Outputs Enabled Power Down Mode	 4.0 2.0		 5.5 5.5	 V V
Supply Current I_{DD}, Static I_{DD}, Dynamic I_{DD}, Dynamic	 Outputs TRI-STATE, f_{IN} = DC, V_{DD} = 5.5V Outputs TRI-STATE, f_{IN} = 32 KHz, V_{DD} = 5.5V $V_{IH} \geq V_{DD} - 0.3V$, $V_{IL} \leq V_{SS} + 0.3V$ Outputs TRI-STATE, f_{IN} = 32 KHz V_{DD} = 5.5V, V_{IH} = 2.0V, V_{IL} = 0.8V			 10 20 5	 μA μA mA
Input Voltage V_{IL} Logical Low V_{IH} Logical High		 0.0 2.0		 0.8 V_{DD}	 V V
I_L Input Leakage Current	$V_{SS} \leq V_{IN} \leq V_{DD}$	−1		1	μA
Output Voltage V_{OL} Logical Low V_{OH} Logical High TRI-STATE®	(I/O and Interrupt Output) V_{DD} = 4.75V, I_{OL} = 1.6mA V_{DD} = 4.75V, I_{OH} = −400μA, I_{OH} = −10μA V_{OUT} = 0V, V_{OUT} = V_{DD}	 2.4 0.8 V_{DD}		 0.4 −1 1	 V V V μA μA
Output Impedance Logical Low, Sink Logical High, Leakage	(Ready and Standby Interrupt Output) V_{DD} = 4.75V, I_{OL} = 1.6mA $V_{OUT} \leq V_{DD}$			 0.4 10	 V μA

Note 1: To insure that no illegal data is read from or written into the chip during power up, the power down input should be enabled only after all other lines (Read, Write, Chip Select, and Data Bus) are valid.

AC Characteristics

Interrupt Timing

(0°C ≤ T_A ≤ 70°C, 4.5V ≤ V_{DD} ≤ 5.5V, V_{SS} = 0V)

Symbol	Parameter	Min.	Max.	Unit
t_{INTON}	Status Register Clock to INTERRUPT OUTPUT (Pin 13) High (Note 1)		5	μs
t_{SBYON}	Compare Valid to STANDBY INTERRUPT (Pin 14) Low (Note 1)		5	μs
t_{INTOFF}	Trailing Edge of Status Register Read to INTERRUPT OUTPUT Low		5	μs
t_{SBYOFF}	Trailing Edge of Write Cycle 9d0 = 0; Address = 16 H) to STANDBY INTERRUPT Off (high Impedance State)		5	μs

Note 1: The status register clocks are: The corresponding counter's rollover to its reset state or the compare becoming valid. The compare becomes valid 61μs after the 1/10,000 of a second counter is clocked, if the real time counter data matches the RAM data.

Read Cycle Timing

($0°C \leq T_A \leq 70°C$, $4.5V \leq V_{DD} \leq 5.5V$, $V_{SS} = 0V$)

Symbol	Parameter	Min.	Max.	Unit
t_{AR}	Address Bus Valid to Read Strobe	100		ns
t_{CSR}	Chip Select to Read Strobe	0		ns
t_{RRY}	Read Strobe to Ready Strobe		150	ns
t_{RYD}	Ready Strobe to Data Valid		800	ns
t_{AD}	Address Bus Valid to Data Valid		1050	ns
t_{RH}	Data Hold Time From Trailing Edge of Read Strobe	0		ns
t_{HZ}	Trailing Edge of Read Strobe to TRI-STATE Mode		250	ns
t_{RYH}	Read Hold Time after Ready Strobe	0		ns
t_{RA}	Address Bus Hold Time from Trailing Edge of Read Strobe	50		ns
t_{RYDV}	Rising Edge of Ready to Data Valid		100	ns

Note 2: If $t_{AR} = 0$ and Chip Select, Address Valid or Read are coincident then they must exist for 1050 ns.

Write Cycle Timing

($0°C \leq T_A \leq 70°C$ $4.5V \leq V_{DD} \leq 5.5V$, $V_{SS} = 0V$)

Symbol	Parameter	Min.	Max.	Unit
t_{AW}	Address Valid to Write Strobe	100		ns
t_{CSW}	Chip Select to Write Strobe	0		ns
t_{DW}	Data Valid before Write Strobe	100		ns
t_{WRY}	Write Strobe to Ready Strobe		150	ns
t_{RY}	Ready 1 Strobe Width		800	ns
t_{RYH}	Write Hold Time after Ready Strobe	0		ns
t_{WD}	Data Hold Time after Write Strobe	50		ns
t_{WA}	Address Hold Time after Write Strobe	50		ns

Note 3: If data changes while CS and WR are low, then it must remain coincident within 1050 ns after the data change to ensure a valid writing.

Data bus loading is 100 pF.

Ready output loading is 50 pF and 3 kΩ pull-up.

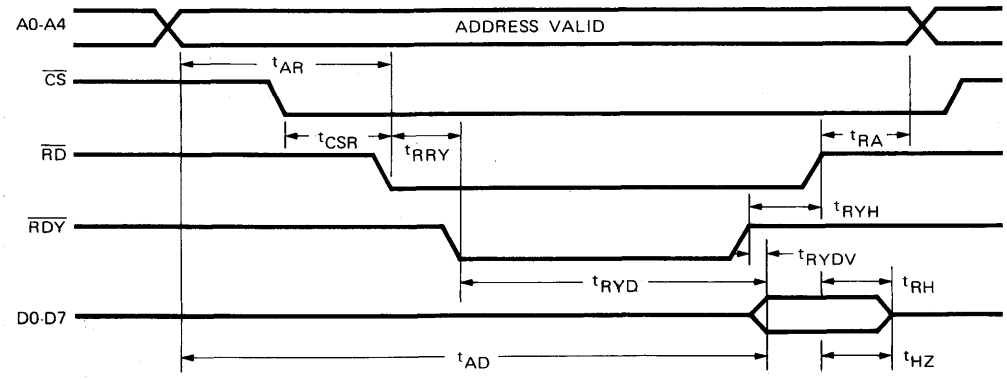
Input and output AC timing levels:

Logical one = 2.0V

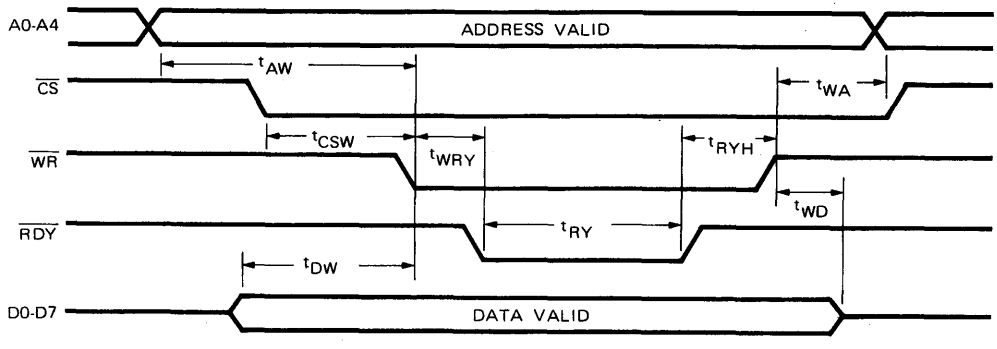
Logical zero = 0.8V

Timing Waveforms

READ CYCLE TIMING



WRITE CYCLE TIMING



Functional Description

Real Time Counter

The real time counter is divided into 4-bit digits with 2 digits being accessed during any read or write cycle. Each digit represents a BCD number and is defined in Table 1. Any unused bits are held at a logical zero and ignored during a write. An unused bit is any bit not necessary to provide a full BDC number. For example, tens of hours can not legally exceed the number 2, thus only 2 bits are necessary to define the tens of hours. The other 2 bits in the tens of hours digit are unused. The unused bits are designated in Table 1 as dashes.

The addressable portion of the counter is from milliseconds to months. The counter itself is a ripple counter. The ripple delay is less than 60μs above 4.0V and 300μs at 2.0V.

Table 1. Real Time Counter Format

Counter Addressed		Units D0	D1	D2	D3	Max. BCD Code	Tens D4	D5	D6	D7	Max. BCD Code
1/10,000 of Seconds	(00_H)	–	–	–	–		D4	D5	D6	D7	9
Hundredths and Tenths Sec	(01_H)	D0	D1	D2	D3	9	D4	D5	D6	D7	9
Seconds	(02_H)	D0	D1	D2	D3	9	D4	D5	D6	–	5
Minutes	(03_H)	D0	D1	D2	D3	9	D4	D5	D6	–	5
Hours	(04_H)	D0	D1	D2	D3	9	D4	D5	–	–	2
Day of the Week	(05_H)	D0	D1	D2	–	7	–	–	–	–	0
Day of the Month	(06_H)	D0	D1	D2	D3	9	D4	D5	–	–	3
Month	(07_H)	D0	D1	D2	D3	9	D4	–	–	–	1

(–) Indicates unused bits

RAM

56 bits of RAM are contained on-chip. These can be used for any necessary power down storage or as an alarm latch for comparison to the real time counter. The data in the RAM can be compared to the real time counter on a digit basis. The only digits that are not compared are the unit, ten thousandths of seconds and days of the week (these are unused in the real time counter). If the two most significant bits of any RAM digit are ones then this RAM location will always compare.

The RAM is formatted the same as the real time counter, 4 bits per digits, 14 digits, however there are no unused bits. The unused bits in the real time counter will compare only to zeros in the RAM.

Interrupts and Comparator

There are two interrupt outputs. The first and most flexible is the INTERRUPT OUTPUT (a true high signal). This output can be programmed to provide 8 different output signals. They are: 10 Hz, 1 Hz, once per minute, once per hour, once a day, once a week, once a month, and when a RAM/real time counter comparison occurs. To enable the output a one is written into the interrupt control register at the bit location corresponding to the desired output frequency (Figure 1). Once one or more bits have been set in the interrupt control register, the corresponding counter's rollover to reset state will clock the interrupt status register and cause the interrupt output to go high. To reset the interrupt and to identify which frequency caused the interrupt, the interrupt status register is read. Reading this register places the contents of the status register on the data bus. The interrupt frequency will be identified by a one in the respective bit position. Removing the read will reset the interrupt.

The second interrupt is the STANDBY INTERRUPT (open drain output, active low). This interrupt occurs when enabled and when a RAM/ real time counter comparison occurs. The STANDBY INTERRUPT is enabled by writing a one on the D0 line at address 16H or disabled by writing a zero on the D0 line. This interrupt is not triggered by the edge of the compare signal, but rather by the level. Thus if the compare is enabled when the STANDBY INTERRUPT is enabled, the interrupt will turn on immediately.

The comparator is a cascaded exclusive NOR. Its output is latched 61μs after the rising edge of the 1KHz clock signal (input to the ten thousandth of seconds counter). This allows the counter to ripple through before looking at the comparator. For operation at less than 4.0V, the thousandth of seconds counters should not be included in a comparison because of the possibility of having a ripple delay greater than 61μs. (For output timing see interrupt timing.)

Tables 2 and 3 are referred for the address input codes and functions and for the counter and latch reset format.

Power Down Mode

The POWER DOWN input is essentially a second chip select. It disables all inputs and outputs except for the STANDBY INTERRUPT. When this input is at a logical zero, the device will not respond to any external signals. It will, however, maintain time keeping and turn on the STANDBY INTERRUPT if programmed to do so. (The programming must be down before the POWER DOWN input goes to a logical zero.) When switching V_{DD} to the standby or power down mode, the POWER DOWN input should go to a logical zero at least 1 μs before V_{DD} is switched. When switching V_{DD} all other inputs must remain between $V_{SS}-0.3V$ and $V_{DD}+0.3V$. When restoring V_{DD} to the normal operating mode, it is necessary to insure that all other inputs are at valid levels before switching the POWER DOWN input back to a logical one. These precautions are necessary to insure that no data

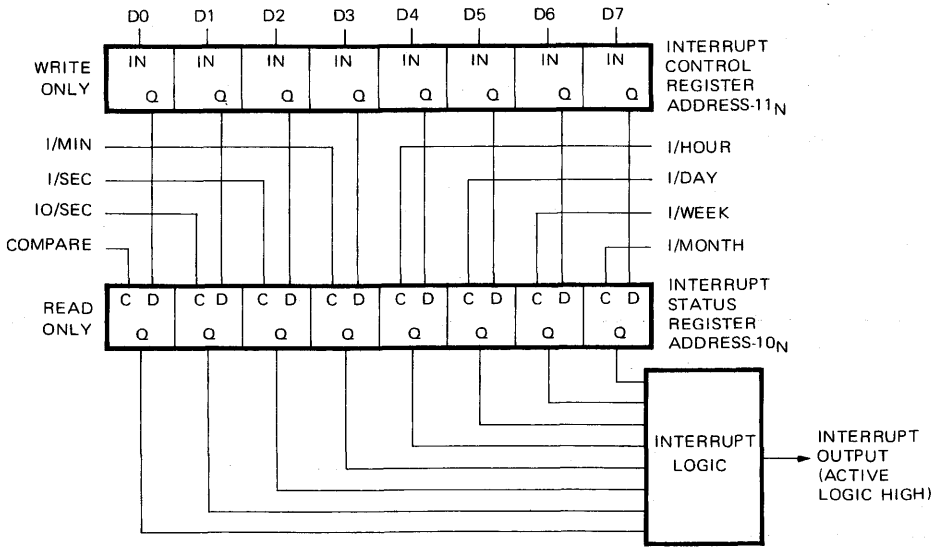


Figure 1. Interrupt Register Format

Table 2. Address Codes and Functions

A4	A3	A2	A1	A0	Function
0	0	0	0	0	Counter – Thousandths of Seconds
0	0	0	0	1	Counter – Hundredths and Tenths of Seconds
0	0	0	1	0	Counter – Seconds
0	0	0	1	1	Counter – Minutes
0	0	1	0	0	Counter – Hours
0	0	1	0	1	Counter – Day of the Week
0	0	1	1	0	Counter – Day of the Month
0	0	1	1	1	Counter – Months
0	1	0	0	0	Latches – Thousandths of Seconds
0	1	0	0	1	Latches – Hundredths and Tenths of Seconds
0	1	0	1	0	Latches – Seconds
0	1	0	1	1	Latches – Minutes
0	1	1	0	0	Latches – Hours
0	1	1	0	1	Latches – Day of the Week
0	1	1	1	0	Latches – Day of the Month
0	1	1	1	1	Latches – Months
1	0	0	0	0	Interrupt Status Register
1	0	0	0	1	Interrupt Control Register
1	0	0	1	0	Counter Reset
1	0	0	1	1	Latch Reset
1	0	1	0	0	Status Bit
1	0	1	0	1	"GO" Command
1	0	1	1	0	Standby Interrupt
1	1	1	1	1	Test Mode

All others unused.

Table 3. Counter and Latch Reset Format

D0	D1	D2	D3	D4	D5	D6	D7	Counter or Latch Reset
1	0	0	0	0	0	0	0	Thousandths of Seconds
0	1	0	0	0	0	0	0	Hundredths and Tenths of Seconds
0	0	1	0	0	0	0	0	Seconds
0	0	0	1	0	0	0	0	Minutes
0	0	0	0	1	0	0	0	Hours
0	0	0	0	0	1	0	0	Day of the Week
0	0	0	0	0	0	1	0	Day of the Month
0	0	0	0	0	0	0	1	Months

For Counter Reset A4–A0 Must be 10010
For Latch Reset A4–A0 Must be 10011

is lost or altered when changing to or from the power down mode.

Counter and RAM Resets; GO Command

The counters and RAM can be reset by writing all 1's (FF) at address 12H or 13H respectively.

A write pulse at address 15H will reset the thousandths, hundredths, tenths, units, and tens of seconds counters. This GO command is used for precise starting of the clock. The data on the data bus is ignored during the writing. If the seconds counter is at a value greater than 39 when the GO is issued, the minute counter will increment; otherwise the minute counter is unaffected. This command is not necessary to start the clock, but merely a convenient way to start precisely at a given minute.

Status Bit

The status bit is provided to inform the user that the clock is in the process of rolling over when a counter is read. The

status bit is set if this 1 KHz clock occurs during or after any counter read. This tells the user that the clock is rippling through the real time counter. Because the clock is rippling, invalid data may be read from the counter. If the status bit is set following a counter read, the counter should be reread.

The status bit appears on D0 when address 14H is read. All the other data lines will be zero. The bit is set when a logical one appears. This bit should be read every time a counter read or after a series of counter reads are done. The trailing edge of the read at address 14H will reset the status bit.

Oscillator

The oscillator is the standard parallel resonant oscillator. Externally, 2 capacitors, a 20M Ohm resistor and the crystal are required. The 20M Ohm resistor is connected between OSC IN and OSC OUT to bias the internal inverter in the linear region. For micropower crystals a resistor in series with the oscillator output may be necessary to insure the crystal is not overdriven. This resistor should be approximately 200K Ohms. The capacitor values should be typically 20 pF – 25 pF. The crystal frequency is 32,768 Hz.

The oscillator input can be externally driven, if desired. In this case the output should be left floating and the input level should be within 0.3V of the supplies.

A ground line or ground plane between pins 9 and 10 may be necessary to prevent interference of the oscillator by the A4 address.

Control Lines

The READ, WRITE, CHIP SELECT signals are active low inputs. The READY signal is an open drain output. At the start of each read or write cycle the READY line (open drain) will pull low and remain low until valid data from a chip read appears on the bus or data on the bus is latched in during a writing. READ and WRITE must be accompanied by a CHIP SELECT (see Timing waveforms for read and write cycle).

During a read or write, address bits must not change while chip select and control strobes are low.

Test Mode

The test mode is merely a mode for production testing. It allows the counters to count at a higher than normal rate. In this mode the 32 KHz oscillator input is connected directly to the ten thousandths of seconds counter. The chip select and write lines must be low and the address must be held at 1 FH.

Typical Application

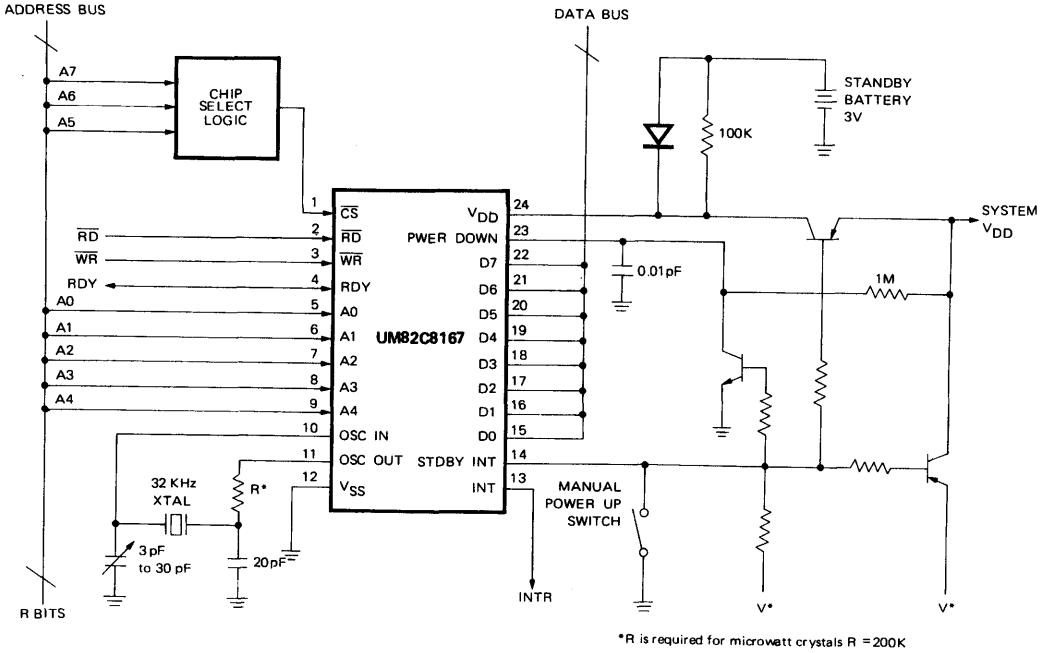


Figure 2. Standby Interrupt is Enable (ON) for Normal Operation and Disabled for Standby Operation

UM82C852

Multi I/O For XT

Features

- Supports game port
- Supports 2nd serial port
- Centronics printer interface
- Independent control of transmit, receive, line status and data set interrupts
- Individual modem control signals
- Programmable serial interface characteristics:
  - 5, 6, 7, or 8 bit characters
  - Even, odd or no-parity bit generation and detection
  - 1, 1½, or 2 stop bit generation
- Milliseconds through month counters for real time clock
- 56 bits of RAM with comparator for comparing the real time counter to the RAM data
- POWER DOWN input that disables all inputs and outputs
- Disables the chip from the reset of the system for standby low power operation by use of a POWER DOWN input
- 32,768 Hz crystal for real time clock
- Four-year calendar (no leap year)
- 24-hour clock

General Description

The Multi-I/O chip, UM82C852 is an integrated chip of UM82C450, UM82C11, UM82C8167. This chip is a Multi-I/O for PC/XT and PS2 model 30.

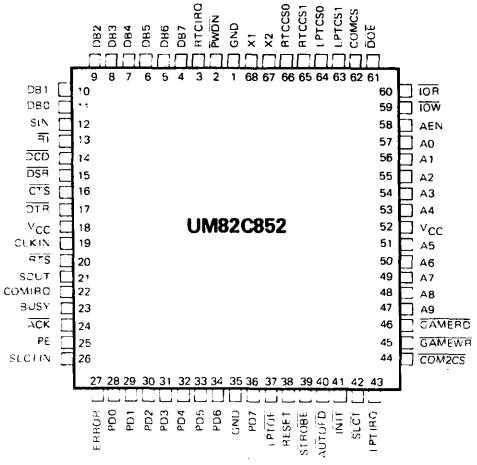
The 82C450 asynchronous communications element (ACE) performs serial-to-parallel conversion on data characters received from peripheral devices or modems, and parallel-to-serial conversion of data characters transmitted by the CPU. The complete status of the ACE can be read at any time during functional operation by CPU. The information obtained includes the type and condition of the transfer operations being performed and error conditions.

The 82C11 parallel port provides the user with a bidirectional parallel data port that fully supports the parallel Centronics type printer.

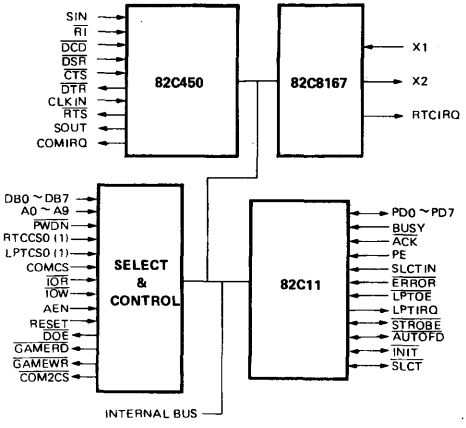
The 82C8167 real time clock includes an addressable real time counter, 56 bits of static RAM with an on chip oscillation circuit which can generate the 32,768 Hz time base.

The 82C852 is packaged in a 68-pin plastic leaded chip carrier.

Pin Configuration



Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description
2	$\overline{PWDN}$	I	POWER DOWN – This input disables all inputs and outputs.
3	RTCIRQ	O	RTC INTERRUPT REQUEST – This is a RTC interrupt request when a RAM/real time counter comparison occurs.
4 ~ 11	DB 0 ~ DB7	I/O	DATA BUS – This data bus provides I/O lines for the transfer of data between CPU and the chip.
12	SIN	I	SERIAL INPUT – This line is used to receive serial data from the communication line.
13	$\overline{RI}$	I	RING INDICATOR – When low, indicates that a telephone ringing signal has been received by the MODEM or data set.
14	$\overline{DCD}$	I	DATA CARRIER DETECT – When low, indicates that the data carrier has been detected by the MODEM or data set.
15	$\overline{DSR}$	I	DATA SET READY – When low, indicates that the MODEM or data set is ready to establish the communication.
16	$\overline{CTS}$	I	CLEAR TO SEND – When low, indicates that the MODEM or data set is ready to receive data.
17	$\overline{DTR}$	O	DATA TERMINAL READY – When low, informs the MODEM or data set that the ACE is ready to communicate.
19	CLKIN	I	CLOCK INPUT – The external clock for 82C450.
20	$\overline{RTS}$	O	REQUEST TO SEND – When low, informs the MODEM or data set that the ACE is ready to transmit data.
21	SOUT	O	SERIAL OUTPUT – Composite serial data output to the communications link.
22	COMIRQ	O	COM INTERRUPT REQUEST – ACE interrupt request.
23	BUSY	I	BUSY STATE – When high, printer can't receive data.
24	$\overline{ACK}$	I	ACKNOWLEDGE – When low, indicates that the data has been received and the printer is ready to accept other data.
25	PE	I	PAPER END – When high, indicates that the printer is out of paper.
26	SLCTIN	I	SELECT IN – This is always high unless the printer is down.
27	$\overline{ERROR}$	I	ERROR – When low, the printer has encountered an error condition.
28 ~ 34, 36	PD0 ~ PD7	I/O	PARALLEL DATA BUS – This bus provides a byte-wide bi-direction data port to the system.
37	$\overline{LPTOE}$	I	LINE PRINTER OUTPUT ENABLE – When low, the printer data output (PD0 ~ PD7) enables.
38	RESET	I	When high, forces the 82C450 and 82C11 to an idle state.
39	$\overline{STROBE}$	I/O	DATA STROBE – When low, the printer reads in the data on printer data bus PD0 ~ PD7, open collector output.
40	$\overline{AUTOFD}$	I/O	AUTO FEED – When low, the printer adds line-feed after a line is printed, open collector output.
41	$\overline{INIT}$	I/O	INITIAL – When low, the printer buffer is cleared, open collector output.

Pin Description (Continued)

Pin No.	Symbol	I/O	Description
42	$\overline{SLCT}$	I/O	PRINTER SELECT – When low, the printer is selected, open collector output.
43	LPTIRQ	O	PRINTER INTERRUPT REQUEST – Printer interrupt request.
44	$\overline{COM2CS}$	O	COM2 CHIP SELECT – When low, COM2 is selected.
45	$\overline{GAMERD}$	O	GAME READ – When low, game port read enables.
46	$\overline{GAMEWR}$	O	GAME WRITE – When low, game port write enables.
47 ~ 51 53 ~ 57	A0 ~ A9	I	ADDRESS BUS – These address lines are used to select chip and internal register during CPU cycle.
58	AEN	I	DMA ADDRESS ENABLE – When high, DMA cycle. When low, CPU cycle.
59	$\overline{IOW}$	I	I/O WRITE – When low, CPU write data to data bus.
60	$\overline{IOR}$	I	I/O READ – When low, CPU read data from data bus.
61	$\overline{DOE}$	O	DATA OUTPUT ENABLE – When low, CPU read/write data to this chip.
62	COMCS	I	COM SELECT – COM address select.
63 ~ 64	LPTCS0 ~ LPTCS1	I	PRINTER SELECT – Printer address select.
65 ~ 66	RTCCS0 ~ RTCCS1	I	RTC SELECT – RTC address select.
67 ~ 68	X1, X2	I	32.768 KHz real time clock crystal input.
18, 52	V_{CC}	I	Power supply.
1, 35	GND	I	Ground.

Function Description:

(a) I/O Port Address:

(i) Parallel port:

LPTCS1	LPTCS0	Address	Comment
0	0	3BC ~ 3BE	LPT1
0	1	378 ~ 37A	LPT2
1	0	278 ~ 27A	LPT3
1	1	–	Disable

(ii) Asynchronous communication port:

COMCS	COM1 Address	COM2 Address
0	3F8 ~ 3FF	2F8 ~ 2FF
1	2F8 ~ 2FF	3F8 ~ 3FF

(iii) Real time clock:

RTCCS1	RTCCS0	Address	Comment
0	0	240 ~ 25F	RTC1
0	1	340 ~ 35F	RTC2
1	0	0E0 ~ 0EF 0B0 ~ 0BF	RTC3
1	1	–	Disable

(iv) Game port:

Address
201

(b) Serial Channel Registers

Three types of internal registers are used in the serial channel of the UM82C852. They are used in the operation of the device and are the control status and data registers. The control registers are the Bit Rate Select Register DLL (Divisor Latch LSB) and DLM (Divisor Latch MSB). Line Control Register Interrupt Enable Register and the Modem Control registers while the status registers are the Line Status Registers and the Modem Status Register. The data registers are the Receiver Buffer Register and the Transmitter Holding Register. The Address Read and Write inputs are used in conjunction with the Divisor Latch Access Bit in the Line Control Register [LCR (7)] to select the register to be written or read (see Table 1). Individual bits within these registers are referred to by the register mnemonic and the bit number in parenthesis. An example LCR (7) refers to Line Control Register Bit 7.

The Transmitter Buffer Register and Receiver Buffer Register are data registers holding from five to eight bits of data. If less than eight data bits are transmitted data is right justified to the LSB. Bit 0 of a data word is always the first serial data bit received and transmitted. The UM82C852 data registers are double-buffered so that read and write operations can be performed at the same time the UART is performing the parallel-to-serial and serial-to-parallel conversion.

The format of the data character is controlled by the Line Control Register. The contents of the LCR may be read, eliminating the need for separate storage of the line characteristics in system memory. The contents of the LCR are described as follows:

LCR (0) Word Length Select Bit 0 (WLS0)
LCR (1) Word Length Select Bit 1 (WLS1)
LCR (2) Stop Bit Select (STB)
LCR (3) Parity Enable (PEN)
LCR (4) Even Parity Select (EPS)
LCR (5) Stick Parity
LCR (6) Set Break
LCR (7) Divisor Latch Access Bit (DLAB)

LCR (0) and LCR (1) word length select bit 1: The number of bits in each serial character is programmed as shown in the following chart:

LCR (1)	LCR (0)	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

LCR (2) Stop Bit Select: LCR (2) specifies the number of stop bits in each transmitted character. If LCR (2) is a logic 0, one stop bit is generated in the transmitted data. If LCR (2) is a logic 1 when a 5-bit word length is selected, 1.5 stop bits are generated. If LCR (2) is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two stop bits are generated. The receiver checks for two stop bits if programmed.

LCR (3) Parity Enable: When LCR (3) is high, a parity bit between the last data word bit and stop bit is generated and checked.

Table 1. Serial Channel Internal Registers

DLAB	A2	A1	A0	Mnemonic	Register
0	0	0	0	RBR	Receiver Buffer Register (read only)
0	0	0	0	THR	Transmitter Holding Register (write only)
0	0	0	1	IER	Interrupt Enable Register
X	0	1	0	IIR	Interrupt Identification Register (read only)
X	0	1	1	LCR	Line Control Register
X	1	0	0	MCR	Modem Control Register
X	1	0	1	LSR	Line Status Register
X	1	1	0	MSR	Modem Status Register
X	1	1	1	SCR	Scratch Register
1	0	0	0	DLL	Divisor Latch (LSB)
1	0	0	1	DLM	Divisor Latch (MSB)

X = "Don't Care" 0 = Logic Low 1 = Logic High

LCR (4) Even Parity Select: When parity is enabled (LCR (3) = 1). LCR (4)-0 selects odd parity, and LCR (4) = 1 selects even parity.

LCR (5) Stick Parity: When parity is enabled (LCR (3) = 1), LCR (5) = 1 causes the transmission and reception of a parity bit to be in the opposite state from that indicated by LCR (4). This allows the user to force parity to a known state and for the receiver to check the parity bit in a known state.

LCR (6) Break Control: When LCR (6) is set to a logic "1", the serial output (SOUT) is forced to the spacing (logic 0) state. The break is disabled by setting LCR (6) to a logic "0". The Break Control bit acts only on SOUT and has no effect on the transmitter logic. Break Control enables the CPU to alert a terminal in a computer communications system. If the following sequence is used, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all "0" pad character in response to THRE.
2. Set break in response to the next THRE.
3. Wait for the transmitter to be idle (TEMT = 1, and clear break when normal transmission has to be restored.

LCR (7) Divisor Latch Access Bit (DLAB): LCR (7) must be set high (logic "1") to access the Divisor Latches DLL and DLM of the Baud Rate Generator during a read or write operation. LCR (7) must be input low to access the Receiver Buffer the Transmitter Holding or the Interrupt Enable Registers.

The Line Status Register (LSR) is a single register that provides status indications. The LSR is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of the serial channel of the UM82C852.

Three error flags OE, FE, and PE provide the status of any error conditions detected in the receiver circuitry. During reception of the stop bits the error flags are set high by an error condition. The error flags are not reset by the absence of an error condition in the next received character. The flags reflect the last character only if no overrun occurs. The Overrun Error character in the Receiver Buffer Register has been over-written by a character from the Receiver Shift Register before being read by the CPU. The character is thereby lost. Framing Error (FE) indicates that the last character received contained incorrect (low) stop bits. This is caused by the absense

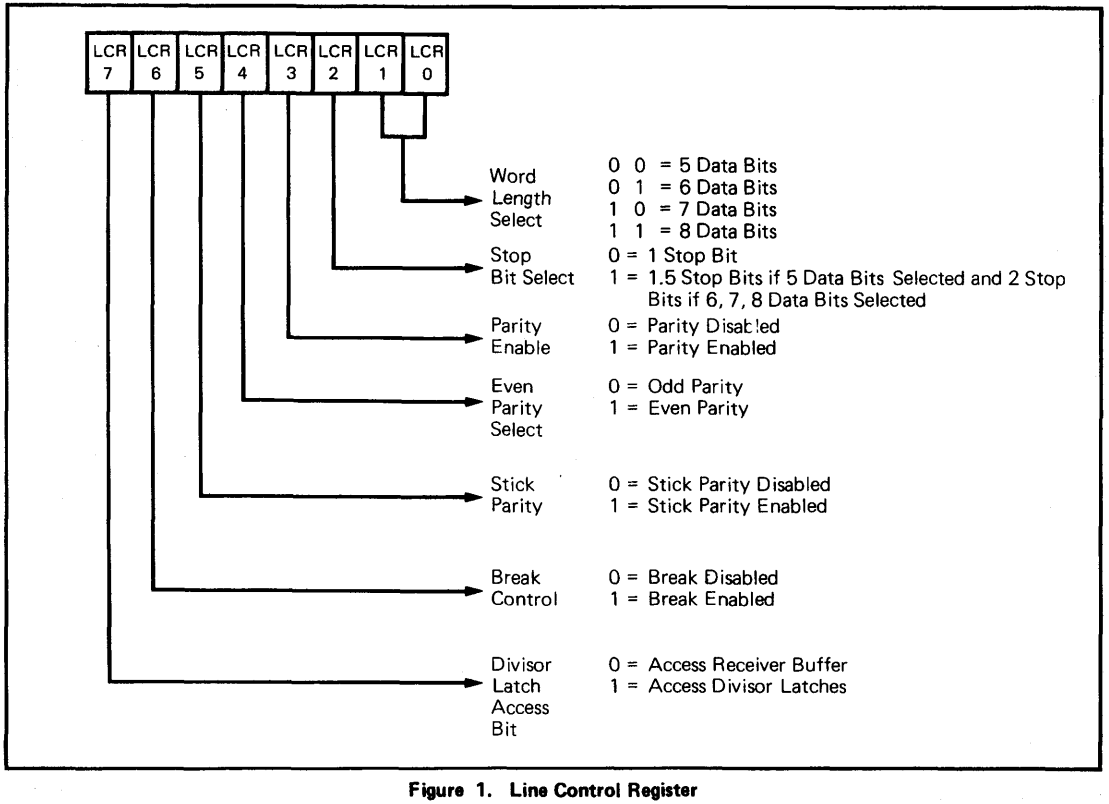


Figure 1. Line Control Register

of the required stop bit or by a stop bit too short to be detected. Parity Error (PE) indicates that the last character received had a parity error based on the programmed and calculated parity of the received character.

The Break Interrupt (BI) status bit indicates that the last character received was a break character. A break character is an invalid data character. However, it is an entire character including parity and stop bits.

The Transmitter Holding Register Empty (THRE) bit indicates that the THR register is empty and may receive another character. The Transmission Shift Register Empty (TEMT) bit indicates that the Transmitter Shift Register is empty and the serial channel has completed transmission of the last character to be sent. If the interrupt is enabled [IER (1)] an active THRE causes an interrupt (INTRPT).

The Data Ready (DR) bit indicates that the RBR has been loaded with a received character (including Break) and that the CPU may access this data.

Reading the LSR clears LSR (1)-LSR (4). (OE, PE, FE, and BI).

The contents of the Line Status Register shown in Table 2 are described below:

LSR (0) Data Ready (DR): Data Ready is set high when an incoming character has been received and transferred into the Receiver Buffer Register. LSR (0) is reset low by a CPU read of the data in the Receiver Buffer Register.

LSR (1) Overrun Error (OE): Overrun Error indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register overwriting the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

LSR (2) Parity Error (PE): Parity Error indicates that the received data character does not have the correct even or odd parity, as selected by the Even Parity Select bit [LCR (4)]. The PE bit is set high upon detection of a parity error, and is reset low when the CPU reads the contents of the LSR.

LSR (3) Framing Error (FE): Framing Error indicates that the received character did not have a valid stop bit. LSR (3) is set high when the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is reset low when the CPU reads the contents of the LSR.

LSR (4) Break Interrupt (BI): Break Interrupt is set high when the received data input is held in the spacing (logic 0) state for longer than a full word transmission time (start bit + data bits + parity ÷ stop bits). The BI indicator is reset when the CPU reads the contents of the Line Status Register.

LSR (1)-LSR (4) are the error conditions that produce a Receiver Line Status interrupt (priority 1 interrupt in the Interrupt Identification Register (IIR)) when any of the conditions are detected. This interrupt is enabled by setting IER(2) = 1 in the Interrupt Enable Register.

LSR (5) Transmitter Holding Register Empty (THRE) THRE: indicates that the UM82C852 is ready to accept a new character for transmission. The THRE bit is set high when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register LSR (5) is reset low by the loading of the Transmitter Holding Register by the CPU. LSR (5) is not reset by a CPU read of the LSR.

When the THRE interrupt is enabled (IER (1) = 1). THRE causes a priority 3 interrupt in the IIR. If THRE is the interrupt source indicated in IIR, INTRPT is cleared by a read of the IIR.

LSR (6) Transmitter Empty (TEMT): TEMT is set high when the Transmitter Holding Register (THR) and the

Table 2. Line Status Register Bits

LSR Bits		Logic 1	Logic 0
LSR (0)	Data Ready (DR)	Ready	Not Ready
LSR (1)	Overrun Error (OE)	Error	No Error
LSR (2)	Parity Error (PE)	Error	No Error
LSR (3)	Framing Error (FE)	Error	No Error
LSR (4)	Break Interrupt (BI)	Break	No Break
LSR (5)	Transmitter Holding Register Empty (THRE)	Empty	Not Empty
LSR (6)	Transmitter Empty (TEMT)	Empty	Not Empty
LSR (7)	Not Used		

Transmitter Shift Register (TSR) are both empty. LSR (6) is reset low when a character is loaded into the THR and remains low until the character is transferred out of SOUT. TEMT is not reset low by a CPU read of the LSR.

LSR (7): This bit is always 0.

The Modem Control Register (MCR) controls the interface with the modem or data set as described in Table 3. MCR can be written and read. The $\overline{RTS}$ and $\overline{DTR}$ outputs are directly controlled by their control bits in this register. A high input asserts a low (true) at the output pins. MCR Bits 0, 1, 3, and 4 are shown below:

MCR (0): When MCR (0) is set high the $\overline{DTR}$ output is forced low. When MCR (0) is reset low, the $\overline{DTR}$ output is forced high. The $\overline{DTR}$ output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

MCR (1): When MCR (1) is set high, the RTS output is forced low. When MCR (1) is reset low, the RTS output is forced high. The $\overline{RTS}$ output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

MCR (3): When MCR (3) is set high, the INT output is enabled.

MCR (4): MCR (4) provides a local loopback feature for diagnostic testing of the channel. When MCR (4) is set high, Serial Output (SOUT) is set to the marking (logic "1") state, and the receiver data input Serial Input (SIN) is disconnected. The output of the Transmitter Shift Register is looped back into the Receiver Shift Register input. The three modem control inputs ($\overline{CTS}$, $\overline{DSR}$, and $\overline{RI}$) are disconnected. The modem control outputs ($\overline{DTR}$ and $\overline{RTS}$) are internally connected to the four modem control inputs. The modem control output pins are forced to their inactive state (high).

In the diagnostic mode, data transmitted is immediately received. This allows the processor to verify the transmit and receive data paths of the selected serial channel. Bits MCR (5)-MCR (7) are permanently set to logic 0.

The MSR provides the CPU with status of the modem input lines from the modem or peripheral devices. The MSR allows the CPU to read the serial channel modem signal inputs by accessing the data bus interface of the UM82C852. In addition to the current status information, four bits of the MSR indicate whether the modem inputs have changed since the last reading of the MSR. The delta status bits are set high when a control input from the modem changes state, and reset low when the CPU reads the MSR.

The modem input lines for each channel are $\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$ and $\overline{DCD}$, MSR (4) - MSR (7) are status indications of these lines. The status indications follow the status of the input lines. If the modem status interrupt in the Interrupt Enable Register is enabled [IER (3)], a change of state in a modem input signal will be reflected by the modem status bits in the IIR register, and an interrupt (INTRPT) is generated. The MSR is a priority 4 interrupt. The contents of the Modem Status Register are described in Table 4. Note that the State (high or low) of the status bits are inverted versions of the actual input pins.

MSR (0) Delta Clear to Send (DCTS): DCTS indicates that the $\overline{CTS}$ input to the serial channel has changed state since the last time it was read by the CPU.

Table 3. Modem Control Register Bits

MCR Bits		Logic 1	Logic 0
MCR (0)	Data Terminal Ready (DTR)	$\overline{DTR}$ Output Low	$\overline{DTR}$ Output High
MCR (1)	Request to Send (RTS)	$\overline{RTS}$ Output Low	$\overline{RTS}$ Output High
MCR (2)	0		
MCR (3)	Interrupt (INT) Enable	INT Enabled	INT Disabled
MCR (4)	Loop	Loop Enabled	Loop Disabled
MCR (5)	0		
MCR (6)	0		
MCR (7)	0		

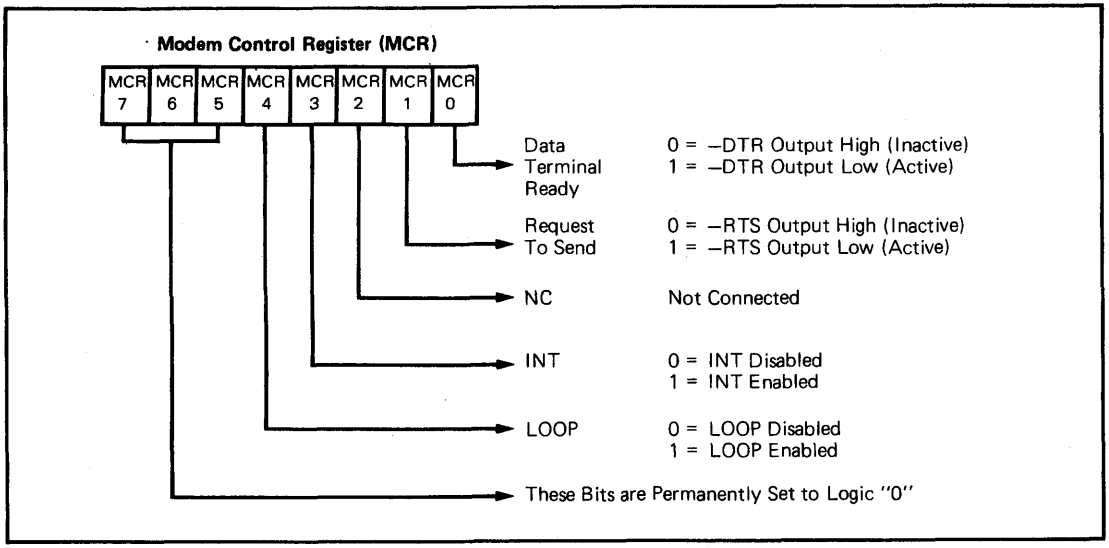


Figure 2. Modem Control Register

Table 4. Modem Status Register Bits

MSR Bit	Mnemonic	Description
MSR (1)	DDSR	Delta Data Set Ready
MSR (2)	TERI	Trailing Edge of Ring Indicator
MSR (0)	DCTS	Delta Clear to Send
MSR (3)	DDCD	Delta Data Carrier Detect
MSR (4)	$\overline{CTS}$	Clear To Send
MSR (5)	$\overline{DSR}$	Data Set Ready
MSR (6)	$\overline{RI}$	Ring Indicator
MSR (7)	$\overline{DCD}$	Data Carrier Detect

MSR (1) Delta Data Set Ready (DDSR): DDSR indicates that the $\overline{DSR}$ input to the serial channel has changed state since the last time it was read by the CPU.

MSR (2) Trailing Edge of Ring Indicator (TERI): TERI indicates that the $\overline{RI}$ input to the serial channel has changed state from high to low since the last time it was read by the CPU. Low to high transitions on $\overline{RI}$ do not activate TERI.

MSR (3) Delta Data Carrier Detect (DDCD): DDCD indicates that the $\overline{DCD}$ input to the serial channel has changed state since the last time it was read by the CPU.

MSR (4) Clear to Send (CTS): Clear to Send (CTS) is the status of the $\overline{CTS}$ input from the modem indicating to the serial channel that the modem is ready to receive data from the serial channel's transmitter, output (SOUT). If the serial channel is in loop mode [MSR (4) = 1]. MSR (4) is equivalent to $\overline{RTS}$ in the MCR.

MSR (5) Data Set Ready (DSR): Data Set Ready (DSR) is a status of the $\overline{DSR}$ input from the modem to the serial channel which indicates that the modem is ready to provide received data to the serial channel receiver circuitry. If the channel is in the loop mode [MCR (4) = 1], MSR (5) is equivalent to DTR in the MCR.

MSR (6) Ring Indicator: Indicates the status to the RI input (pin 39). If the channel is in the loop mode [MCR (4) = 1], MSR (6) is not connected in the MCR.

MSR (7) Data Carrier Detect: Data Carrier Detect indicates the status of the Data Carrier Detect ($\overline{DCD}$) input. If the channel is in the loop mode [MCR (4) = 1], MSR (4) is equivalent to OUT2 of the MCR.

The modem status inputs (RI, $\overline{DCD}$, $\overline{DSR}$, and $\overline{CTS}$) reflect the modem input lines with any change of status. Reading the MSR register will clear the delta modem status indications but has no effect on the status bits. The status bits reflect the state of the input pins regardless of the mask control signals. If a DCTS, DDSR, TERI, or DDCD are true, and a state change occurs during a read operation ($\overline{IOR}$), the state change is not indicated in the MSR. If DCTS, DDSR, TERI, or DDCD are false, and a state change occurs during a read operation, the state change is indicated after the read operation.

For LSR and MSR, the setting of status bits ($\overline{IOR}$) is inhibited during status register read operations. If a status condition is generated during a read operation. ($\overline{IOR}$), the status bit is not set until the trailing edge of the read ($\overline{IOR}$).

If a status bit is set during a read $\overline{IOR}$ operation, and the same status condition occurs, that status bit will be cleared at the trailing edge of the read $\overline{IOR}$ instead of being set again.

The UM82C852 serial channel contains a programmable Baud Rate Generator (BRG) that divides the clock (DC to 3.1 MHz) by any divisor from 1 to $2^{16}-1$ (see also BRG description). The output frequency of the Baud Generator is 16X the data rate [divisor # = clock + (baud rate x 16)]. Two 8-bit divisor latch registers store the divisor in a 16-bit binary format. These Divisor Latch registers must be loaded during initialization. Upon loading either of the Divisor latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load.

The receiver circuitry in each serial channel of the UM82C852 is programmable for 5, 6, 7, or 8 data bits per character. For words of less than 8 bits, the data is right justified to the least significant bit LSB = Data Bit 0 [RBR (0)]. Data Bit 0 of a data word [RBR (0)] is the first data bit received. The unused bits in a character less than 8 bits are output low to the parallel output by the serial channel.

Received data at the SIN input pin is shifted into the Receiver Shift Register by the 16X clock provided at the CLKIN input. This clock is synchronized to the incomplete data based on the position of the start bit. When a complete character is shifted into the Receiver Shift Register, the assembled data bits are parallel loaded into the Receiver Buffer Register. The DR flag in the LSR register is set.

Double buffering of the received data permits continuous reception of data without losing received data. While the Receiver Shift Register is shifting a new character into the serial channel, the Receiver Buffer Register is holding a previously received character for the CPU to read. Failure to read the data in the RBR before complete reception of the next character results in the loss of the data in the Receiver Register. The OE flag in the LSR register indicates the overrun condition.

RBR Bits 0 thru 7:

RBR (0)	Data Bit 0
RBR (1)	Data Bit 1
RBR (2)	Data Bit 2
RBR (3)	Data Bit 3
RBR (4)	Data Bit 4
RBR (5)	Data Bit 5
RBR (6)	Data Bit 6
RBR (7)	Data Bit 7

The Transmitter Holding Register (THR) holds parallel data from the data bus (D0-D7) until the Transmitter Shift Register is empty and ready to accept a new character for transmission. The transmitter and receiver word length and number of stop bits are the same. If the character is less than eight bits, unused bits at the microprocessor data bus are ignored by the transmitter.

Data Bit 0 [THR (0)] is the first serial data bit transmitted. The THRE flag [LSR (5)] reflects the status of the THR. The TEMT flag [LSR (5)] indicates if both the THR and TSR are empty.

THR Bits 0 thru 7

THR (0)	Data Bit 0
THR (1)	Data Bit 1
THR (2)	Data Bit 2
THR (3)	Data Bit 3
THR (4)	Data Bit 4
THR (5)	Data Bit 5
THR (6)	Data Bit 6
THR (7)	Data Bit 7

The Scratchpad Register is an 8-bit Read/Write register that has no effect on either channel in the UM82C852 It is intended to be used by the programmer to hold data temporarily.

SCR Bits 0 thru 7

SCR (0)	Data Bit 0
SCR (1)	Data Bit 1
SCR (2)	Data Bit 2
SCR (3)	Data Bit 3
SCR (4)	Data Bit 4
SCR (5)	Data Bit 5
SCR (6)	Data Bit 6
SCR (7)	Data Bit 7

Interrupts

The Interrupt Identification Register (IIR) in the serial channel of the UM82C852 has interrupt capability for interfacing to current microprocessors. In order to minimize software overhead during data character transfers, the serial channel prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows:

1. Receiver Line Status (priority 1)
2. Received Data Ready (priority 2)
3. Transmitter Holding Register Empty (priority 3)
4. Modem Status (priority 4)

Information indicating that a prioritized interrupt is pending and the type of interrupt is stored in the interrupt Identification Register (IIR). When addressed during

chip select time, the IIR indicates the highest priority interrupt pending. No other interrupts are acknowledged until the interrupt is serviced by the CPU. The logic equivalent of the interrupt control circuit is shown in Figure 3. The contents of the IIR are indicated in Table 5 and are described below.

IIR (0): IIR (0) can be used in either a hard-wired prioritized or polled environment to indicate whether an interrupt is pending. When IIR (0) is low, an interrupt is pending, and IIR contents may be used as a pointer to the appropriate interrupt service routine. When IIR (0) is high, no interrupt is pending.

IIR (1) and IIR (2) are used to identify the highest priority interrupt pending as indicated in Table 5.

IIR (3)-IIR (7): These five bits of the IIR are logic 0.

The Interrupt Enable Register (IER) is a Write register used to independently enable the four serial channel interupts which activate the interrupt (INTRPT) output. All interrupts are disabled by resetting IER (0)-IER (3) of the Interrupt Enable Register. Interrupts are enabled by setting the appropriate bits of the IER high. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers. The content of the Interrupt Enable Register is described in Table 6 and below.

IER (0): When programmed high [IER (0) = Logic 1], IER (0) enables Received Data Available Interrupt.

IER (1): When programmed high [IER (1) = Logic 1], IER (1) enables the Transmitter Holding Register Empty interrupt.

IER (2): When programmed high [IER (2) = Logic 1], IER (2) enables the Receiver Line Status interrupt.

IER (3): When programmed high [IER (3) = Logic 1], IER (3) enables the Modem Status Interrupt.

IER (4)-IER (7): These four bits of the IER are logic 0.

Transmitter

The serial transmitter section consists of a Transmitter Holding Register (THR), Transmitter Shift Register (TSR), and associated control logic. The Transmitter Holding Register Empty (THRE) and Transmitter Shift Register Empty (TEMT) are two bits in the Line Status Register which indicate the status of THR and TSR. To transmit a 5 to 8-bit word, the word is written through DB0-DB7 to the THR. The microprocessor should perform a write operation only if THRE is high. The THRE is set high when the word is automatically transferred from the THR to the TSR during the transmission of the start bit.

When the transmitter is idle, THRE and TEMT are high. The last word written causes THRE to be reset to 0. After the transfer, THRE returns high. TEMT remains low for at least the duration of the transmission of the data word. If a second character is transmitted to the THR, the THRE is reset low. Since the data word cannot be transferred from the THR to the TSR until the TSR is empty, THRE remains low until the TSR has completed sending the word. When the last word has been transmitted out of the TSR, TEMT is set high. THRE is set high one THR to TSE transfer time later.

Receiver

Serial asynchronous data is input into the SIN pin. The idle state of the line providing the input into SIN is high. A start bit detect circuit continually searches for a high to low transition from the idle state. When the transition is detected, a counter is reset, and counts the 16X clock to 71/2, which is the center of the start bit. The start bit is valid if the SIN is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the SIN input.

The Line Control Register determines the number of data bits in a character (LCR (0), LCR (1)), number of stop bits LCR (2), if parity is used LCR (3), and the polarity of parity LCR (4). If Status for the receiver is provided in the Line Status Register to the Receiver Buffer Register when the Data Received indication in LSR (0) is set high, the CPU reads the Receiver Buffer Register through D0-D7. This read resets LSR (0). If D0-D7 are not read prior to a new character transfer from the RSR to the RBR, the overrun error status indication is set in LSR (1). The parity check tests for even or odd parity on the parity bit, which precedes the first stop bit. If there is a parity error, the parity error is set in LSR (2). There is circuitry which tests whether the stop bit is high. If it is not, a framing error indication is generated in LSR (3).

The center of the start bit is defined as clock count 7 1/2. If the data into SIN is a symmetrical square wave, the center of the data cells will occur within ±3.125% of the actual center, providing an error margin of 46.875%. The start bit can begin as much as one 16X clock cycle prior to being detected.

Baud Rate Generator (BRG)

The BRG generates the clocking for the UART function,

providing standard ANSI/CCITT bit rates. The clock driving the BRG is provided by the CLKIN input.

The data rate is determined by the Divisor Latch registers DLL and DLM and the external frequency. The bit rate is selected by programming the two divisor latches, Divisor Latch Most Significant Byte and Divisor Latch Least Significant Byte. Setting DLL = 1 and DLM = 0 selects the divisor to divide by 1 (divide by 1 gives the maximum baud rate for a given input frequency at the CLKIN input.

The BRG can use any of three different popular frequencies to provide standard baud rates. These frequencies are 1.8432 MHz, 2.4576 MHz, and 3.072 MHz. With these frequencies, standard bit rates from 50 to 38.5 kbps are available. Tables 7, 8, and 9 illustrate the divisors needed to obtain standard rates using these three crystal frequencies.

Reset

After power up, the UM82C852 RESET input should be held high for 500 ns to reset the UM82C852 circuits to an idle mode until initialization. A high on RESET causes the following:

1. Initializes the transmitter and receiver internal clock counters.
2. Clears the Line Status Register (LSR), except for Transmitter Shift Register Empty (TEMT) and Transmit Holding Register Empty (THRE), which are set. The Modem Control Register (MCR) is also cleared. All of the discrete lines, memory elements and miscellaneous logic associated with these register bits are also cleared or turned off. The Line Control Register (LCR), Divisor Latches, Receiver Buffer Register, Transmitter Buffer Register are not affected.

Following removal of the reset condition (Reset high), the UM82C852 remains in the idle mode until programmed.

A hardware reset of the UM82C852 sets the THRE and TEMT status bit in the LSR. When interrupts are subsequently enabled, an interrupt occurs due to THRE.

A summary of the effect of a reset on the UM82C852 is given in Table 10.

Programming

Each serial channel of the UM82C852 is programmed by the control registers LCR, IER, DLL and DLM, and MCR. These control words define the character length, number of stop bits, parity, baud rate, and modem interface. While the control register can be written in any order, the IER should be written to last because it controls the interrupt enables. Once a serial channel is programmed and operational, these registers can be updated any time the UM82C852 serial channel is not transmitting or receiving data.

The control signals required to access each serial channel's internal registers are shown below.

Software Reset

A software reset of the serial channel is a useful method for returning to a completely known state without a system reset. Such a reset consists of writing to the LCR, Divisor Latches, and MCR registers. The LSR and RBR registers should be read prior to enabling interrupts in order to clear out any residual data or status bits which may be invalid for subsequent operation.

Clock Input Operation

The maximum input frequency of the external clock of the UM82C852 is 3.1 MHz.

(c) Parallel Port Registers

The UM82C852's parallel port interfaces the device to a Centronics-style printer. When parallel port address selected ($\overline{IOR}$) and write ($\overline{IOW}$) pin are as shown, the Read Data Register allows the microprocessor to read the information on the parallel bus. The Read Status Register allows the microprocessor to read the status of the printer in the five most significant bits. The status bits are Printer Busy (BUSY). Acknowledge (ACK) which is a handshake function. Paper Empty (PE), Printer Selected (SLCT), and Error. (ERROR). The Read Control Register allows the state of the control lines to be read. The Write Control Register sets the state of the control lines.

They are LPTIRQ Enable (IRQ ENB). Select In (SLIN). Initialize the Printer (INIT). Autofeed the Paper (AUTOFD). Strobe (STROBE), which informs the printer of the presence of a valid byte on the parallel bus. The Write Data Register allows the microprocessor to write a byte to the parallel bus.

The parallel port is completely compatible with the parallel port implementation used in the IBM Serial/Parallel Adaptor.

Table 5. Interrupt Identification Register

Interrupt Identification				Interrupt Set and Reset Functions		
Bit 2	**Bit 1**	**Bit 0**	**Priority Level**	**Interrupt Flag**	**Interrupt Source**	**Interrupt Reset Control**
X	X	1		None	None	
1	1	0	First	Receiver Line Status	OE, PE FE, or BI	LSR Read
1	0	0	Second	Received Data Available	Received Data Available	RBR Read
0	1	0	Third	THRE	THRE	IIR Read if THRE is the Interrupt Source or THR Write
0	0	0	Fourth	Modem Status	–CTS, –DSR –RI, –DCD)	MSR Read

X = Not Defined.

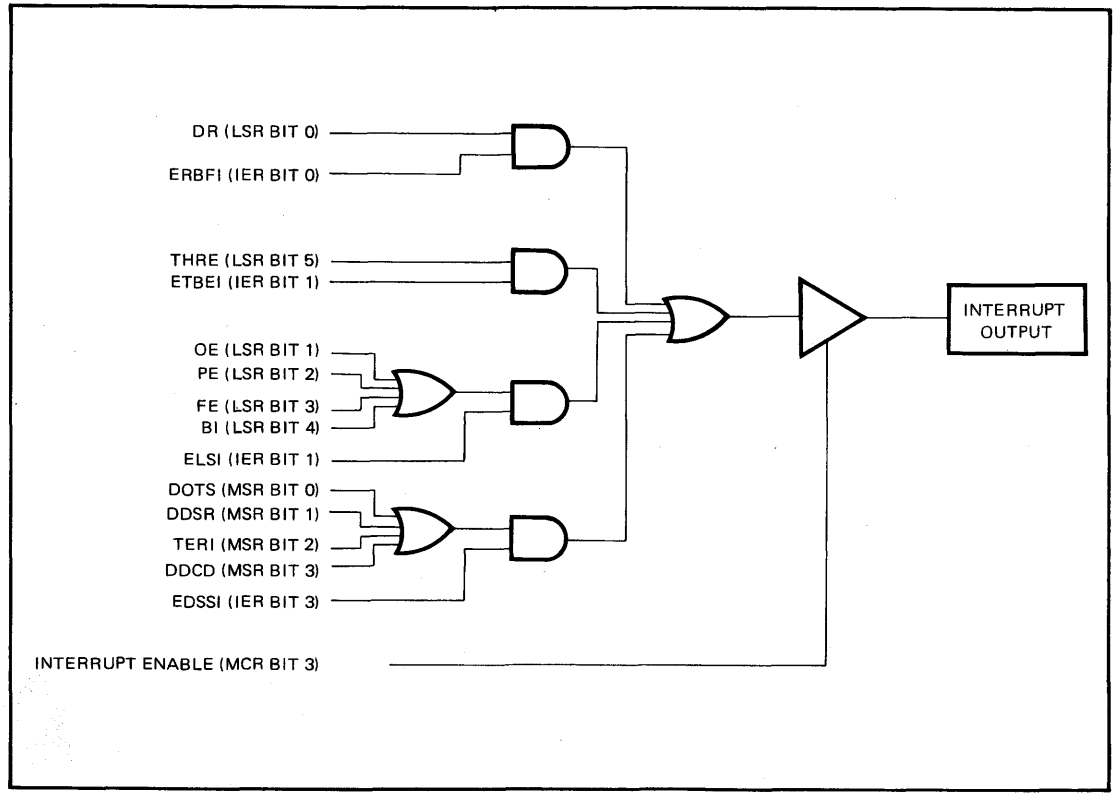


Figure 3. Interrupt Control Logic

Table 6. Serial Channel Accessible Registers

Register Mnemonic	Register Bit Number							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
RBR (Read Only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)*
THR (Write Only)	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
IER	0	0	0	0	(EDSSI) Enable Modem Status Interrupt	(ELSI) Enable Receiver Line Status Interrupt	(ETBEI) Enable Transmitter Holding Register Empty Interrupt	(ERBFI) Enable Received Data Available Interrupt
IIR (Read Only)	0	0	0	0	0	Interrupt ID Bit (1)	Interrupt ID Bit (0)	"0" 1F Interrupt Pending
LCR	(DLAB) Divisor Latch Access Bit	Set Break	Stick Parity	(EPS) Even Parity Select	(PEN) Parity Enable	(STB) Number of Stop Bits	(WLSB1) Word Length Select Bit 1	(WLSB0) Word Length Select Bit 0
MCR	0	0	0	Loop	Out 2	Out 1	(RTS) Request To Send	(DTR) Data Terminal Ready
LSR	0	(TEMT) Transmitter Empty	(THRE) Transmitter Holding Register Empty	(BI) Break Interrupt	(FE) Framing Error	(PE) Parity Error	(OE) Overrun Error	(DR) Data Ready
MSR	(DCD) Data Carrier Detect	(RI) Ring Indicator	(DSR) Data Ready Set	(CTS) Clear to Send	(DDCD) Delta Data Carrier Detect	(TERI) Trailing Edge Ring Indicator	(DDSR) Delta Data Set Ready	(DCTS) Delta Clear to Send
SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

*LSB Data Bit 0 is the first bit transmitted or received.

Table 7. Baud Rates (1.8432 MHz Clock)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	2304	–
75	1536	–
110	1047	0.026
134.5	857	0.058
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.69
2400	48	–
3600	32	–
4800	24	–
7200	16	–
9600	12	–
19200	6	–
38400	3	–
56000	2	2.86

Table 8. Baud Rates (2.4576 MHz Clock)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	3072	–
75	2048	–
110	1396	0.026
134.5	1142	0.0007
150	1024	–
300	512	–
600	256	–
1200	128	–
1800	85	0.392
2000	77	0.260
2400	64	–
3600	43	0.775
4800	32	–
7200	21	1.587
9600	16	–
19200	8	–
38400	4	–

Table 9. Baud Rates (3.072 MHz Clock)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	3840	–
75	2560	–
110	1745	0.026
134.5	1428	0.034
150	1280	–
300	640	–
600	320	–
1200	160	–
1800	107	0.312
2000	96	–
2400	80	–
3600	53	0.628
4800	40	–
7200	27	1.23
9600	20	–
19200	10	–
38400	5	–

(d) Real Time Counter

The real time counter is divided into 4-bit digits with 2 digits being accessed during any read or write cycle. Each digit represents a BCD number and is defined in Table 13. Any unused bits are held at a logical zero and ignored during a write. An unused bit is any bit not necessary to provide a full BCD number. For example, tens of hours can not legally exceed the number 2, thus only 2 bits are necessary to define the tens of hours. The other 2 bits in the tens of hours digit are unused. The unused bits are designated in Table 1 as dashes.

The addressable portion of the counter is from milliseconds to months. The counter itself is a ripple counter. The ripple delay is less than 60μs above 4.0V and 300μs at 2.0V.

RAM

56 bits of RAM are contained on-chip. These can be used for any necessary power down storage or as an alarm latch for comparison to the real time counter. The data in the RAM can be compared to the real time counter on a digit basis. The only digits that are not compared are the unit ten thousandths of seconds and tens of days of the week (these are unused in the real time counter). If the two most significant bits of any RAM digit are ones then this RAM location will always compare.

Table 10. Reset Control of Register and Pinout Signals

Register/Signal	Reset Control	Reset Status
Interrupt Enable Register	Reset	All Bits low
Interrupt Identification Register	Reset	Bit 0 is high and Bits 1-7 are low
Line Control Register	Reset	All Bits low
Modem Control Register	Reset	All Bits low
Line Status Register	Reset	Bits 5, 6 are high, others are low
Modem Status Register	Reset	Bits 0-3 are low, Bits 4-7 are input signal
SOUT	Reset	High
RTS DTR	Reset	High
COMIRQ	Reset	High-Impedance
STB, AFD, SLIN	Reset	High
INIT	Reset	Low

Table 11. Parallel Port Registers

Register	Register Bits							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Read Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Read Status	BUSY	ACK	PE	SLCT	ERROR	1	1	1
Read Control	1	1	1	LPTIRQ ENB	SLIN	INIT	AUTOFD	STROBE
Write Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Write Control	1	1	1	LPTIRQ ENB	SLIN	INIT	AUTOFD	STROBE

Table 12. Parallel Port Register Select

Control Pins				Register Selected
$\overline{IOR}$	$\overline{IOW}$	A1	A0	
0	1	0	0	Read Data
0	1	0	1	Read Status
0	1	1	0	Read Control
1	0	0	0	Write Data
1	0	0	1	Invalid
1	0	1	0	Write Control

The RAM is formatted the same as the real time counter. 4 bits per digit, 14 digits, however there are no unused bits. The unused bits in the real time counter will compare only to zeros in the RAM.

Interrupts and Comparator

There is one interrupt output. The most flexible is the RTCIRQ OUTPUT (a true high signal). This output can be programmed to provide 8 different output signals. They are: 10 Hz, 1 Hz, once per minute, once per hour, once a day, once a week, once a month, and when a RAM/real time counter comparison occurs. To enable the output a one is written into the interrupt control register at the bit location corresponding to the desired output frequency Once one or more bits have been set in the interrupt

Table 13. Real Time Counter Format

Counter Addressed		Units D0	D1	D2	D3	Max. BCD Code	Tens D4	D5	D6	D7	Max. BCD Code
1/10,000 of Seconds	(00H)	–	–	–	–		D4	D5	D6	D7	9
Hundredths and Tenths Sec	(01H)	D0	D1	D2	D3	9	D4	D5	D6	D7	9
Seconds	(02H)	D0	D1	D2	D3	9	D4	D5	D6	–	5
Minutes	(03H)	D0	D1	D2	D3	9	D4	D5	D6	–	5
Hours	(04H)	D0	D1	D2	D3	9	D4	D5	–	–	2
Day of the Week	(05H)	D0	D1	D2	–	7	–	–	–	–	0
Day of the Month	(06H)	D0	D1	D2	D3	9	D4	D5	–	–	3
Month	(07H)	D0	D1	D2	D3	9	D4	–	–	–	1

(–) Indicates unused bits

control register, the corresponding counter's rollover to reset state will clock the interrupt status register and cause the interrupt output to go high. To reset the interrupt and to identify which frequency caused the interrupt, the interrupt status register is read. Reading this register places the contents of the status register on the data bus. The interrupt frequency will be identified by a one in the respective bit position. Removing the read will reset the interrupt.

The comparator is a cascaded exclusive NOR. Its output is latched 61μs after the rising edge of the 1KHz clock signal (input to the ten thousandth of seconds counter). This allows the counter to ripple through before looking at the comparator.

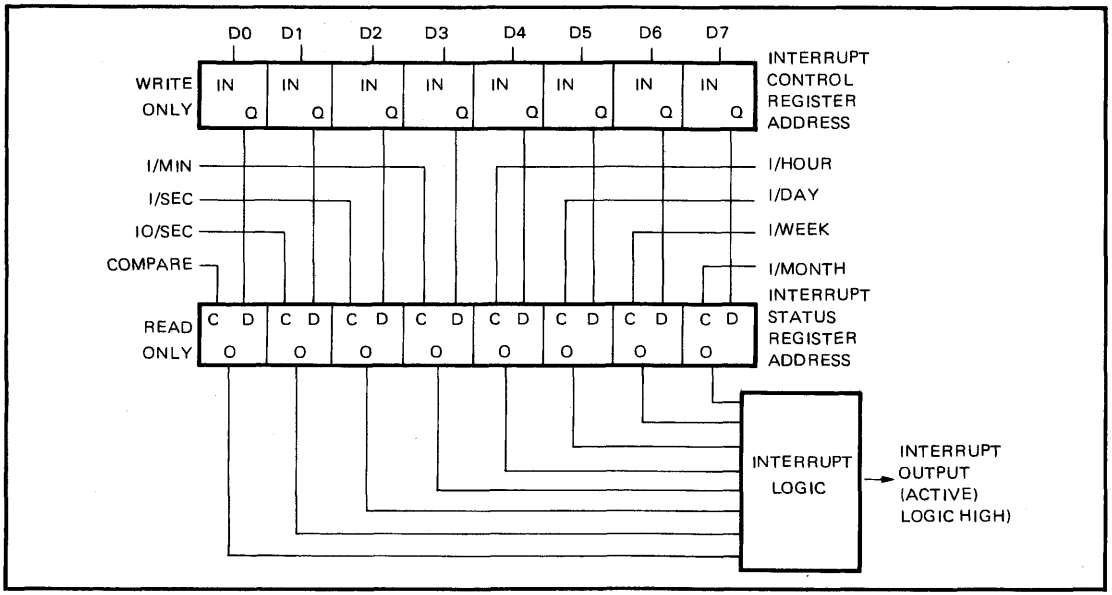


Figure 4. Interrupt Register Format

Table 14. Address Codes and Functions

A4	A3	A2	A1	A0	Function
0	0	0	0	0	Counter – Thousandths of Seconds
0	0	0	0	1	Counter – Hundredths and Tenths of Seconds
0	0	0	1	0	Counter – Seconds
0	0	0	1	1	Counter – Minutes
0	0	1	0	0	Counter – Hours
0	0	1	0	1	Counter – Day of the Week
0	0	1	1	0	Counter – Day of the Month
0	0	1	1	1	Counter – Months
0	1	0	0	0	Latches – Thousandths of Seconds
0	1	0	0	1	Latches – Hundredths and Tenths of Seconds
0	1	0	1	0	Latches – Seconds
0	1	0	1	1	Latches – Minutes
0	1	1	0	0	Latches – Hours
0	1	1	0	1	Latches – Day of the week
0	1	1	1	0	Latches – Day of the Month
0	1	1	1	1	Latches – Months
1	0	0	0	0	Interrupt Status Register
1	0	0	0	1	Interrupt Control Register
1	0	0	1	0	Counter Reset
1	0	0	1	1	Latch Reset
1	0	1	0	0	Status Bit
1	0	1	0	1	"GO" Command
1	0	1	1	0	Standby Interrupt
1	1	1	1	1	Test Mode

All others unused.

Table 15. Counter and Latch Reset Format

D0	D1	D2	D3	D4	D5	D6	D7	Counter or Latch Reset
1	0	0	0	0	0	0	0	Thousandths of Seconds
0	1	0	0	0	0	0	0	Hundredths and Tenths of Seconds
0	0	1	0	0	0	0	0	Seconds
0	0	0	1	0	0	0	0	Minutes
0	0	0	0	1	0	0	0	Hours
0	0	0	0	0	1	0	0	Day of the Week
0	0	0	0	0	0	1	0	Day of the Month
0	0	0	0	0	0	0	1	Months

For Counter Reset A4–A0 Must be 10010

For Latch Reset A4-A0 Must Be 10011

For operation at less than 4.0V, the thousandth of seconds counters should not be included in a compare because of the possibility of having a ripple delay greater than 61μs. (For output timing see interrupt timing).

Tables 14 and 15 are referred for the address input codes and functions and for the counter and latch reset format.

Power Down Mode

The POWER DOWN input is essentially a second chip select. It disables all inputs and outputs. When this input is at a logic zero, the device will not respond to any external signals. (The programming must be done before the POWER DOWN input goes to a logic zero). When switching V_{DD} to the standby or power done mode, the POWER DOWN input should go to a logic zero at least 1μs before V_{DD} is switched. When switching V_{DD} all other inputs must remain between $V_{SS}-0.3V$ and V_{DD} + 0.3V. When restoring V_{DD} to the normal operating mode, it is necessary to insure that all other inputs are at valid levels before switching the POWER DOWN input back to a logic one. These precautions are necessary to insure that no data is lost or altered when changing to or from the power down mode.

Counter and RAM Resets: Go Command

The counter's and RAM can be reset by writing all 1's (FF) at addresses 12H or 13H respectively.

A write pulse at address 15H will reset the thousandths hundredths, tenths, units and tens of seconds counters. This GO command is used for precise starting of the clock. the data on the data bus is ignored during the writing. If the seconds counter is at a value greater than 39. When the GO is issued the minute counter will increment: otherwise the minute counter is unaffected. This command is not necessary to start the clock but merely a convenient way to start precisely at a given minute.

(e) GAME PORT:
Game: 201

I/O Write:

7	6	5	4	3	2	1	0	Function
							x	A Paddle Coordinate
						x		B Paddle Coordinate
					x			C Paddle Coordinate
				x				D Paddle Coordinate
			x					Status of A Paddle Button
		x						Status of B Paddle Button
	x							Status of C Paddle Button
x								Status of D Paddle Button

Status Bit

The status bit is provided to inform the user the clock is in the process of rolling over when a counter is read. The status bit is set if this 1 KHz clock occurs during or after any counter read. This tells the user that the clock is rippling through the real time counter. Because the clock is rippling, invalid data may be read from the counter. If the status bit is set following a counter read, the counter should be read.

The status bit appears on D0 when address 14H is read. All the other data lines will be zero. The bit is set when a logical one appears. This bit should be read every time a counter read or after a series of counter reads are done. The trailing edge of the read at address 14H will reset the status bit.

Oscillator

The oscillator is the standard parallel resonant oscillator. Externally, 2 capacitors, a 20M Ohm resistor and the crystal are required. The 20M Ohm resistor is connected between X1 and X2 to bias the internal inverter in the linear region. For micropower crystals a resistor in series with the oscillator output may be necessary to insure the crystal is not overdriven. This resistor should be approximately 200K Ohms. The capacitor values should be typically 300pF. The crystal frequency is 32,768 Hz.

The oscillator input can be externally driven, if desired. In this case the output should be left floating and the input level should be within 0.3V of the supplies.

Test Mode

The test mode is merely a mode for production testing. It allows the counters to count at a higher than normal rate. In this mode the 32 KHz oscillator input is connected directly to the ten thousandths of seconds counter. The chip select and write lines must be low and the address must be held at 1 FH.

I/O Read:

7	6	5	4	3	2	1	0	Function
							x	A Joystick X Coordinate
						x		A Joystick Y Coordinate
					x			B Joystick X Coordinate
				x				B Joystick Y Coordinate
			x					Status of A Joystick Button 1
		x						Status of A Joystick Button 2
	x							Status of B Joystick Button 1
x								Status of B Joystick Button 2

Absolute Maximum Ratings *

Operating Temperature . . . . . 0°C to 70°C
Storage Temperature . . . . . –55°C to 150°C
All Output Voltages . . . . . –0.5V to +7V
All Input Voltages . . . . . –0.5V to +7V
Supply Voltage V_{CC} . . . . . 5V ± 10%
Power Dissipation 0.5W

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = 0°C to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{CC}	Supply Voltage	4.5		5.5	V	Output Enable
V_{CC}	Supply Voltage	2.0		5.5	V	Power Down
V_{IL}	Input Low Voltage	–0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 6 mA
						I_{OL} = 12 mA, (PD0 ~ PD7)
V_{OH}	Output High Voltage	2.4			V	I_{OH} = 2 mA
						I_{OH} = 4 mA, (PD0 ~ PD7)
V_{IHR} ~ V_{ILR}	Schmitt Trigger Hysteresis	0.25			V	RESET, CLKIN RTCCS0(1), COMCS LPTCS0(1)
I_{CC}	Power Supply Current			20	μA	Power Down
				50	mA	Output Enable

AC Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%)

Input Requirement

No.	Symbol	Parameter	Min.	Typ.	Max.	Unit
1	t_{AW}	$\overline{IOW}$ Delay Time from Address	50			ns
2	t_{WA}	Address Hold Time from $\overline{IOW}$	20			ns
3	t_{DS}	Data Setup Time to $\overline{IOW}$	40			ns
4	t_{DH}	Data Hold Time from $\overline{IOW}$	40			ns
5	t_{AR}	$\overline{IOR}$ Delay Time from Address	50			ns
6	t_{RA}	Address Hold Time from $\overline{IOR}$	20			ns

Output Response

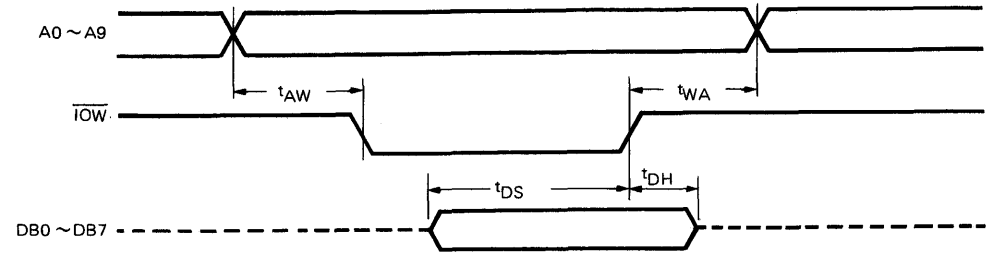
7	t_{RD}	Data Delay Time from $\overline{IOR}$			125	ns
8	t_{HZ}	Data Floating Time from $\overline{IOR}$	0		100	ns

AC Characteristics (Continued)

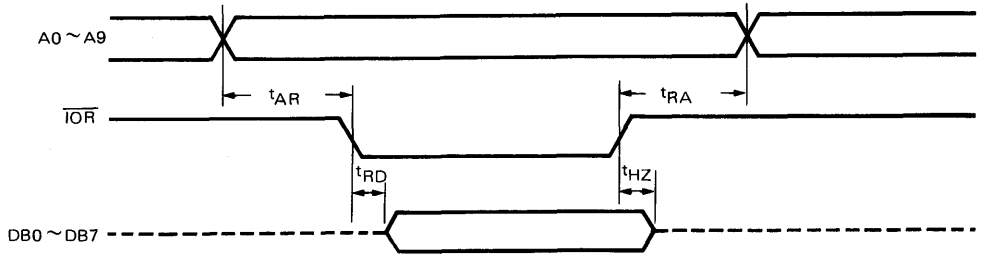
No.	Symbol	Parameter	Min.	Typ.	Max.	Unit
9	t_{SINT}	Set Interrupt Delay Time from Stop Bit	1		1	CLK cycle
10	t_{RINT}	Reset Interrupt Delay Time from RD RBR/LSR			1	μs
12	t_{IRS}	Transmit Start Delay Time from Initial INTR	8		24	CLK cycle
13	t_{SI}	Set Interrupt Delay Time from Initial write	16		32	CLK cycle
14	t_{STI}	Set Interrupt Delay Time from Stop Bit	8		8	CLK cycle
15	t_{IR}	Reset Interrupt Delay from RD IIR			250	ns
16	t_{MDO}	MODEM Output Delay Time from WR MCR			200	ns
17	t_{SIM}	Set Interrupt Delay Time from MODEM Input			200	ns
18	t_{RIM}	Reset Interrupt Delay Time from RD MSR			250	ns
19	t_{PPW}	Parallel Port Delay Time from WR PDR or PCR			300	ns
20	t_{SIAK}	Set Interrupt Delay Time from ACK			200	ns
21	t_{GMRW}	Game Command Delay Time from RD/WR Game Port			150	ns

Timing Waveforms

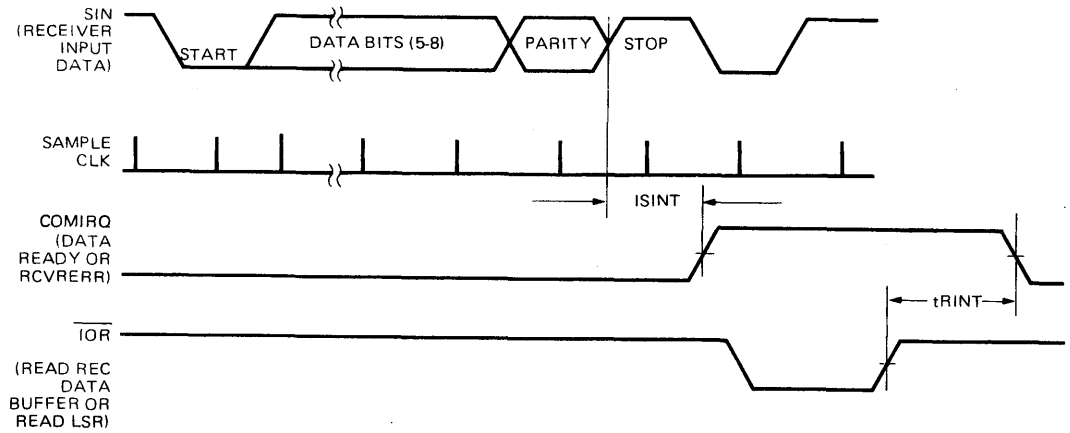
Write Cycle Timing



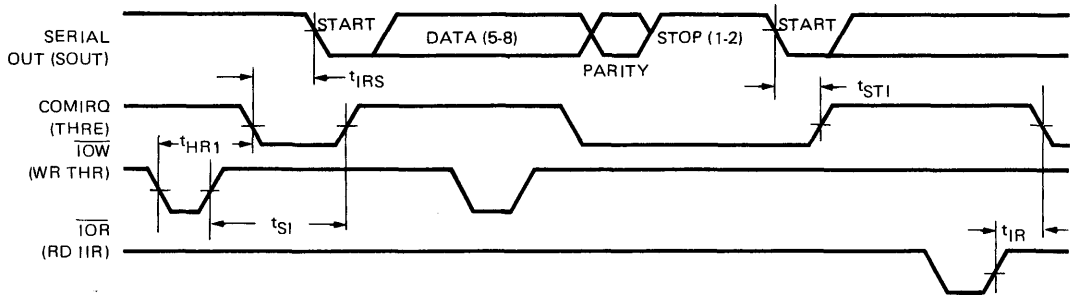
Read Cycle Timing



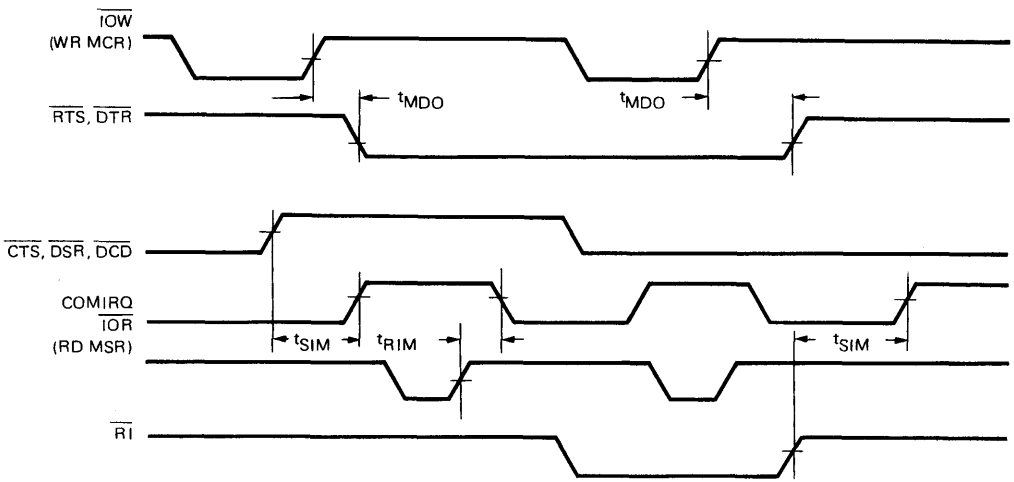
Timing Waveforms (Continued)



Transmitter Timing

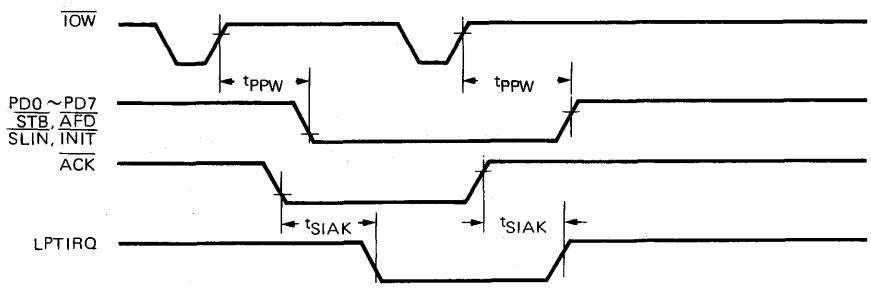


Modem Timing



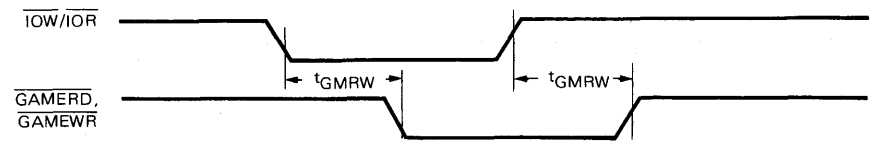
Timing Waveforms (Continued)

PARALLEL PORT TIMING

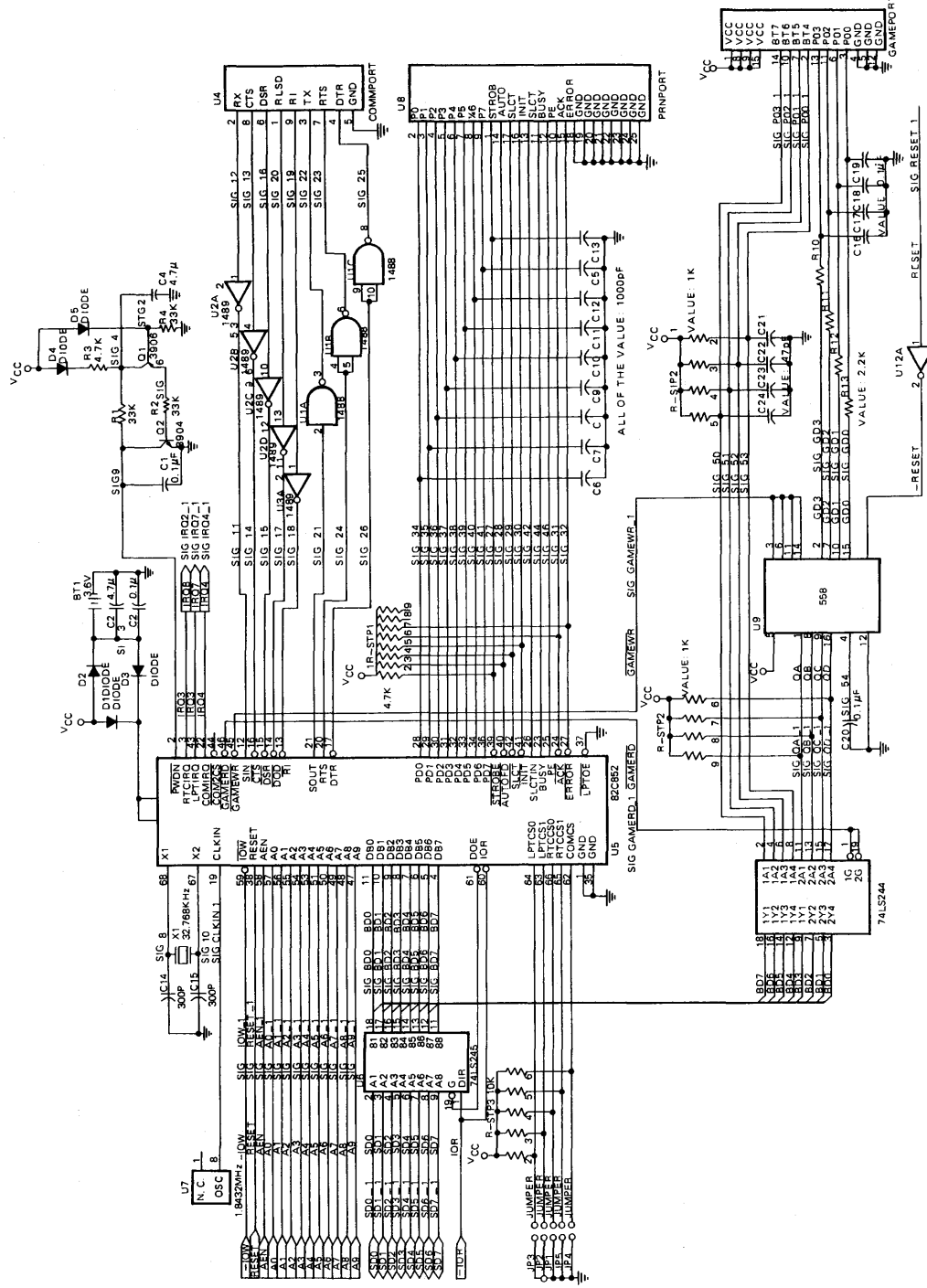


** Outputs of STB, AFD, SLIN and INIT are pulled up by 1K ohms resisters.

Game Port Timing



Application Circuit



UM82450

Asynchronous Communication Element (ACE)

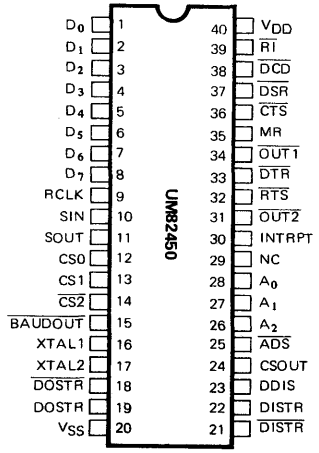
Features

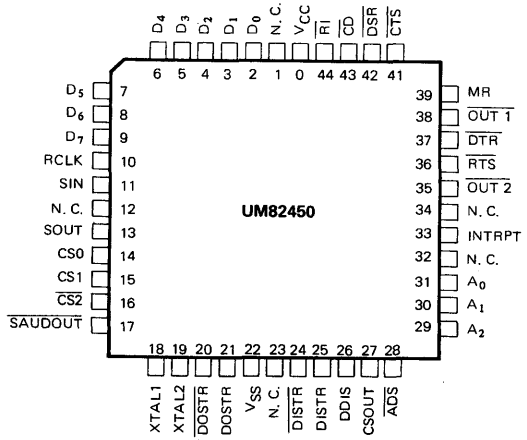
- Adds or deletes standard asynchronous communication bits (start, stop, and parity) to or from a serial data stream
- Full double buffering eliminates the need for precise synchronization
- Independently controlled transmit, receive, line status, and data set interrupts
- Programmable baud rate generator allows division of any input clock by 1 to $2^{16}-1$ and generates the internal 16x clock
- Independent receiver clock input
- Modem control functions (CTS, RTS, DSR, DTR, RI, and DCD)
- Single +5 volt power supply
- TRI-STATE TTL Drive capabilities for bidirectional data bus and control bus.
- Fully programmable serial-interface characteristics
  - 5-, 6-, 7-, or 8-bit characters
  - Even, odd, or no-parity bit generation and detection
  - 1-, 1½-, or 2-stop bit generation
  - Baud rate generation (DC to 56k baud)
- False start bit detection
- Complete status reporting capabilities
- Easily interfaces to most popular microprocessors
- Line break generation and detection
- Internal diagnostic capabilities
  - Loopback controls for communications link fault isolation
  - Break, parity, overrun, framing error simulation
- Fully prioritized interrupt system controls

General Description

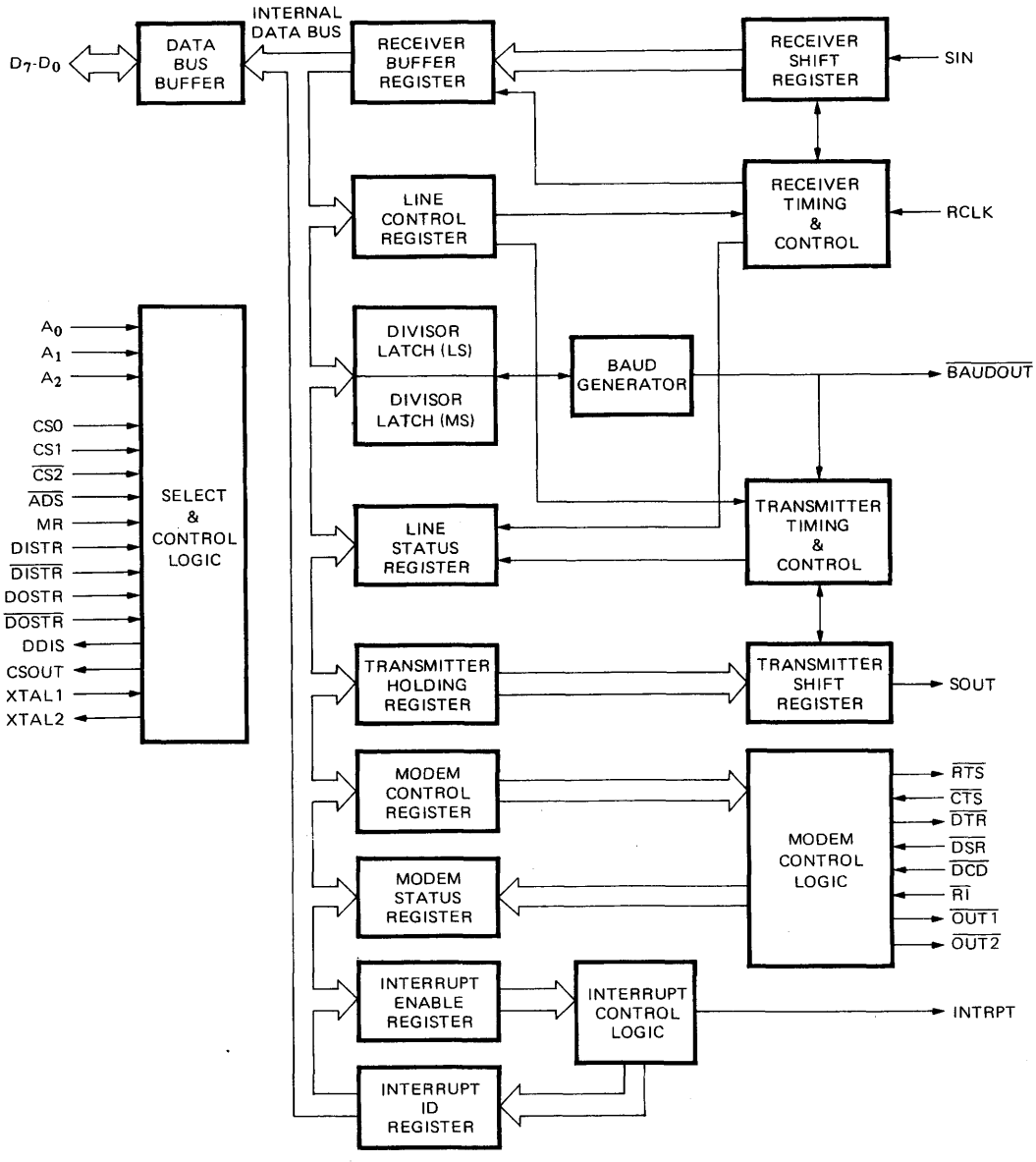
UM82450 is a programmable Asynchronous Communication Element (ACE) chip fabricated using the Si-Gate NMOS process. The UM82450 is an improved version of the UM8250. It performs serial-to-parallel conversion on data characters received from a peripheral device or a modem, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the ACE at any time during functional operation. It also includes a programmable baud rate generator that is capable of dividing the timing reference clock input by divisors of 1 to 2^{16} - 1, and producing a 16x clock for driving the internal transmitter logic.

Pin Configurations





Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +150°C
All Input or Output Voltages with
Respect to V_{SS} . . . . . −0.5V to +7.0V
Power Dissipation . . . . . 700 mW

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

T_A = 0°C to +70°C, V_{DD} = +5V ± 5%, V_{SS} = 0V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{ILX}	Clock Input Low Voltage		−0.5	0.8	V
V_{IHX}	Clock Input High Voltage		2.0	V_{CC}	V
V_{IL}	Input Low Voltage		−0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA on all*		0.4	V
V_{OH}	Output High Voltage	I_{OL} = −1.0 mA*	2.4		V
I_{CC} (AV)	Avg Power Supply Current (V_{CC})	V_{CC} = 5.25V, T_A = 25°C No Loads on output SIN, DSR, RLSD, CTS, RI = 2.0V All other inputs = 0.8V		120	mA
I_{IL}	Input Leakage	V_{CC} = 5.25V, V_{SS} = 0V All other pins floating. V_{IN} = 0V, 5.25V		±10	μA
I_{CL}	Clock Leakage			±10	μA
I_{OZ}	TRI-STATE Leakage	V_{CC} = 5.25V, V_{SS} = 0V V_{OUT} = 0V, 5.25V 1) Chip deselected 2) WRITE Mode, chip selected		±20	μA
V_{ILMR}	MR Schmitt V_{IL}			0.8	V
V_{IHMR}	MR Schmitt V_{IH}		2.0		V

* Does not apply to XTAL2

Capacitance

T_A = 25°C, V_{CC} = V_{SS} = 0V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C_{XTAL2}	Clock Input Capacitance	f_c = 1 MHz Unmeasured pins returned to V_{SS}		15	20	pF
C_{XTAL1}	Clock Output Capacitance			20	30	pF
C_{IN}	Input Capacitance			6	10	pF
C_{OUT}	Output Capacitance			10	20	pF

AC Characteristics

T_A = 0°C to b 70°C, V_{DD} = +5V ± 5%

Symbol	Parameter	Conditions	Min.	Max.	Units
t_{AW}	Address Strobe Width		60	–	ns
t_{AS}	Address Setup Time		60		ns
t_{AH}	Address Hold Time		0		ns
t_{CS}	Chip Select Setup Time		60		ns
t_{CH}	Chip Select Hold Time		0		ns
t_{DIW}	$\overline{DISTR}$/DISTR Strobe Width		125		ns
t_{RC}	Read Cycle Delay		175		ns
RC	Read Cycle = t_{AR}* + t_{DIW} + t_{RC}		360		ns
t_{DD}	$\overline{DISTR}$/DISTR to Driver Disable Delay	@ 100 pF loading ***		60	ns
t_{DDD}	Delay from $\overline{DISTR}$/DISTR to Data	@ 100 pF loading		125	ns
t_{HZ}	$\overline{DISTR}$/DISTR to Floating Data Delay	@ 100 pF loading ***	0	100	ns
t_{DOW}	$\overline{DOSTR}$/DOSTR Strobe Width		100		ns
t_{WC}	Write Cycle Delay		200		ns
WC	Write Cycle = t_{AW} + t_{DOW} + t_{WC}		360		ns
t_{DS}	Data Setup Time		40		ns
t_{DH}	Data Hold Time		40		ns
t_{CSC}*	Chip Select Output Delay from Select	@ 100 pF loading		100	ns
t_{RA}*	Address Hold Time from $\overline{DISTR}$/DISTR		20		ns
t_{RCS}*	Chip Select Hold Time from $\overline{DISTR}$/DISTR		20		ns
t_{AR}*	$\overline{DISTR}$/DISTR Delay from Address		60		ns
t_{CSR}*	$\overline{DISTR}$/DISTR Delay from Chip Select		50		ns
t_{WA}*	Address Hold Time from $\overline{DOSTR}$/DOSTR		20		ns
t_{WCS}*	Chip Select Hold Time from $\overline{DOSTR}$/DOSTR		20		ns
t_{AW}*	$\overline{DOSTR}$/DOSTR Delay from Address		60		ns
t_{CSW}*	$\overline{DOSTR}$/DOSTR Delay from Select		50		ns
t_{MRW}	Master Reset Pulse Width		5		ns
t_{XH}	Duration of Clock High Pulse	External Clock (3.1 MHz Max.)	140		µs
t_{XL}	Duration of Clock Low Pulse	External Clock (3.1 MHx Max.)	140		ns
Baud Generator					
N	Baud Divisor		1	$2^{16}-1$	
t_{BLD}	Baud Output Negative Edge Delay	100 pF Load		125	ns
t_{BHD}	Baud Output Positive Edge Delay	100 pF Load		125	ns
t_{LW}	Baud Output Down Time	f_X = 2 MHz, ÷ 2, 100 pF Load	425		ns
t_{HW}	Baud Output Up Time	f_X = 3 MHz, ÷ 3, 100 pF Load	330		ns
Receiver					
t_{SCD}	Delay from RCLK to Sample Time			2	µs
t_{SINT}	Delay from Stop to Set Interrupt		1	1	RCLK** Cycles
t_{RINT}	Delay from $\overline{DISTR}$/DISTR (RD RBR/RDLSR) to Reset Interrupt	100 pF Load		1	µs

*Applicable only when $\overline{ADS}$ is tied low.

**RCLK is equal to t_{XH} and t_{XL}.

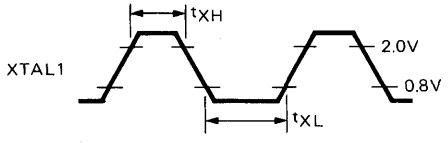
***Charge and discharge time is determined by V_{OL}, V_{OH} and the external loading.

AC Characteristics (Continued)

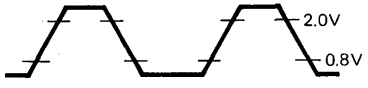
Symbol	Parameter	Conditions	Min.	Max.	Unit
Transmitter					
t_{HR}	Delay from $\overline{DOSTR}$/DOSTR (WR THR) to Reset Interrupt	100 pF Load		175	ns
t_{IRS}	Delay from Initial INTR Reset to Transmit Start		8	24	RCLK Cycles
t_{SI}	Delay from Initial Write to Interrupt		16	32	RCLK Cycles
t_{STI}	Delay from Stop to Interrupt (THRE)		8	8	RCLK Cycles
t_{IR}	Delay from $\overline{DISTR}$/DISTR (RD IIR) to Reset Interrupt (THRE)	100 pF Load		250	ns
Modem Control					
t_{MDO}	Delay from $\overline{DOSTR}$/DOSTR (WR MCR) to Output	100 pF Load		200	ns
t_{SIM}	Delay to Set Interrupt from MODEM Input	100 pF Load			ns
t_{RIM}	Delay to Reset Interrupt from $\overline{DISTR}$/ DISTR (RD MSR)	100 pF Load		250	ns

Timing Waveforms

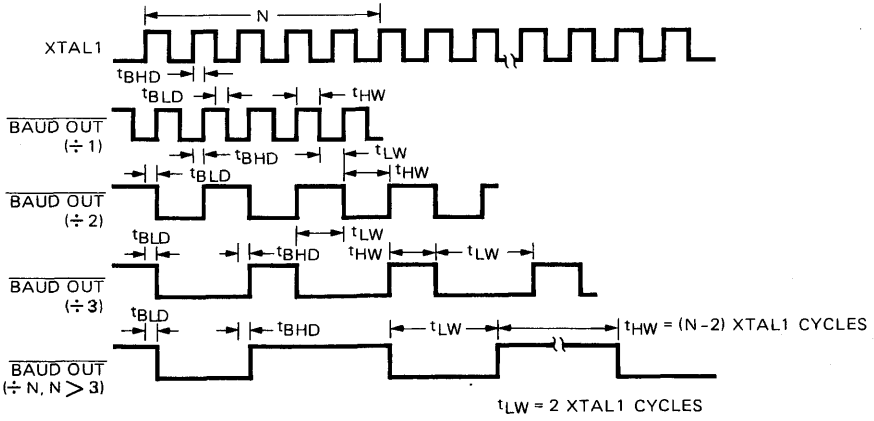
EXTERNAL CLOCK INPUT (3.1 MHz MAX.)



AC TEST POINTS

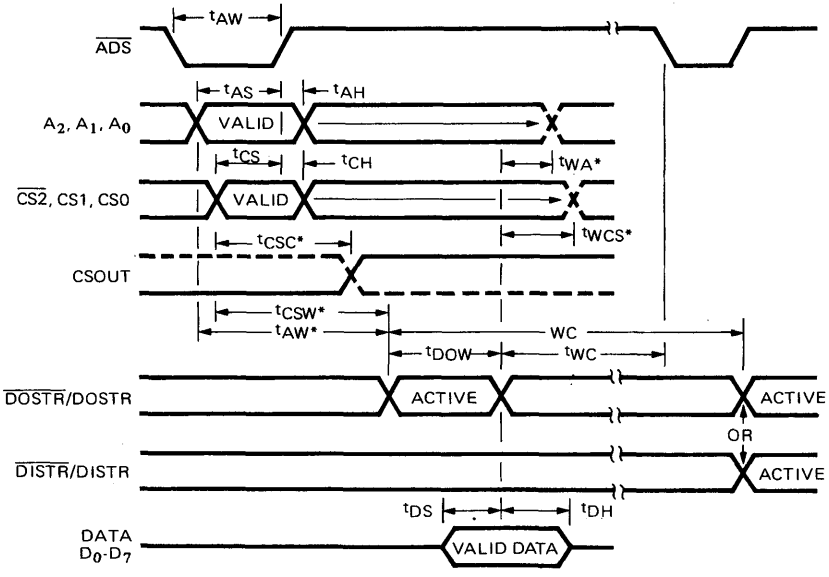


$\overline{BAUDOUT}$ TIMING



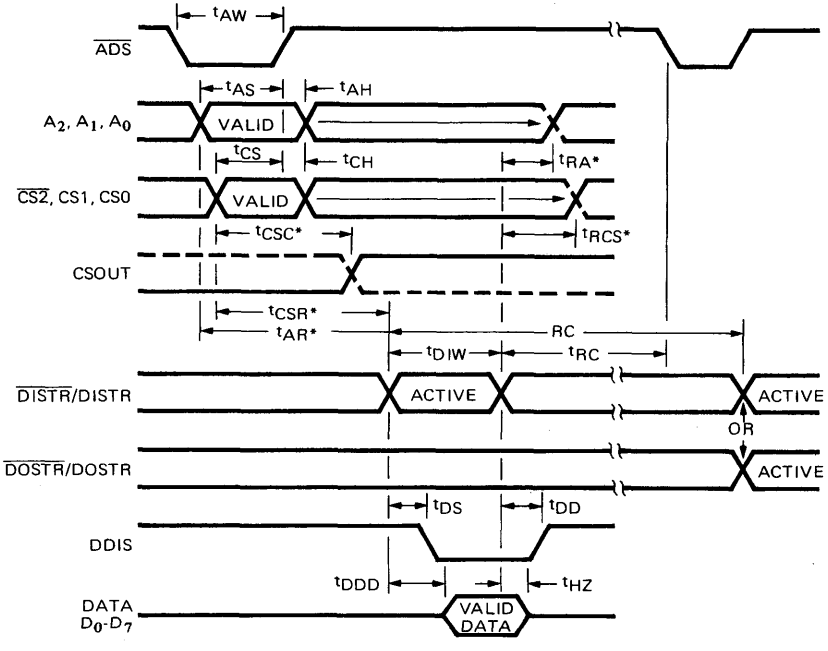
Timing Waveforms (Continued)

WRITE CYCLE



*Applicable Only When $\overline{ADS}$ is Tied Low.

READ CYCLE

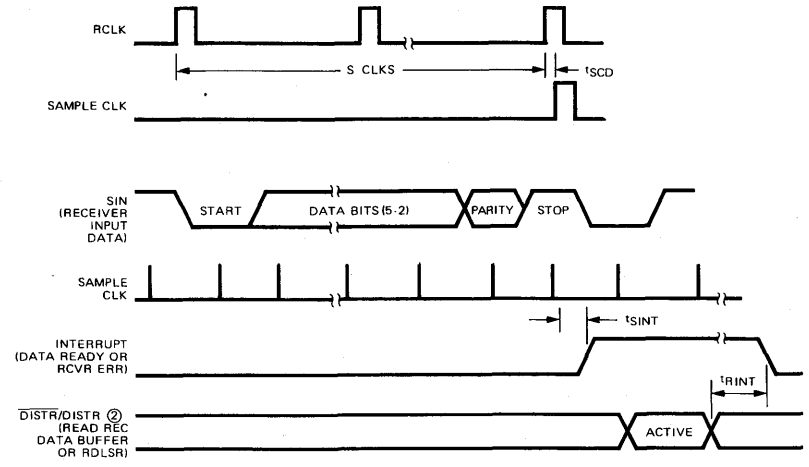


*Applicable Only When $\overline{ADS}$ is Tied Low.

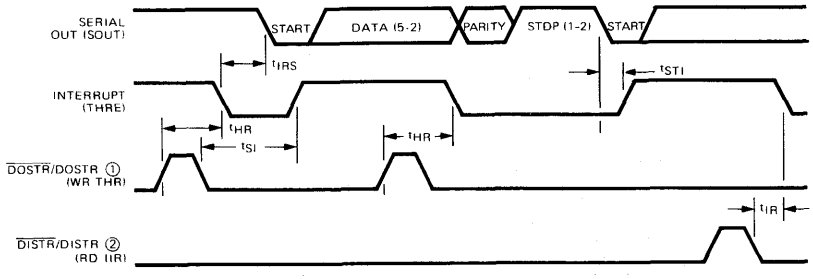
I/O And Peripherals

Timing Waveforms (Continued)

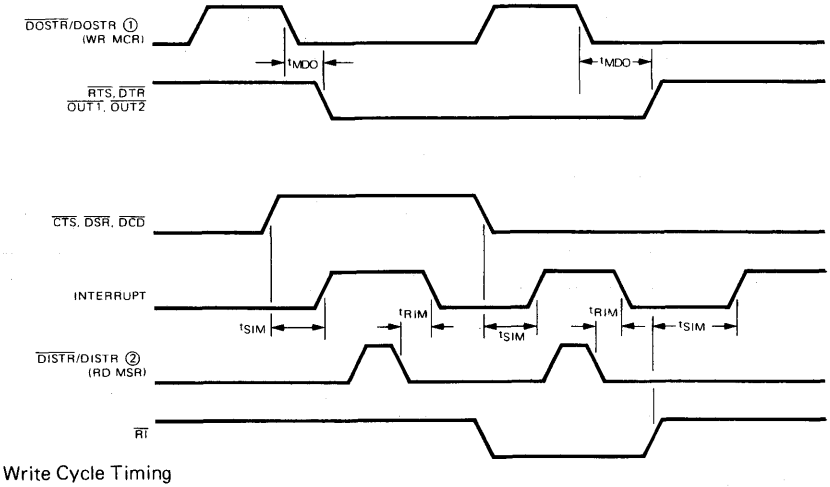
RECEIVER TIMING



TRANSMITTER TIMING



MODEM CONTROL TIMING



Note: 1. See Write Cycle Timing
2. See Read Cycle Timing

Pin Description

Input Signals

Chip Select (CS0, CS1, $\overline{CS2}$), Pins 12–14: When CS0 and CS1 are high and $\overline{CS2}$ is low, the chip is selected. Chip selection is complete when the decoded chip select signal is latched with an active (low) Address Strobe ($\overline{ADS}$) input. This enables communication between the ACE and the CPU.

Data Input Strobe (DISTR, $\overline{DISTR}$), Pins 22 and 21: When DISTR is high or $\overline{DISTR}$ is low while the chip is selected, it allows the CPU to read status information or data from a selected register of the ACE. Only an active DISTR or $\overline{DISTR}$ input is required to transfer data from the ACE during a read operation. Therefore, tie either the DISTR input permanently low or the $\overline{DISTR}$ input permanently high, if not used.

Data Output Strobe (DOSTR, $\overline{DOSTR}$), Pins 19 and 18: The DOSTR is high or $\overline{DOSTR}$ is low while the chip is selected, which allows the CPU to write data or control words into a selected register of the ACE. Only an active DOSTR or $\overline{DOSTR}$ input is required to transfer data to the ACE during a write operation. Therefore, tie either the $\overline{DOSTR}$ input permanently low or the DOSTR input permanently high, if not used.

Address Strobe ($\overline{ADS}$), Pin 25: When this is low, it provides latching for the Register Select (A_0, A_1, A_2) and Chip Select (CS0, CS1, $\overline{CS2}$) signals. An active $\overline{ADS}$ input is required when the Register Select (A_0, A_1, A_2) signals are not stable for the duration of a read or write operation. If not required, tie the $\overline{ADS}$ input permanently low.

Register Select (A_2, A_1, A_0), Pins 26–28: These three inputs are used during a read or write operation to select an ACE register to read from or write to as indicated in Table 1. The DLAB must be set high by the system software to access the Baud Generator Divisor Latches.

Master Reset (MR), Pin 35: This input is buffered with a TTL-compatible Schmitt Trigger with 0.5V typical hysteresis. When high, it clears all the registers (except the Receiver Buffer, Transmitter Holding, and Divisor Latches), and the control logic of the ACE. Also, the state of various output signals (SOUT, INTRPT, $\overline{OUT1}$, $\overline{OUT2}$, $\overline{RTS}$, $\overline{DTR}$) are affected by an active MR input. (Refer to Table 2)

Receiver Clock (RCLK), Pin 9: This input is the 16 x baud rate clock for the receiver section of the chip.

Serial Input (SIN), Pin 10: Serial data input from the communications link (peripheral device, MODEM, or data set).

Clear to Send ($\overline{CTS}$), Pin 36: The $\overline{CTS}$ signal is a MODEM control function input whose conditions can be tested by the CPU by reading bit 4 (CTS) of the MODEM Status Register. Bit 0 (DCTS) of the MODEM Status Register indicates whether the $\overline{CTS}$ input has changed state since the previous reading of the MODEM Status Register. $\overline{CTS}$ has no effect on the Transmitter. Whenever the CTS bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

DLAB	A_2	A_1	A_0	Register
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	1	Line Control
X	1	0	0	MODEM Control
X	1	0	1	Line Status
X	1	1	0	MODEM Status
X	1	1	1	Scratch
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

Table 1. Register address

Data Set Ready ($\overline{DSR}$), Pin 37: When low, this indicates that the MODEM or data set is ready to establish the communications link and transfer data with the ACE. The $\overline{DSR}$ signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 5 (DSR) of the MODEM Status Register. Bit 1 (DDSR) of the MODEM Status Register indicates whether the $\overline{DSR}$ input has changed state since the previous reading of the MODEM Status Register. Whenever the DSR bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Data Carrier Detect ($\overline{DCD}$), Pin 38: When low, this indicates that the data carrier has been detected by the MODEM or data set. The $\overline{DCD}$ signal is a MODE-control function input whose condition can be tested by the CPU by reading bit 7 (DCD) of the MODEM Status Register. Bit 3 (DDCD) of the MODEM Status Register indicates whether the $\overline{DCD}$ input has changed state since the previous reading of the MODEM Status Register. $\overline{DCD}$ has no effect on the receiver. Whenever the DCD bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Ring Indicator ($\overline{RI}$), Pin 39: When low, it indicates that a telephone ringing signal has been received by the MODEM or data set. The $\overline{RI}$ signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 6 (RI) of the MODEM Status Register. Bit 2 (TERI)

of the MODEM Status Register indicates whether the $\overline{RI}$ input has changed from a low to a high state since the previous reading of the MODEM Status Register. Whenever the RI bit of the MODEM Status Register changes from a high to a low state, an interrupt is generated if the MODEM Status Register is enabled.

V_{DD}, Pin 40: +5V supply.

V_{SS}, Pin 20: Ground (0V) reference.

Output Signals

Data Terminal Ready ($\overline{DTR}$), Pin 33: When low, this informs the MODEM or data set that the ACE is ready to communicate. The DTR output signal can be set to an active low by programming bit 0 (DTR) of the MODEM Control Register to a high level. The DTR signal is set high upon a Master Reset operation. The DTR signal is forced to its inactive state (high) during loop mode operation.

Request to Send ($\overline{RTS}$), Pin 32: When low, this informs the MODEM or data set that the ACE is ready to transmit data. The $\overline{RTS}$ output signal can be set to an active low by programming bit 1 (RTS) of the MODEM Control Register. The $\overline{RTS}$ signal is set high upon a Master Reset operation. The $\overline{RTS}$ signal is forced to its inactive state (high) during loop mode operation.

Output 1 ($\overline{OUT\ 1}$), Pin 34: This is a User-designated output that can be set to an active low by programming bit 2 (OUT 1) of the MODEM Control Register to a high level. The $\overline{OUT\ 1}$ signal is set high upon a Master Reset Operation. The $\overline{OUT\ 1}$ signal is forced to its inactive state (high) during loop mode operation.

Output 2 ($\overline{OUT\ 2}$), Pin 31: This is a User-designated output that can be set to an active low by programming bit 3 (OUT 2) of the MODEM Control Register to a high level. The $\overline{OUT\ 2}$ signal is set high upon a Master Reset Operation. The $\overline{OUT\ 2}$ signal is forced to its inactive state (high) during loop mode operation.

Chip Select Out (CSOUT), Pin 24: When high, indicates that the chip has been selected by active, CS0, CS1, and CS2 inputs. No data transfer can be initiated until the CSOUT signal is a logic 1. CSOUT goes low when the chip is deselected.

Driver Disable (DDIS), Pin 23: This goes low whenever the CPU is reading data from the ACE. A high-level DDIS output can be used to disable an external transceiver (if used between the CPU and ACE on the D_7–D_0 Data Bus) at all times, except when the CPU is reading data.

Baud Out ($\overline{BAUDOUT}$), Pin 15: This is a 16x clock signal for the transmitter section of the ACE. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches. The BAUDOUT may also be used for the receiver section by tying this output to the RCLK input of the chip.

Interrupt (INTRPT), Pin 30: Goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER: Receiver Error Flag; Received Data Available; Transmitter Holding Register Empty and MODEM Status. The INTRPT signal is reset low upon the appropriate interrupt service or a Master Reset operation.

Serial Output (SOUT), Pin 11: Composite serial data output to the communications link (peripheral, MODEM or data set). The SOUT signal is set to the Marking (logic 1) state upon a Master Reset operation.

Input/Output Signals

Data (D_7–D_0) Bus, Pins 1–8: This bus comprises eight TRI-STATE input/output lines. The bus provides bidirectional communications between the ACE and the CPU. Data, control words and status information are transferred via the D_7–D_0 Data Bus.

External Clock Input/Output (XTAL 1, XTAL 2), Pins 16 and 17: These two pins connect the main timing reference (crystal or signal clock) to the ACE.

Programmable Registers

The system programmer may access or control any of the ACE registers summarized in Table 3 via the CPU. These registers are used to control ACE operations and to transmit and receive data.

Line Control Register

The system programmer specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format, the programmer may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. The contents of the Line Control Register are indicated in Table 3 and are described below.

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits in each transmitted character. If bit 2 is a logic 0, one Stop bit is generated in the transmitted data. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one and a half Stop bits are generated. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two Stop bits are generated. The Receiver checks the first Stop-bit only, regardless of the number of Stop bits selected.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1s is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bits 3, 4 and 5 are logic 1s the Parity bit is transmitted and checked by the receiver as a logic 0. If bits 3 and 5 are 1s and bit 4 is a logic 0 then the Parity bit is transmitted as a 0.

Bit 6: This bit is the Break Control bit. When it is set to a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state. The break is disabled by setting bit 6 to a logic 0. The Break Control bit acts only on SOUT and has no effect on the transmitter logic.

Note: This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all 0s, pad character, in response to THRE.
2. Set break after the next THRE.
3. Wait for the transmitter to be idle, (TEMT = 1), and clear the break when normal transmission has been restored.

During the break, the Transmitter can be used as a character timer to accurately establish the break duration.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

Table 2. ACE Reset Functions

Register/Signal	Reset Control	Reset State
Interrupt Enable Register	Master Reset	All Bits Low (0 - 3 forced and 4 - 7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High, Bits 1 and 2 Low Bits 3 - 7 are Permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low, Except Bits 5 & 6 are High
MODEM Status Register	Master Reset	Bits 0 - 3 Low Bits 4 - 7 — Input Signal
SOUT	Master Reset	High
INTRPT (RCVR Errs)	Read LSR/MR	Low
INTRPT (RCVR Data Ready)	Read RBR/MR	Low
INTRPT (THRE)	Read IIR/Write THR/MR	Low
INTRPT (Modem Status Changes)	Read MSR/MR	Low
$\overline{\text{OUT 2}}$	Master Reset	High
$\overline{\text{RTS}}$	Master Reset	High
$\overline{\text{DTR}}$	Master Reset	High
$\overline{\text{OUT 1}}$	Master Reset	High

Table 3. Summary of Accessible Registers

Bit No.	Register Address										
	0 DLAB=0	0 DLAB=0	1 DLAB=0	2	3	4	5	6	7	0 DLAB=1	1 DLAB=1
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident. Register (Read Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Register	Divisor Latch (LS)	Divisor Latch (MS)
	RBR	THR	IER	IIR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Data Bit 0*	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	(WL Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OR)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	0	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Data Carrier Detect (DDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

* Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Programmable Baud Generator

The ACE contains a programmable Baud Generator that is capable of taking any clock input (DC to 3.1 MHz) and dividing it by any divisor from 1 to $2^{16}-1$. The output frequency of the Baud Generator is 16 x the Baud [divisor # = (frequency input) ÷ (baud rate x 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to ensure desired operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables 4 and 5 illustrate the use of the Baud Generator with crystal frequencies of 1.8432 MHz and 3.072 MHz respectively. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen. The maximum operating frequency of the Baud Generator is 3.1 MHz. However, when using divisors of 3 and below, the maximum frequency is equal to the divisor in MHz. For example, if the divisor is 1, then the maximum frequency is 1 MHz. In no case should the data rate be greater than 56k Baud.

Line Status Register

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of the Line Status Register are indicated in Table 3 and are described below.

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 is reset to a logic 0 by reading the data in the Receiver Buffer Register.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

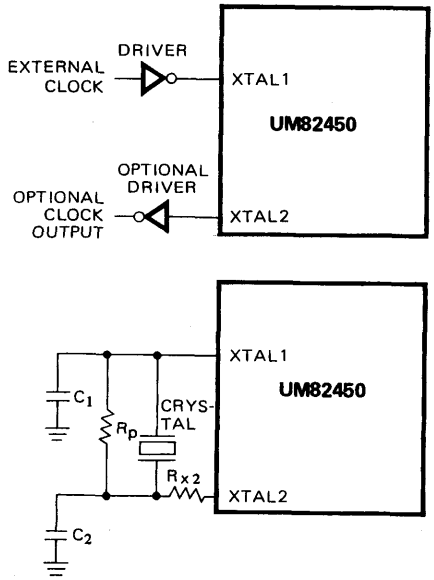
Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level). The FE indicator is reset whenever the CPU reads the contents of the Line Status indicator.

Table 4. Baud Rates Using a 1.8432 MHz Crystal

Desired Baud Rate	Divisor Used to Generate 16 x Clock	Percent Error Difference Between Desired and Actual
50	2304	–
75	1536	–
110	1047	0.026
134.5	857	0.058
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.69
2400	48	–
3600	32	–
4800	24	–
7200	16	–
9600	12	–
19200	6	–
38400	3	–
56000	2	2.86

Typical Oscillator Application



Typical Crystal Oscillator Network

Crystal	R_p	R_{x2}	C_1	C_2
3.1 MHz	1 MΩ	1.5K	10-30 pF	40-60 pF
1.8 MHz	1 MΩ	1.5K	10-30 pF	40-60 pF

Table 5. Baud Rates Using 3.072 MHz Crystal

Desired Baud Rate	Divisor Used to Generate 16 x Clock	Percent Error Difference Between Desired and Actual
50	3840	–
75	2560	–
110	1745	0.026
134.5	1428	0.034
150	1280	–
300	640	–
600	320	–
1200	160	–
1800	107	0.312
2000	96	–
2400	80	–
3600	53	0.628
4800	40	–
7200	27	1.23
9600	20	–
19200	10	–
38400	5	–

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits). The BI indicator is reset whenever the CPU reads the contents of the Line Status indicator. Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the ACE is ready to accept a new character for transmission. In addition, this bit causes the ACE to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

Bit 6: This bit is the Transmitter Empty (TEMT) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. It is reset to a logic 0 whenever either the THR or TSR contains a data character.

Table 6. Interrupt Control Functions

Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 2	**Bit 1**	**Bit 0**	**Priority Level**	**Interrupt Type**	**Interrupt Source**	**Interrupt Reset Control**
0	0	1	–	None	None	–
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Receive Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

Bit 7: This bit is permanently set to logic 0. The Line Status Register is intended for read operations only. Writing to this register is not recommended as this operation is used for factory testing.

Interrupt Identification Register

The ACE has an on-chip interrupt capability that allows for flexibility in interfacing popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the ACE prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and Modem Status (priority 4).

Information indicating that a prioritized interrupt is pending and the type of that interrupt are stored in the Interrupt Identification Register (IIR). When addressed during chip-select time, the IIR freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The contents of the IIR are indicated in Table 3 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table 5.

Bits 3 through 7: These five bits of the IIR are always logic 0.

Interrupt Enable Register

This 8-bit register enables the four types of interrupts of the ACE to separately activate the chip interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are indicated in Table 3 and are described below.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bits 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

MODEM Control Register

This 8-bit register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in Table 3 and are described below.

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1. The DTR output of the ACE may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the Output 1 ($\overline{OUT\ 1}$) signal, which is an auxiliary user-designated output. Bit 2 affects the $\overline{OUT\ 1}$ output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the Output 2 ($\overline{OUT\ 2}$) signal, which is an auxiliary user-designated output. Bit 3 affects the $\overline{OUT\ 2}$ output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a local loopback feature for diagnotic testing of the ACE. When bit 4 is set to logic 1, the following occurs: the transmitter Serial Output (SOUT) is set to the Marking (logic 1) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and RI) are disconnected; and the four MODEM Control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT\ 1}$, and $\overline{OUT\ 2}$) are internally connected to the four MODEM Control inputs, and the MODEM Control output pins are forced to their inactive state (high). In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit-and received-data paths of the ACE.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational, but the interrupts' sources are

now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

Bit 5 through 7: These bits are permanently set to logic 0.

MODEM Status Register

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

Accessible Registers

The contents of the MODEM Status Register are indicated in Table 3 and are described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the Chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from a low to a high state.

Bit 3: This bit is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the $\overline{DCD}$ input to the chip has changed state. Whenever bits 0, 1, 2, or 3 are set to logic 1, a MODEM Status Interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send ($\overline{CTS}$) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.

Bit 5: This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to DTR in the MCR.

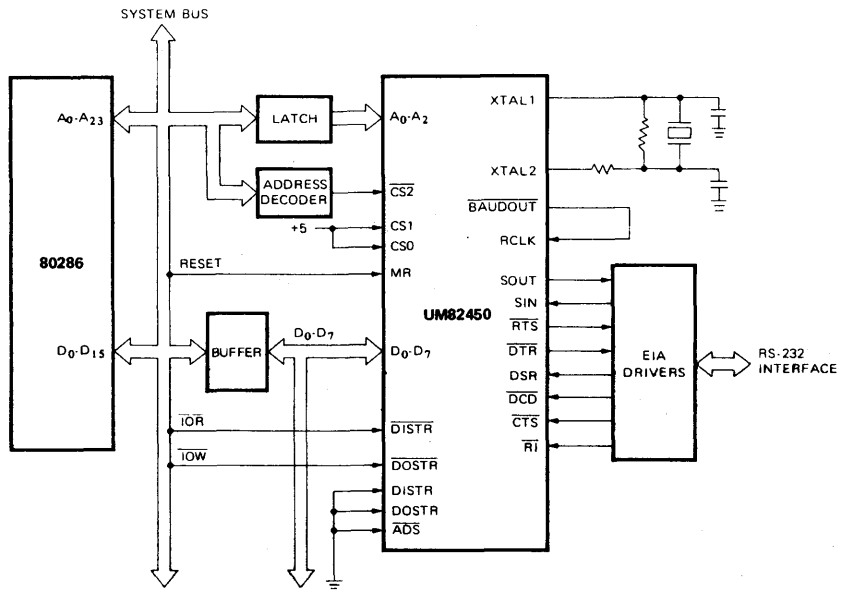
Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 1 in the MCR.

Bit 7: This bit is the complement of the Data Carrier Detect ($\overline{DCD}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 2 of the MCR.

Scratchpad Register

This 8-bit Read/Write Register does not control the ACE in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

Typical Application



Ordering Information

Part No.	Package
UM82450	40L DIP
UM82450L	44L PLCC

UMC

UMC

UM8250A

Asynchronous Communication Element (ACE)

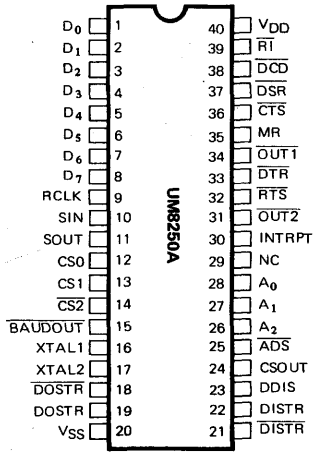
Features

- Adds or deletes standard asynchronous communication bits (start, stop, and parity) to or from a serial data stream
- Full double buffering eliminates the need for precise synchronization
- Independently controlled transmit, receive, line status, and data set interrupts
- Programmable baud rate generator allows division of any input clock by 1 to $2^{16}-1$ and generates the internal 16x clock
- Independent receiver clock input
- Modem control functions (CTS, RTS, DSR, DTR, RI, and DCD
- Single +5 volt power supply
- TRI-STATE TTL Drive capabilites for bidirectional data bus and control bus.
- Fully programmable serial-interface characteristics
  - 5-, 6-, 7-, or 8-bit characters
  - Even, odd, or no-parity bit generation and detection
  - 1-, 1½-, or 2-stop bit generation
  - Baud rate generation (DC to 56k baud)
- False start bit detection
- Complete status reporting capabilities
- Easily interfaces to most popular microprocessors
- Line break generation and detection
- Internal diagnostic capabilities
  - Loopback controls for communications link fault isolation
  - Break, parity, overrun, framing error simulation
- Fully prioritized interrupt system controls

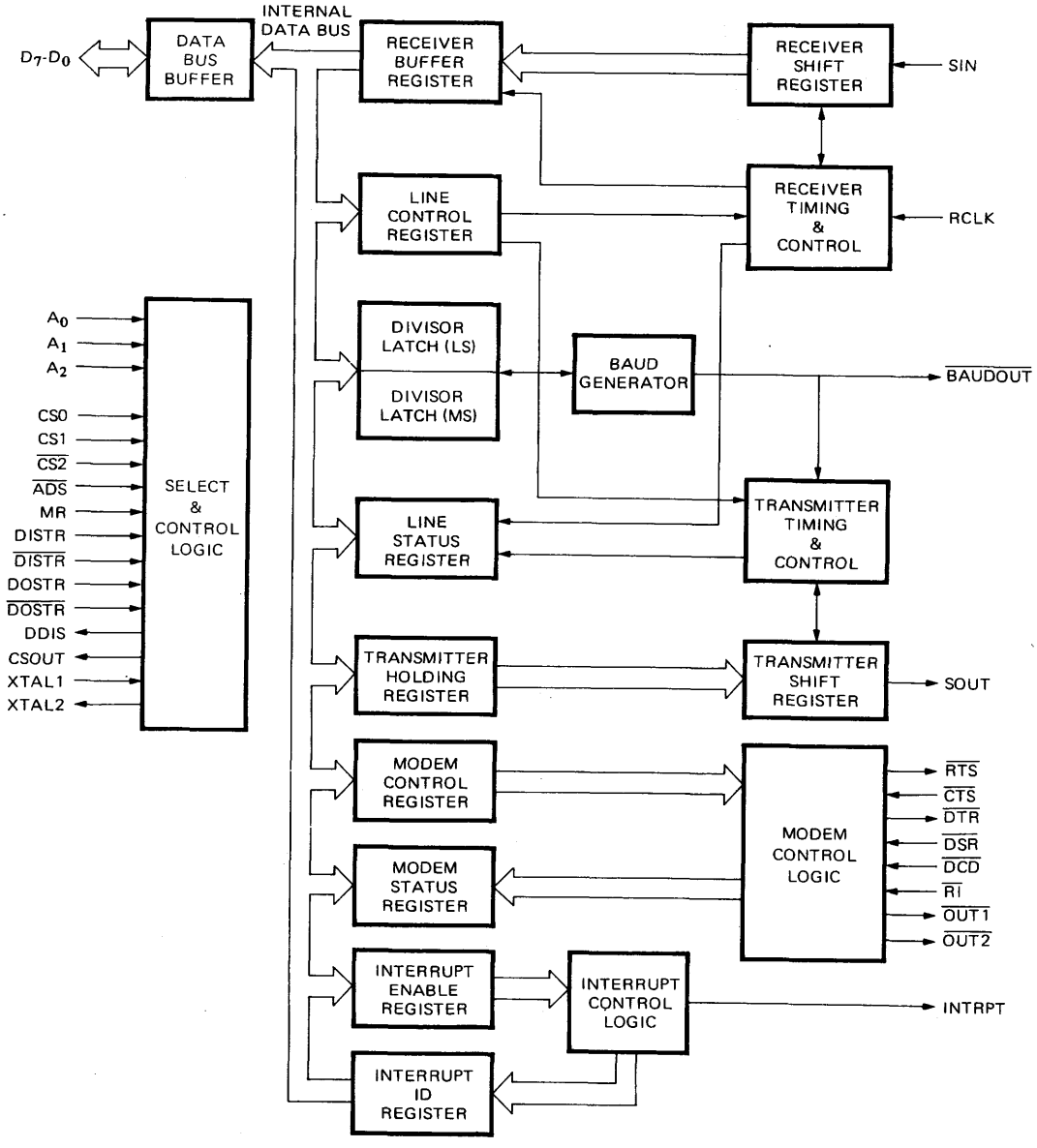
General Description

UM8250A is a programmable Asynchronous Communication Element (ACE) chip fabricated using the Si-Gate NMOS process. It performs serial-to-parallel conversion on data characters received from a peripheral device or a modem, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the ACE at any time during the functional operation. It also includes a programmable baud rate generator that is capable of dividing the timing reference clock input by divisors of 1 to $2^{16}-1$, and producing a 16x clock for driving the internal transmitter logic.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +150°C
All Input or Output Voltages with
Respect to V_{SS} . . . . . −0.5V to +7.0V
Power Dissipation . . . . . 700 mW

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

T_A = 0°C to +70°C, V_{DD} = +5V ± 5%, V_{SS} = 0V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{ILX}	Clock Input Low Voltage		−0.5	0.8	V
V_{IHX}	Clock Input High Voltage		2.0	V_{CC}	V
V_{IL}	Input Low Voltage		−0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA on all*		0.4	V
V_{OH}	Output High Voltage	I_{OL} = −1.0 mA*	2.4		V
I_{CC} (AV)	Avg Power Supply Current (V_{CC})	V_{CC} = 5.25V, T_A = 25°C No Loads on output SIN, DSR, RLSD, CTS, RI = 2.0V All other inputs = 0.8V		95	mA
I_{IL}	Input Leakage	V_{CC} = 5.25V, V_{SS} = 0V All other pins floating. V_{IN} = 0V, 5.25V		±10	μA
I_{CL}	Clock Leakage			±10	μA
I_{OZ}	TRI-STATE Leakage	V_{CC} = 5.25V, V_{SS} = 0V V_{OUT} = 0V, 5.25V 1) Chip deselected 2) WRITE Mode, chip selected		±20	μA
V_{ILMR}	MR Schmitt V_{IL}			0.8	V
V_{IHMR}	MR Schmitt V_{IH}		2.0		V

* Does not apply to XTAL 2

Capacitance

T_A = 25°C, V_{CC} = V_{SS} = 0V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C_{XTAL2}	Clock Input Capacitance	f_C = 1 MHz Unmeasured pins returned to V_{SS}		15	20	pF
C_{XTAL1}	Clock Output Capacitance			20	30	pF
C_{IN}	Input Capacitance			6	10	pF
C_{OUT}	Output Capacitance			10	20	pF

AC Characteristics

T_A = 0°C to b 70°C, V_{DD} = +5V ± 5%

Symbol	Parameter	Conditions	Min.	Max.	Unit
t_{AW}	Address Strobe Width		90	–	ns
t_{AS}	Address Setup Time		90		ns
t_{AH}	Address Hold Time		0		ns
t_{CS}	Chip Select Setup Time		90		ns
t_{CH}	Chip Select Hold Time		0		ns
t_{DIW}	$\overline{DISTR}$/DISTR Strobe Width		175		ns
t_{RC}	Read Cycle Delay		500		ns
RC	Read Cycle = t_{AR}* + t_{DIW} + t_{RC}		755		ns
t_{DD}	$\overline{DISTR}$/DISTR to Driver Disable Delay	@100 pF loading***		75	ns
t_{DDD}	Delay from $\overline{DISTR}$/DISTR to Data	@100 pF loading		175	ns
t_{HZ}	$\overline{DISTR}$/DISTR to Floating Data Delay	@100 pF loading***	30	150	ns
t_{DOW}	$\overline{DOSTR}$/DOSTR Strobe Width		175		ns
t_{WC}	Write Cycle Delay		500		ns
WC	Write Cycle = t_{AW} + t_{DOW} + t_{WC}		755		ns
t_{DS}	Data Setup Time		90		ns
t_{DH}	Data Hold Time		60		ns
t_{CSC}*	Chip Select Output Delay from Select	@100 pF loading		125	ns
t_{RA}*	Address Hold Time from $\overline{DISTR}$/DISTR		20		ns
t_{RCS}*	Chip Select Hold Time from $\overline{DISTR}$/DISTR		20		ns
t_{AR}*	$\overline{DISTR}$/DISTR Delay from Address		80		ns
t_{CSR}*	$\overline{DISTR}$/DISTR Delay from Chip Select		80		ns
t_{WA}*	Address Hold Time from $\overline{DOSTR}$/DOSTR		20		ns
t_{WCS}*	Chip Select Hold Time from $\overline{DOSTR}$/DOSTR		20		ns
t_{AW}*	$\overline{DOSTR}$/DOSTR Delay from Address		80		ns
t_{CSW}*	$\overline{DOSTR}$/DOSTR Delay from Select		80		ns
t_{MRW}	Master Reset Pulse Width		10		ns
t_{XH}	Duration of Clock High Pulse	External Clock (3.1 MHz Max.)	140		μs
t_{XL}	Duration of Clock Low Pulse	External Clock (3.1 MHx Max.)	140		ns
Baud Generator					
N	Baud Divisor		1	$2^{16}-1$	
t_{BLD}	Baud Output Negative Edge Delay	100 pF Load		250	ns
t_{BHD}	Baud Output Positive Edge Delay	100 pF Load		250	ns
t_{LW}	Baud Output Down Time	f_X = 2 MHz, ÷ 2, 100 pF Load	425		ns
t_{HW}	Baud Output Up Time	f_X = 3 MHz, ÷ 3, 100 pF Load	330		ns
Receiver					
t_{SCD}	Delay from RCLK to Sample Time			2	μs
t_{SINT}	Delay from Stop to Set Interrupt		1	1	RCLK** Cycles
t_{RINT}	Delay from $\overline{DISTR}$/DISTR (RD RBR/RDLSR) to Reset Interrupt	100 pF Load		890	ns

*Applicable only when $\overline{ADS}$ is tied low.

**RCLK is equal to t_{XH} and t_{XL}.

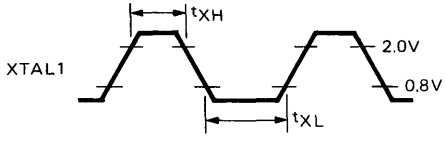
***Charge and discharge time is determined by V_{OL}, V_{OH} and the external loading.

AC Characteristics (Continued)

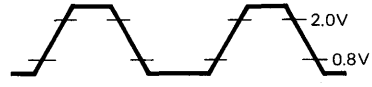
Symbol	Parameter	Conditions	Min.	Max.	Units
Transmitter					
t_{HR}	Delay from $\overline{DOSTR}$/DOSTR (WR THR) to Reset Interrupt	100 pF Load		890	ns
t_{IRS}	Delay from Initial INTR Reset to Transmit Start		8	24	RCLK Cycles
t_{SI}	Delay from Initial Write to Interrupt		16	32	RCLK Cycles
t_{STI}	Delay from Stop to Interrupt (THRE)		8	8	RCLK Cycles
t_{IR}	Delay from $\overline{DISTR}$/DISTR (RD IIR) to Reset Interrupt (THRE)	100 pF Load		890	ns
Modem Control					
t_{MDO}	Delay from $\overline{DOSTR}$/DOSTR (WR MCR) to Output	100 pF Load		1000	ns
t_{SIM}	Delay to Set Interrupt from MODEM Input	100 pF Load		1000	ns
t_{RIM}	Delay to Reset Interrupt from $\overline{DISTR}$/ DISTR (RD MSR)	100 pF Load		1000	ns

Timing Waveforms

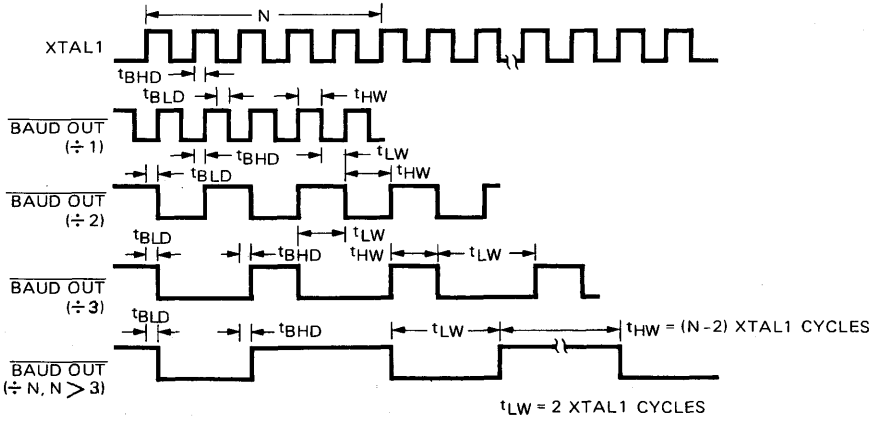
EXTERNAL CLOCK INPUT (3.1 MHz MAX.)



AC TEST POINTS

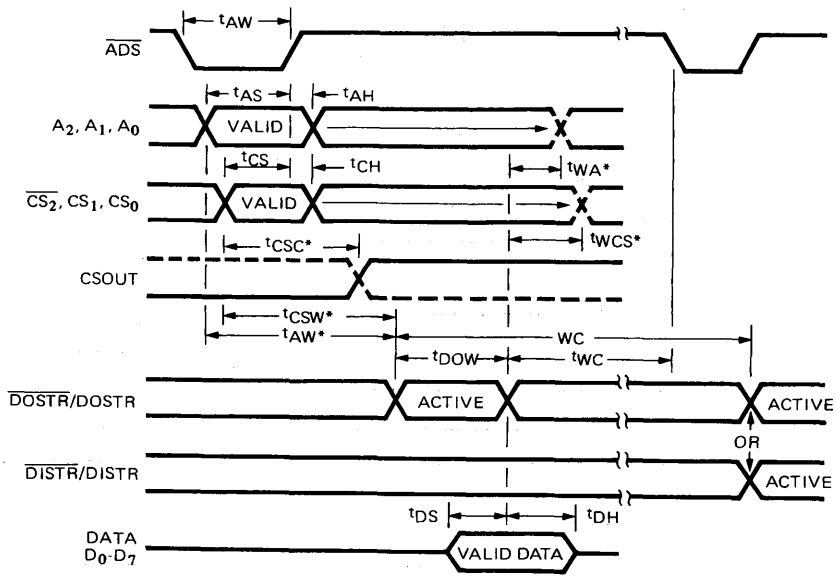


$\overline{BAUDOUT}$ TIMING



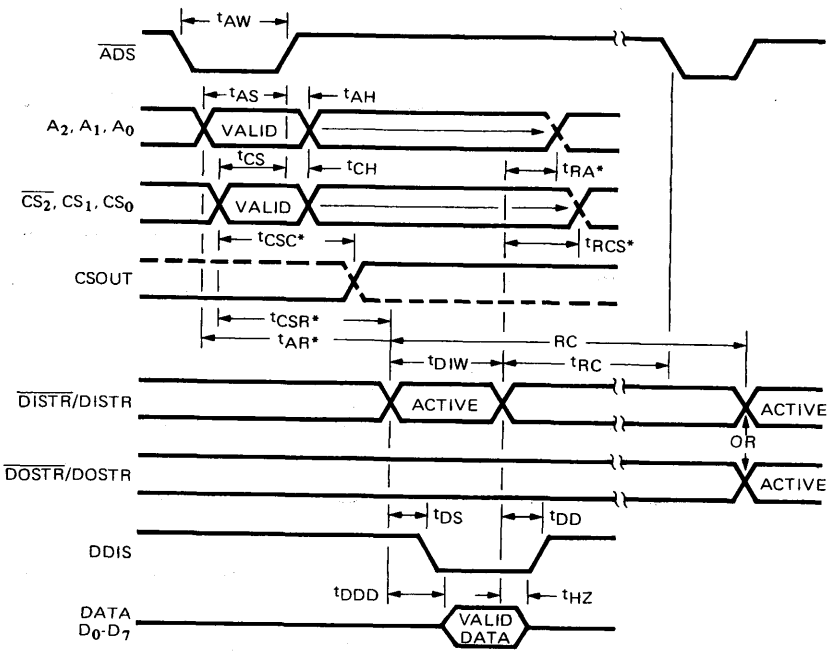
Timing Waveforms (Continued)

WRITE CYCLE



*Applicable Only When $\overline{ADS}$ is Tied Low.

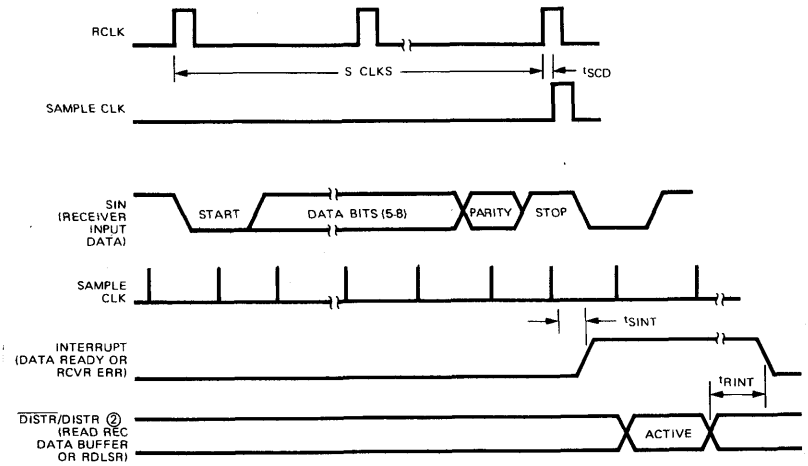
READ CYCLE



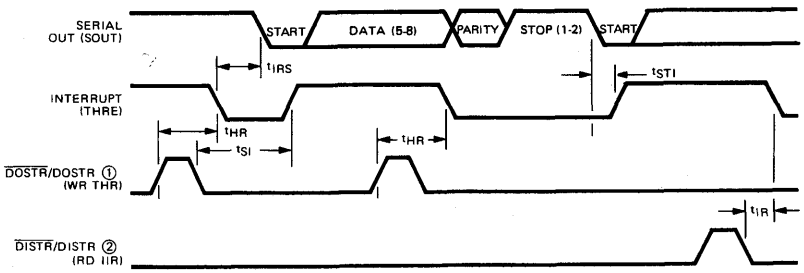
*Applicable Only When $\overline{ADS}$ is Tied Low.

Timing Waveforms (Continued)

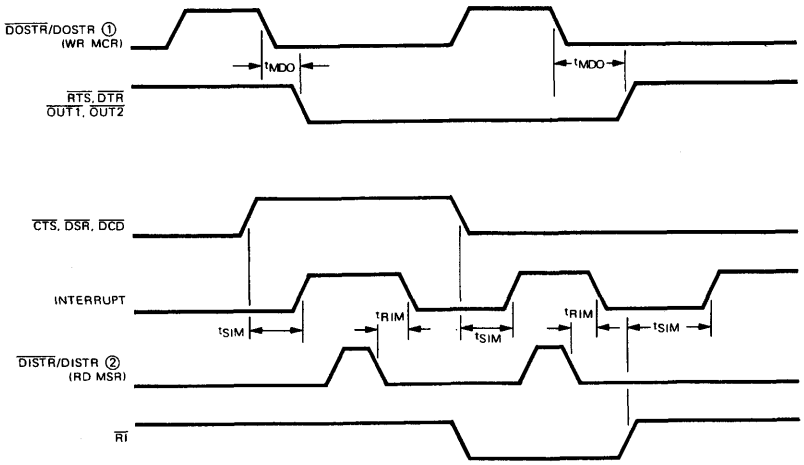
RECEIVER TIMING



TRANSMITTER TIMING



MODEM CONTROL TIMING



Note: 1. See Write Cycle Timing
2. See Read Cycle Timing

Pin Description

Input Signals

Chip Select (CS0, CS1, $\overline{CS2}$), Pins 12–14: When CS0 and CS1 are high and $\overline{CS2}$ is low, the chip is selected. Chip selection is complete when the decoded chip select signal is latched with an active (low) Address Strobe ($\overline{ADS}$) input. This enables communication between the ACE and the CPU.

Data Input Strobe (DISTR, $\overline{DISTR}$), Pins 22 and 21: When DISTR is high or $\overline{DISTR}$ is low while the chip is selected, it allows the CPU to read status information or data from a selected register of the ACE. Only an active DISTR or $\overline{DISTR}$ input is required to transfer data from the ACE during a read operation. Therefore, tie either the DISTR input permanently low or the $\overline{DISTR}$ Input permanently high, if not used.

Data Output Strobe (DOSTR, $\overline{DOSTR}$), Pins 19 and 18: When DOSTR is high or $\overline{DOSTR}$ is low while the chip is selected, allows the CPU to write data or control words into a selected register of the ACE. Only an active DOSTR or $\overline{DOSTR}$ input is required to transfer data to the ACE during a write operation. Therefore, tie either the DOSTR input permanently low or the $\overline{DOSTR}$ input permanently high, if not used.

Address Strobe ($\overline{ADS}$), Pin 25: When low, provides latching for the Register Select (A_2, A_1, A_0) and Chip Select (CS0, CS1, $\overline{CS2}$) signals. An active $\overline{ADS}$ input is required when the Register Select (A_2, A_1, A_0) signals are not stable for the duration of a read or write operation. If not required, tie the $\overline{ADS}$ input permanently low.

Register Select (A_2, A_1, A_0), Pins 26–28: These three inputs are used during a read or write operation to select an ACE register to read from or write into as indicated in Table 1. The DLAB must be set high by the system software to access the Baud Generator Divisor Latches.

Master Reset (MR), Pin 35: This input is buffered with a TTL-compatible Schmitt Trigger with 0.5V typical hysteresis. When high, it clears all the registers (except the Receiver Buffer, Transmitter Holding, and Divisor Latches), and the control logic of the ACE. Also, the state of various output signals (SOUT, INTRPT, $\overline{OUT\ 1}$, $\overline{OUT\ 2}$, $\overline{RTS}$, $\overline{DTR}$) are affected by an active MR input. (Refer to Table 1.)

Receiver Clock (RCLK), Pin 9: This input is the 16 x baud rate clock for the receiver section of the chip.

Serial Input (SIN), Pin 10: Serial data input from the communications link (peripheral device, MODEM, or data set).

Clear to Send ($\overline{CTS}$), Pin 36: The $\overline{CTS}$ signal is a MODEM control function input whose conditions can be tested by the CPU by reading bit 4 (CTS) of the MODEM Status Register. Bit 0 (DCTS) of the MODEM Status Register indicates whether the $\overline{CTS}$ input has changed state since the previous reading of the MODEM Status Register. $\overline{CTS}$ has no effect on the Transmitter. Whenever the CTS bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

DLAB	A_2	A_1	A_0	Register
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	1	Line Control
X	1	0	0	MODEM Control
X	1	0	1	Line Status
X	1	1	0	MODEM Status
X	1	1	1	Scratch
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

Table 1. Register Address

Data Set Ready ($\overline{DSR}$), Pin 37: When low, this indicates that the MODEM or data set is ready to establish the communications link and transfer data with the ACE. The $\overline{DSR}$ signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 5 (DSR) of the MODEM Status Register. Bit 1 (DDSR) of the MODEM Status Register indicates whether the $\overline{DSR}$ input has changed state since the previous reading of the MODEM Status Register. Whenever the DSR bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Data Carrier Detect ($\overline{DCD}$), Pin 38: When low, indicates that the data carrier has been detected by the MODEM or data set. The $\overline{DCD}$ signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 7 (DCD) of the MODEM Status Register. Bit 3 (DDCD) of the MODEM Status Register indicates whether the $\overline{DCD}$ input has changed state since the previous reading of the MODEM Status Register. $\overline{DCD}$ has no effect on the receiver. Whenever the DCD bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Ring Indicator ($\overline{RI}$), Pin 39: When low, indicates that a telephone ringing signal has been received by the MODEM or data set. The $\overline{RI}$ signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 6 (RI) of the MODEM Status Register. Bit 2 (TERI)

of the MODEM Status Register indicates whether the $\overline{RI}$ input has changed from a low to a high state since the previous reading of the MODEM Status Register. Whenever the RI bit of the MODEM Status Register changes from a high to a low state, an interrupt is generated if the MODEM Status Register is enabled.

V_{DD}, Pin 40: +5V supply.

V_{SS}, Pin 20: Ground (0V) reference.

Output Signals

Data Terminal Ready ($\overline{DTR}$), Pin 33: When low, informs the MODEM or data set that the ACE is ready to communicate. The DTR output signal can be set to an active low by programming bit 0 (DTR) of the MODEM Control Register to a high level. The DTR signal is set high upon a Master Reset operation. The DTR signal is forced to its inactive state (high) during loop mode operation.

Request to Send ($\overline{RTS}$), Pin 32: When low, informs the MODEM or data set that the ACE is ready to transmit data. The $\overline{RTS}$ output signal can be set to an active low by programming bit 1 (RTS) of the MODEM Control Register. The $\overline{RTS}$ signal is set high upon a Master Reset operation. The $\overline{RTS}$ signal is forced to its inactive state (high) during loop mode operation.

Output 1 ($\overline{OUT\ 1}$), Pin 34: User-designated output that can be set to an active low by programming bit 2 (OUT 1) of the MODEM Control Register to a high level. The $\overline{OUT\ 1}$ signal is set high upon a Master Reset Operation. The $\overline{OUT\ 1}$ signal is forced to its inactive state (high) during loop mode operation.

Output 2 ($\overline{OUT\ 2}$), Pin 31: User-designated output that can be set to an active low by programming bit 3 (OUT 2) of the MODEM Control Register to a high level. The $\overline{OUT\ 2}$ signal is set high upon a Master Reset Operation. The $\overline{OUT\ 2}$ signal is forced to its inactive state (high) during loop mode operation.

Chip Select Out (CSOUT), Pin 24: When high, indicates that the chip has been selected by active, CS0, CS1, and CS2 inputs. No data transfer can be initiated until the CSOUT signal is a logic 1. CSOUT goes low when chip is deselected.

Driver Disable (DDIS), Pin 23: Goes low whenever the CPU is reading data from the ACE. A high-level DDIS output can be used to disable an external transceiver (if used between the CPU and ACE on the D_7–D_0 Data Bus) at all times, except when the CPU is reading data.

Baud Out ($\overline{BAUDOUT}$), Pin 15: 16 x clock signal for the transmitter section of the ACE. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches. The BAUDOUT may also be used for the receiver section by tying this output to the RCLK input of the chip.

Interrupt (INTRPT), Pin 30: Goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER: Receiver Error Flag; Received Data Available; Transmitter Holding Register Empty; and MODEM Status. The INTRPT signal is reset low upon the appropriate interrupt service or a Master Reset operation.

Serial Output (SOUT), Pin 11: Composite serial data output to the communications link (peripheral, MODEM or data set). The SOUT signal is set to the Marking (logic 1) state upon a Master Reset operation.

Input/Output Signals

Data (D_7–D_0) Bus, Pins 1–8: This bus comprises eight TRI-STATE input/output lines. The bus provides bidirectional communications between the ACE and the CPU. Data, control words, and status information are transferred via the D_7–D_0 Data Bus.

External Clock Inpuy/Output (XTAL 1, XTAL 2), Pins 16 and 17: These two pins connect the main timing reference (crystal or signal clock) to the ACE.

Programmable Registers

The system programmer may access or control any of the ACE registers summarized in Table 2 via the CPU. These registers are used to control ACE operations and to transmit and receive data.

Line Control Register

The system programmer specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format, the programmer may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. The contents of the Line Control Register are indicated in Table 2 and are described below.

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits in each transmitted character. If bit 2 is a logic 0, one Stop bit is generated in the transmitted data. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one and a half Stop bits are generated. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two Stop bits are generated. The Receiver checks the first Stop-bit only, regardless of the number of Stop bits selected.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1s is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bits 3, 4 and 5 are logic 1 the Parity bit is transmitted and checked by the receiver as a logic 0. If bits 3 and 5 are 1 and bit 4 is a logic 0 then the Parity bit is transmitted as a 0.

Bit 6: This bit is the Break Control bit. When it is set to a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state. The break is disabled by setting bit 6 to a logic 0. The Break Control bit acts only on SOUT and has no effect on the transmitter logic.

Note: This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all 0s, pad character, in response to THRE.
2. Set break after the next THRE.
3. Wait for the transmitter to be idle, (TEMT = 1), and clear break when normal transmission has to be restored.

During the break, the Transmitter can be used as a character timer to accurately establish the break duration.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

Table 1. ACE Reset Functions

Register/Signal	Reset Control	Reset State
Interrupt Enable Register	Master Reset	All Bits Low (0 - 3 forced and 4 - 7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High, Bits 1 and 2 Low Bits 3 - 7 are Permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low, Except Bits 5 & 6 are High
MODEM Status Register	Master Reset	Bits 0 - 3 Low Bits 4 - 7 — Input Signal
SOUT	Master Reset	High
INTRPT (RCVR Errs)	Read LSR/MR	Low
INTRPT (RCVR Data Ready)	Read RBR/MR	Low
INTRPT (THRE)	Read IIR/Write THR/MR	Low
INTRPT (Modem Status Changes)	Read MSR/MR	Low
$\overline{\text{OUT 2}}$	Master Reset	High
$\overline{\text{RTS}}$	Master Reset	High
$\overline{\text{DTR}}$	Master Reset	High
$\overline{\text{OUT 1}}$	Master Reset	High

Table 2. Summary of Accessible Registers

Bit No.	Register Address										
	0 DLAB=0	0 DLAB=0	1 DLAB=0	2	3	4	5	6	7	0 DLAB=1	1 DLAB=1
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident. Register (Read Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Register	Divisor Latch (LS)	Divisor Latch (MS)
	RBR	THR	IER	IIR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Data Bit 0*	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	(WL Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OR)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (DESSI)	0	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Data Carrier Detect (DDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

* Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Programmable Baud Generator

The ACE contains a programmable Baud Generator that is capable of taking any clock input (DC to 3.1 MHz) and dividing it by any divisor from 1 to $2^{16}-1$). The output frequency of the Baud Generator is 16 x the Baud [divisor # = (frequency input) ÷ (baud rate x 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to ensure desired operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables 3 and 4 illustrate the use of the Baud Generator with crystal frequencies of 1.8432 MHz and 3.072 MHz respectively. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen. The maximum operating frequency of the Baud Generator is 3.1 MHz. However, when using divisors of 3 and below, the maximum frequency is equal to the divisor in MHz. For example, if the divisor is 1, then the maximum frequency is 1 MHz. In no case should the data rate be greater than 56K Baud.

Line Status Register

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of the Line Status Register are indicated in Table 2 and are described below.

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 is reset to a logic 0 by reading the data in the Receiver Buffer Register.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

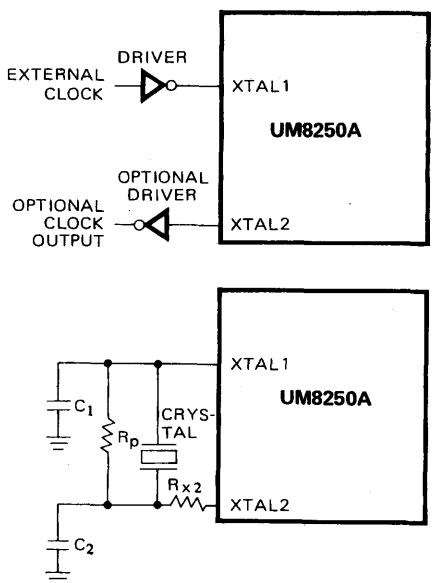
Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level). The FE indicator is reset whenever the CPU reads the contents of the Line Status indicator.

Table 3. Baud Rates Using 1.8432 MHz Crystal

Desired Baud Rate	Divisor Used to Generate 16 x Clock	Percent Error Difference Between Desired and Actual
50	2304	–
75	1536	–
110	1047	0.026
134.5	857	0.058
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.69
2400	48	–
3600	32	–
4800	24	–
7200	16	–
9600	12	–
19200	6	–
38400	3	–
56000	2	2.86

Typical Oscillator Application



Typical Crystal Oscillator Network

Crystal	R_p	R_{x2}	C_1	C_2
3.1 MHz	1 MΩ	1.5K	10-30 pF	40-60 pF
1.8 MHz	1 MΩ	1.5K	10-30 pF	40-60 pF

Table 4. Baud Rates Using 3.072 MHz Crystal

Desired Baud Rate	Divisor Used to Generate 16 x Clock	Percent Error Difference Between Desired and Actual
50	3840	–
75	2560	–
110	1745	0.026
134.5	1428	0.034
150	1280	–
300	640	–
600	320	–
1200	160	–
1800	107	0.312
2000	96	–
2400	80	–
3600	53	0.628
4800	40	–
7200	27	1.23
9600	20	–
19200	10	–
38400	5	–

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits). The BI indicator is reset whenever the CPU reads the contents of the Line Status indicator. Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the ACE is ready to accept a new character for transmission. In addition, this bit causes the ACE to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

Bit 6: This bit is the Transmitter Empty (TEMT) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. It is reset to a logic 0 whenever either the THR or TSR contains a data character.

Table 5. Interrupt Control Functions

Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 2	**Bit 1**	**Bit 0**	**Priority Level**	**Interrupt Type**	**Interrupt Source**	**Interrupt Reset Control**
0	0	1	–	None	None	–
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

Bit 7: This bit is permanently set to logic 0. The Line Status Register is intended for read operations only. Writing to this register is not recommended as this operation is used for factory testing.

Interrupt Identification Register

The ACE has an on-chip interrupt capability that allows for flexibility in interfacing popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the ACE prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and Modem Status (priority 4).

Information indicating that a prioritized interrupt is pending and the type of that interrupt are stored in the Interrupt Identification Register (IIR). When addressed during chip-select time, the IIR freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The contents of the IIR are indicated in Table 2 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table 5.

Bits 3 through 7: These five bits of the IIR are always logic 0.

Interrupt Enable Register

This 8-bit register enables the four types of interrupts of the ACE to separately activate the chip interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are indicated in Table 2 and are described below.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bits 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

MODEM Control Register

This 8-bit register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in Table 2 and are described below.

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1. The DTR output of the ACE may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the Output 1 ($\overline{OUT\ 1}$) signal, which is an auxiliary user-designated output. Bit 2 affects the $\overline{OUT\ 1}$ output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the Output 2 ($\overline{OUT\ 2}$) signal, which is an auxiliary user-designated output. Bit 3 affects the $\overline{OUT\ 2}$ output in a manner identical to that described avove for bit 0.

Bit 4: This bit provides a local loopback feature for diagnotic testing of the ACE. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to the Marking (logic 1) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and RI) are disconnected; and the four MODEM Control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT\ 1}$, and $\overline{OUT\ 2}$) are internally connected to the four MODEM Control inputs, and the MODEM Control output pins are forced to their inactive state (high). In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit-and received-data paths of the ACE.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational, but the interrupts' sources are

now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

Bit 5 through 7: These bits are permanently set to logic 0.

MODEM Status Register

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

Accessible Registers

The contents of the MODEM Status Register are indicated in Table 2 and are described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the Chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from a low to a high state.

Bit 3: This bit is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the $\overline{DCD}$ input to the chip has changed state. Whenever bits 0, 1, 2, or 3 are set to logic 1, a MODEM Status Interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send ($\overline{CTS}$) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.

Bit 5: This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to DTR in the MCR.

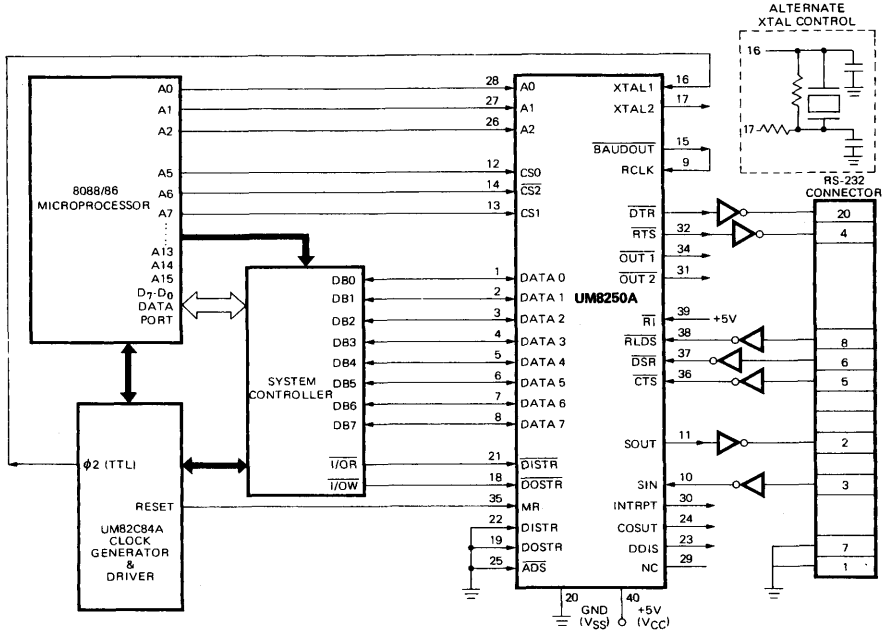
Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 1 in the MCR.

Bit 7: This bit is the complement of the Data Carrier Detect ($\overline{DCD}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 2 of the MCR.

Scratchpad Register

This 8-bit Read/Write Register does not control the ACE in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

Typical Application



UM8250B

Asynchronous Communication Element (ACE)

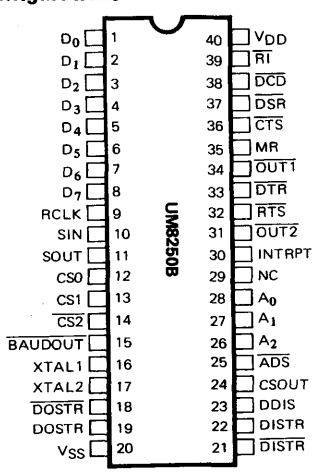
Features

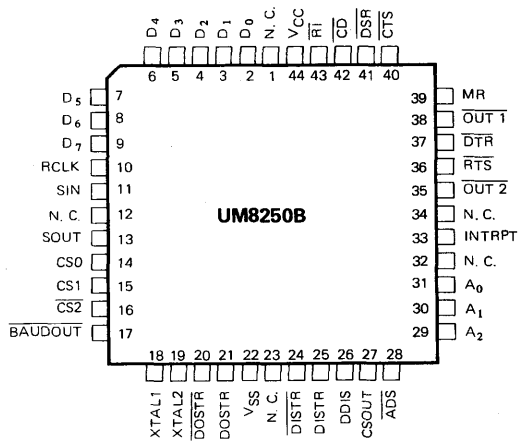
- Adds or deletes standard asynchronous communication bits (start, stop, and parity) to or from a serial data stream
- Full double buffering eliminates the need for precise synchronization
- Independently controlled transmit, receive, line status, and data set interrupts
- Programmable baud rate generator allows division of any input clock by 1 to $(2^{16}-1)$ and generates the internal 16x clock
- Independent receiver clock input
- Modem control functions (CTS, RTS, DSR, DTR, RI, and carrier detect)
- Single +5 volt power supply
- TRI-STATE TTL drive capabilities for bidirectional data bus and controll bus.
- Fully programmable serial-interface characteristics:
  - 5-, 6-, 7-, or 8-bit characters
  - Even, odd, or no-parity bit generation and detection
  - 1, 1½, or 2-stop bit generation
  - Baud rate generation (DC to 56K baud)
- False start bit detection
- Complete status reporting capabilities
- Easily interfaces to most popular microprocessors
- Line break generation and detection
- Internal diagnostic capabilities
  - Loopback controls for communications link fault isolation
  - Break, parity, overrun, framing error simulation
- Fully prioritized interrupt system controls

General Description

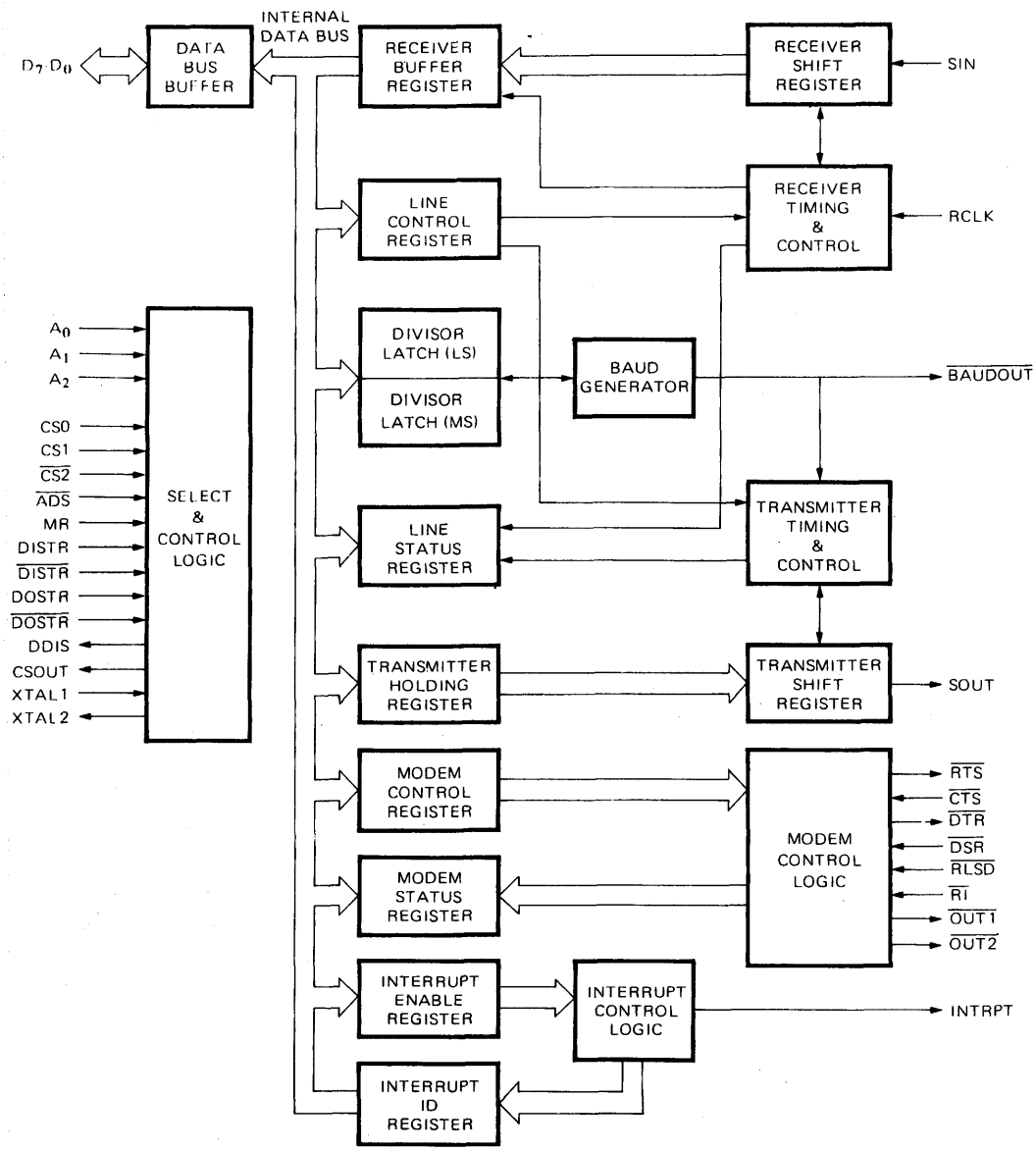
The UM8250B is a programmable Asynchronous Communication Element (ACE) chip fabricated using Si-Gate NMOS process. This product performs serial-to-parallel conversion on data characters received from a peripheral device or a modem, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the ACE at any time during operation. It also includes a programmable baud rate generator that is capable of dividing the timing reference clock input by a divisor of 1 to $(2^{16}-1)$, and producing a 16X clock for driving the internal transmitter logic.

Pin Configurations





Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias . . . . . 0°C to +70°C
Storage Temperature . . . . . –65°C to + 150°C
All input or Output Voltages with
Respect to V_{SS} . . . . . –0.5V to + 7.0V
Power Dissipation 700mW

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

T_A = 0°C to +70°C, V_{CC} = +5V ± 5%, V_{SS} = 0V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{ILX}	Clock Input Low Voltage		–0.5	0.8	V
V_{IHX}	Clock Input High Voltage		2.0	V_{CC}	V
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA on all*		0.4	V
V_{OH}	Output High Voltage	I_{OL} = –1.0 mA*	2.4		V
I_{CC} (AV)	Avg Power Supply Current (V_{CC})	V_{CC} = 5.25V, T_A = 25°C No Loads on output SIN, DSR, RLSD, CTS, RI = 2.0V All other inputs = 0.8V		90	mA
I_{IL}	Input Leakage	V_{CC} = 5.25V, V_{SS} = 0V All other pins floating. V_{IN} = 0V, 5.25V		± 10	µA
I_{CL}	Clock Leakage			± 10	µA
I_{OZ}	TRI-STATE Leakage	V_{CC} = 5.25V, V_{SS} = 0V V_{OUT} = 0V, 5.25V 1) Chip deselected 2) WRITE Mode, chip selected		± 20	µA
V_{ILMR}	MR Schmitt V_{IL}			0.8	V
V_{IHMR}	MR Schmitt V_{IH}		2.0		V

* Does not apply to XTAL2

Capacitance

T_A = 25°C, V_{CC} = V_{SS} = 0V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C_{XTAL2}	Clock Input Capacitance			15	20	pF
C_{XTAL1}	Clock Output Capacitance	f_C = 1 MHz		20	30	pF
C_{IN}	Input Capacitance	Unmeasured pins returned to V_{SS}		6	10	pF
C_{OUT}	Output Capacitance			10	20	pF

AC Characteristics

T_A = 0°C to +70°C, V_{CC} = +5V ± 5%

Symbol	Parameter	Conditions	Min.	Max.	Unit
t_{AW}	Address Strobe Width		90	–	ns
t_{AS}	Address Setup Time		90		ns
t_{AH}	Address Hold Time		0		ns
t_{CS}	Chip Select Setup Time		90		ns
t_{CH}	Chip Select Hold Time		0		ns
t_{DIW}	$\overline{DISTR}$/DISTR Strobe Width		175		ns
t_{RC}	Read Cycle Delay		500		ns
RC	Read Cycle = t_{AR}* + t_{DIW} + t_{RC}		755		ns
t_{DD}	$\overline{DISTR}$/DISTR to Driver Disable Delay	@ 100 pF loading***		125	ns
t_{DDD}	Delay from $\overline{DISTR}$/DISTR to Data	@ 100 pF loading		175	ns
t_{HZ}	$\overline{DISTR}$/DISTR to Floating Data Delay	@ 100 pF loading***		150	ns
t_{DOW}	$\overline{DOSTR}$/DOSTR Strobe Width		175		ns
t_{WC}	Write Cycle Delay		500		ns
WC	Write Cycle = t_{AW} + t_{DOW} + t_{WC}		755		ns
t_{DS}	Data Setup Time		90		ns
t_{DH}	Data Hold Time		60		ns
t_{CSC}*	Chip Select Output Delay from Select	@ 100 pF loading		125	ns
t_{RA}*	Address Hold Time from $\overline{DISTR}$/DISTR		50		ns
t_{RCS}*	Chip Select Hold Time from $\overline{DISTR}$/DISTR		20		ns
t_{AR}*	$\overline{DISTR}$/DISTR Delay from Address		80		ns
t_{CSR}*	$\overline{DISTR}$/DISTR Delay from Chip Select		80		ns
t_{WA}*	Address Hold Time from $\overline{DOSTR}$/DOSTR		50		ns
t_{WCS}*	Chip Select Hold Time from $\overline{DOSTR}$/DOSTR		20		ns
t_{AW}*	$\overline{DOSTR}$/DOSTR Delay from Address		80		ns
t_{CSW}*	$\overline{DOSTR}$/DOSTR Delay from Select		80		ns
t_{MRW}	Master Reset Pulse Width		10		μs
t_{XH}	Duration of Clock High Pulse	External Clock (3.1 MHz Max.)	140		ns
t_{XL}	Duration of Clock Low Pulse	External Clock (3.1 MHx Max.)	140		ns
Baud Generator					
N	Baud Divisor		1	$2^{16}-1$	
t_{BLD}	Baud Output Negative Edge Delay	100 pF Load		250	ns
t_{BHD}	Baud Output Positive Edge Delay	100 pF Load		250	ns
t_{LW}	Baud Output Down Time	100 pF Load	425		ns
t_{HW}	Baud Output Up Time	100 pF Load	330		ns
Receiver					
t_{SCD}	Delay from RCLK to Sample Time			2	μs
t_{SINT}	Delay from Stop to Set Interrupt			1	RCLK** Cycles
t_{RINT}	Delay from $\overline{DISTR}$/DISTR (RD RBR/RDLSR) to Reset Interrupt	100 pF Load		700	ns

AC Characteristics (Continued)

Symbol	Parameter	Conditions	Min.	Max.	Unit
TRANSMITTER					
t_{HR}	Delay from $\overline{DOSTR}$/DOSTR (WR THR) to Reset Interrupt	100 pF Load		700	ns
t_{IRS}	Delay from initial INTR Reset to Transmit Start			16	RCLK Cycles
t_{SI}	Delay from Initial Write to Interrupt			24	RCLK Cycles
t_{SS}	Delay from stop to Next start	100 pF Load		1	μS
t_{STI}	Delay from Stop to Interrupt (THRE)			8	RCLK Cycles
t_{IR}	Delay from $\overline{DISTR}$/DISTR (RD IIR) to Reset Interrupt (THRE)	100 pF Load		700	ns
MODEM CONTROL					
t_{MDO}	Delay from $\overline{DOSTR}$/DOSTR (WR MCR) to Output	100 pF Load		700	ns
t_{SIM}	Delay to Set Interrupt from MODEM Input	100 pF Load		1000	ns
t_{RIM}	Delay to Reset Interrupt from $\overline{DISTR}$/DISTR (RD MSR)	100 pF Load		700	ns

* Applicable only when $\overline{ADS}$ is tied low.

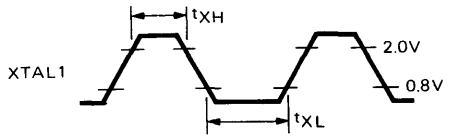
** RCLK is equal to t_{XH} and t_{XL}.

*** Charge and discharge time is determined by V_{OL}, V_{OH} and the external loading.

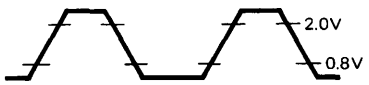
Note: Timings assume one level of multiplexers around the ACE to facilitate testing. Some variation in timings may result from non-typical placement/routing.

Timing Waveforms

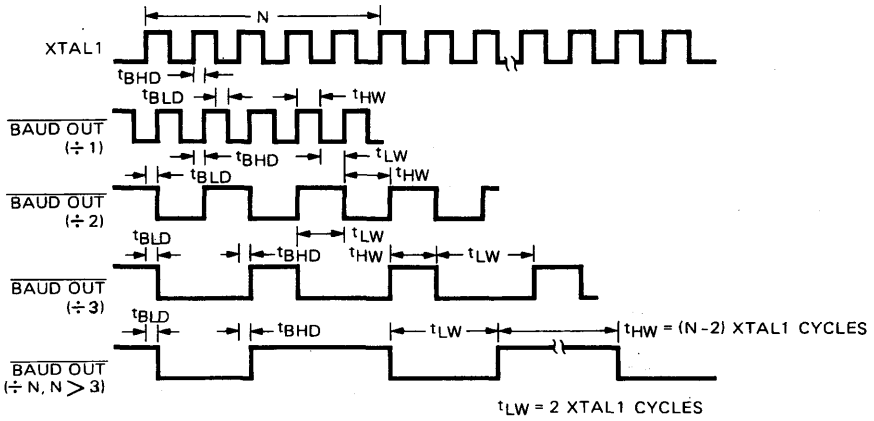
EXTERNAL CLOCK INPUT (3.1 MHz MAX.)



AC TEST POINTS

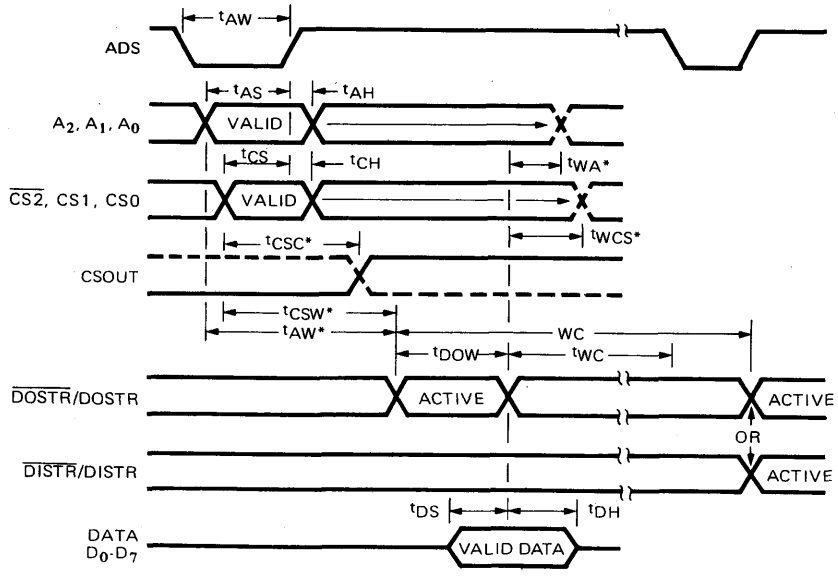


$\overline{BAUDOUT}$ TIMING



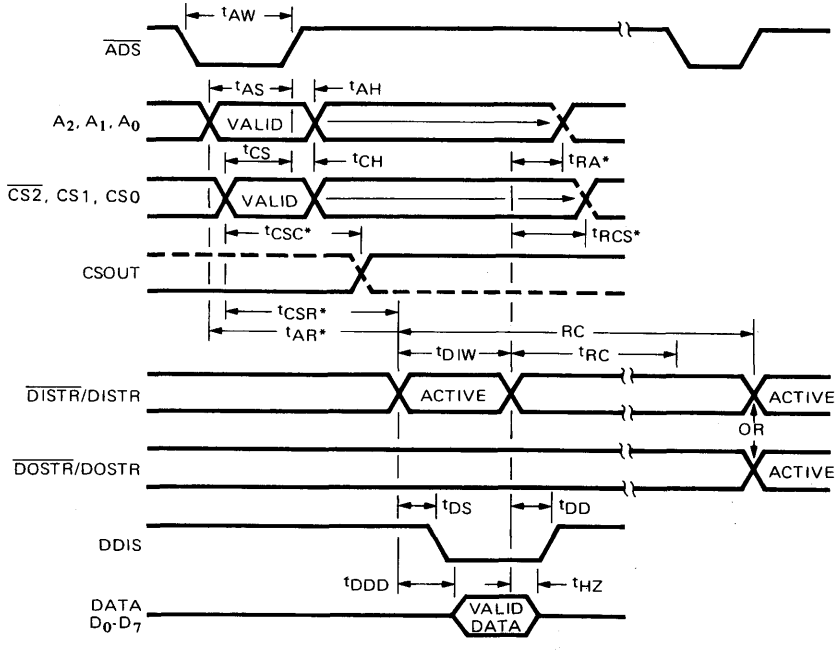
Timing Waveforms (Continued)

WRITE CYCLE



* Applicable Only When $\overline{ADS}$ is Tied Low.

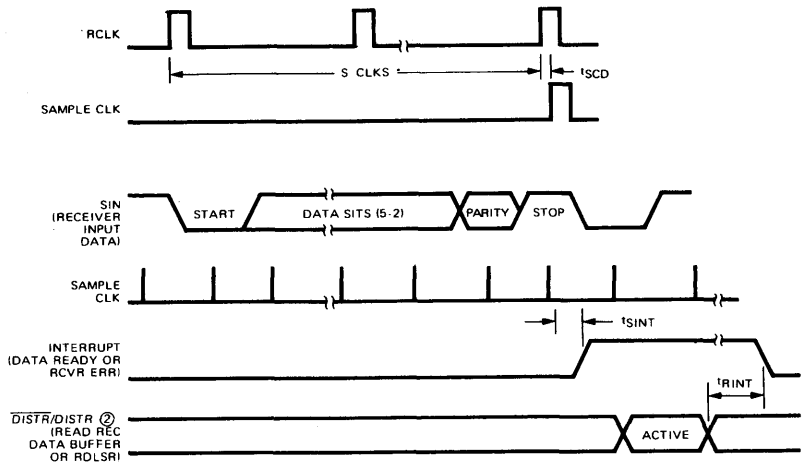
READ CYCLE



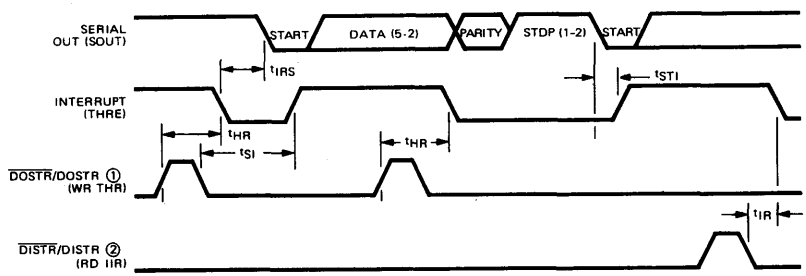
* Applicable Only When $\overline{ADS}$ is Tied Low.

Timing Waveforms (Continued)

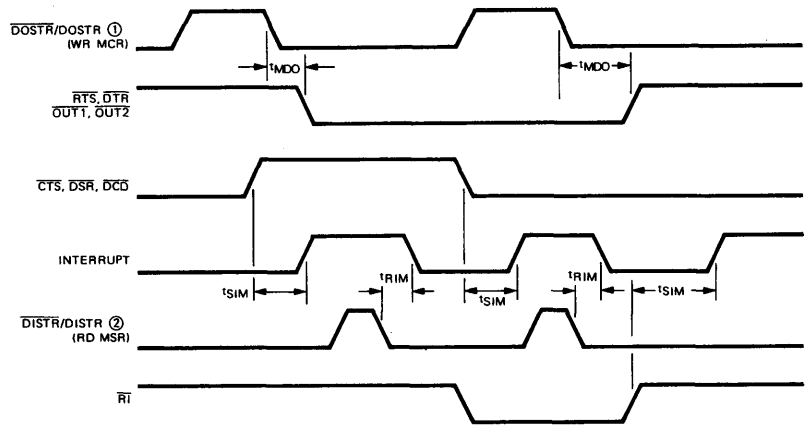
RECEIVER TIMING



TRANSMITTER TIMING

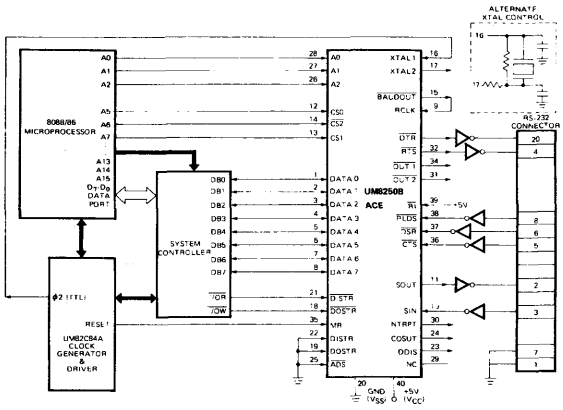


MODEM CONTROL TIMING



1: See Write Cycle Timing
2: See Read Cycle Timing

Typical Application



Pin Description

Input Signal

Chip Select (CS0, CS1, $\overline{CS2}$), Pins 12–14: When CS0 and CS1 are high and $\overline{CS2}$ is low, the chip is selected. Chip selection is complete when the decoded chip select signal is latched with an active (low) Address Strobe ($\overline{ADS}$) input.

Data Input Strobe (DISTR, $\overline{DISTR}$), Pins 21 and 22: When DISTR is high or when $\overline{DISTR}$ is low, the chip is selected; it allows the CPU to read status information or data from a selected register of the UM8250B.

Data Output Strobe (DOSTR, $\overline{DOSTR}$), Pins 18 and 19: The chip is selected when DOSTR is high or $\overline{DOSTR}$ is low and allows the CPU to write data or control words into a selected register of the UM8250B.

* Note that only one of these two inputs, DISTR and $\overline{DISTR}$ (DOSTR and $\overline{DOSTR}$) is needed to activate the CPU read (Write). Tie either DISTR (DOSTR) low or $\overline{DISTR}$ ($\overline{DOSTR}$) high if not needed.

Address Strobe ($\overline{ADS}$), Pin 25: When low, provides latching for the Register Select (A_0, A_1, A_2) and Chip Select (CS0, CS1, $\overline{CS2}$) signals. An active $\overline{ADS}$ input is required when the Register Select (A_0, A_1, A_2) signals are not stable for the duration of a read or write operation. If not required, tie the $\overline{ADS}$ input permanently low.

Register Select (A_0, A_1, A_2), Pins 26–28: These three inputs are used during a read or write operation to select a UM8250B register to read from or write into as indicated in Table 1. Note that the state of the Divisor Latch Access Bit (DLAB), which is the most significant bit of the Line Control Register, affects the selection of certain UM8250B registers. The DLAB must be set high by the system software to access the Baud Generator Divisor Latches.

Receiver Clock (RCLK), Pin 9: This input is the 16X baud rate clock for the receiver section of the chip.

Serial Input (SIN), Pin 10: Serial data input from the communications link (peripheral device, MODEM, or data set).

Clear to Send ($\overline{CTS}$), Pin 36: The $\overline{CTS}$ signal is a MODEM control function input whose conditions can be tested by the CPU by reading bit 4 (CTS) of the MODEM Status Register. Bit 0 (DCTS) of the MODEM Status Register indicates whether the $\overline{CTS}$ input has changed state since the previous reading of the MODEM Status Register. CTS has no effect on the Transmitter. Whenever the CTS bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Data Set Ready ($\overline{DSR}$), Pin 37: When low, this indicates that the MODEM or data set is ready to establish the communications link and transfer data with the ACE. The DSR signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 5 (DSR) of the MODEM Status Register. Bit 1 (DDSR) of the MODEM Status Register indicates whether the $\overline{DSR}$ input has changed state since the previous reading of the MODEM Status Register. Whenever the DSR bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Data Carrier Detect ($\overline{DCD}$) Pin 38: When low, indicates that the data carrier has been detected by MODEM or data set.

The $\overline{DCD}$ Signal is a MODEM Control function input and can be tested by reading bit 7 (DCD) of the MSR. Bit 3 (DDCD) of MSR indicates whether the $\overline{DCD}$ input has changed state since the previous reading of MSR. Whenever the DCD bit of MSR changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Table 1. Register Address

DLAB	A_2	A_1	A_0	Register
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write).
0	0	0	1	Interrupt Enable.
X	0	1	0	Interrupt Identification (read only).
X	0	1	1	Line Control.
X	1	0	0	MODEM Control.
X	1	0	1	Line Status.
X	1	1	0	MODEM Status.
X	1	1	1	None.
1	0	0	0	Divisor Latch (least significant byte).
1	0	0	1	Divisor Latch (most significant byte).

Ring Indicator ($\overline{RI}$), Pin 39: When low, indicates that a telephone ringing signal has been received by the MODEM or data set. The $\overline{RI}$ signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 6 (RI) of the MODEM Status Register. Bit 2 (TERI) of the MODEM Status Register indicates whether the RI input has changed from a low to a high state since the previous reading of the MODEM Status Register. Whenever the $\overline{RI}$ bit of the MODEM Status Register changes from a high to a low state, an interrupt is generated if the MODEM Status Register is enabled.

Master Reset (MR), Pin 35: This input is buffered with a TTL-compatible Schmitt Trigger with 0.5V typical hysteresis. When high, it clears all the registers (except the Receiver Buffer, Transmitter Holding, and Divisor Latches) and the control logic of the UM8250B. Also, the state of various output signals (SOUT, INTRPT, $\overline{OUT\ 1}$, $\overline{OUT\ 2}$, $\overline{RTS}$, $\overline{DTR}$) are affected by an active MR input. (Refer to Table 2).

Table 2. Reset Function

Register/Signal	Reset Control	Reset State
Interrupt Enable Register	Master Reset	All bits Low (0–3 forced and 4–7 permanent).
Interrupt Identification Register	Master Reset	Bit 0 is High, Bits 1 and 2 Low, Bits 3–7 are Permanently Low.
Line Control Register	Master Reset	All Bits Low.
MODEM Control Register	Master Reset	All Bits Low.
Line Status Register	Master Reset	All Bits Low, Except Bits 5 and 6 which are High.
MODEM Status Register	Master Reset	Bits 0–3 Low, Bits 4–7 – Input Signal.
SOUT	Master Reset	High
INTRPT (RCVR Errs)	Read LSR/MR	Low
INTRPT (RCVR Data Ready)	Read RBR/MR	Low
INTRPT (THRE)	Read IIR/Write THR/MR	Low
INTRPT (Modem Status Changes)	Read MSR/MR	Low
OUT 2	Master Reset	High
RTS	Master Reset	High
DTR	Master Reset	High
OUT 1	Master Reset	High

Output Signals

Request to Send ($\overline{RTS}$), Pin 32: When low, it informs the MODEM or data set that the UM8250B is ready to transmit data. The $\overline{RTS}$ output signal can be set to an active low by programming bit 1 (RTS) of the MODEM Control Register. The RTS signal is set high in a Master Reset operation.

Data Terminal Ready ($\overline{DTR}$), Pin 33: When low, it informs the MODEM or data set that the UM8250B is ready to communicate. The DTR output signal can be set to an active low by programming bit 0 (DTR) of the MODEM Control Register to a high level. The DTR signal is set high in a Master Reset operation.

Output 1 ($\overline{OUT\ 1}$), Pin 34: User-designated output can be set to an active low by programming bit 2 ($\overline{OUT\ 1}$) of the MODEM Control Register to a high level. The OUT 1 signal is set high in a Master Reset Operation.

Output 2 ($\overline{OUT\ 2}$), Pin 31: User-designated output can be set to an active low by programming bit 3 ($\overline{OUT\ 2}$) of the MODEM Control Register to a high level. The $\overline{OUT\ 2}$ signal is set high in a Master Reset Operation.

*Note that the $\overline{RTS}$, $\overline{DTR}$, $\overline{OUT\ 1}$ and $\overline{OUT\ 2}$ are forced to inactive state (high) during loop mode operation.

Chip Select Out (CSOUT), Pin 24: When high, it indicates that the chip has been selected by active, CS0, CS1, and $\overline{CS2}$ inputs. No data transfer can be initiated until the CSOUT signal is a logic 1. When chip is not selected, CSOUT remains low.

Driver Disable (DDIS), Pin 23: This pin remains low whenever the CPU is reading data from UM8250B. A high-level output can be used to disable an external transceiver if the CPU is not reading.

Baud Out ($\overline{BAUDOUT}$), Pin 15: 16X clock signal for the transmitter section of the UM8250B. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches.

The $\overline{BAUDOUT}$ may also be used for the receiver section by tying this output to the RCLK input of the chip.

Interrupt (INTRPT), Pin 30: Goes high whenever any of the following interrupt types has an active high condition and is enabled via the IER: Receiver Error Flag; Received Data Available; Transmitter Holding Register Empty and MODEM Status. The INTRPT signal is reset to low at the appropriate interrupt service or in a Master Reset operation.

Serial Output (SOUT), Pin 11: Composite serial data output to the communications link (peripheral, MODEM or data set). The SOUT signal is set to the Marking (logic 1) state in a Master Reset operation.

Input/Output Signals

Data (D_7–D_0) Bus, Pins 1–8: This bus comprises eight TRI-STATE input/output lines. The bus provides bidirectional communications between the UM8250B and the CPU. Data, control words, and status information are transferred via the D_7–D_0 Data Bus.

External Clock Input/Output (XTAL 1, XTAL 2), Pins 16 and 17: These two pins connect the main timing reference (crystal or clock signal) to the UM8250B.

Accessible Registers

There are 10 registers, as shown in Table 3, which may be accessed or controlled by the programmer via the CPU. These registers are used to control operations and to transmit and receive data.

Line Control Register

The system programmer specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format, the programmer may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. The contents of the Line Control Register are indicated in Table 3 and are described below:

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Table 3 Summary of UM8250B Programmable Registers

Bit No.	Register Address									
	0 DLAB=0	0 DLAB=0	1 DLAB=0	2	3	4	5	6	0 DLAB=1	1 DLAB=1
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident. Register (Read Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Divisor Latch (LS)	Divisor Latch (MS)
	RBR	THR	IER	IIR	LCR	MCR	LSR	MSR	DLL	DLM
0	Data Bit 0*	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OR)	Delta Data Set Ready (DDSR)	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	0	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Data Carrier Detect (DDCD)	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register Empty (THRE)	Data Set Ready (DSR)	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Shift Register Empty (TSRE)	Ring Indicator (RI)	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Data Carrier Detect (DCD)	Bit 7	Bit 15

*Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Encoding of bit 0 and bit 1.

Bit 2: This bit specifies the number of Stop bits in each transmitted or received serial character. If bit 2 is a logic 0, 1 Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logic 1 and a 5-bit word length is selected via bits 0 and 1, 1½ Stop bits are generated or checked. If bit 2 is a logic 1 and a 6-, 7-, or 8-bit word length is selected, 2 Stop bits are generated or checked.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are added.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1s are transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the Parity bit is transmitted and then detected by the receiver as a logic 0 if bit 4 is a logic 1 or a logic 1, and if bit 4 is a logic 0.

Bit 6: This bit is the Break Control bit. When bit 6 is a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state and remains there regardless of other transmitter activities. The set break is disabled by setting bit 6 to a logic 0. This feature enables the CPU to alert a terminal in a computer communications system.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

Programmable Baud Rate Generator

The UM8250B contains a programmable Baud Rate Generator that is capable of taking any clock input (DC to 3.1 MHz) and dividing it by any divisor from 1 to $(2^{16}-1)$. The output frequency of the Baud Generator is 16X the Baud rate [divisor #= (frequency input) ÷ (baud rate x 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to ensure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables 4 and 5 illustrate the use of the Baud Generator with crystal frequencies of 1.8432 MHz and 3.072 MHz respectively. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen. The maximum operating frequency of the Baud Generator is 3.1 MHz. However, when using divisors of 3 and below, the maximum frequency is equal to the divisor in MHz. For example, if the divisor is 1, then the maximum frequency is 1 MHz. In no case should the data rate be greater than 56K Baud.

Table 4. Baud Rates Using 1.8432 MHz Crystal

Desired Baud Rate	Divisor Used to Generate 16 x Clock	Percent Error Difference Between Desired and Actual
50	2304	–
70	1536	–
110	1047	0.026
133.5	857	0.0258
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.69
2400	48	–
3600	32	–
4800	24	–
7200	16	–
9600	12	–
19200	6	–
38400	3	–
56000	2	2.86

Note: 1.8432 MHz is the standard 8080 frequency divided by 10.

Table 5. Baud Rates Using 3.072 MHz Crystal

Desired Baud Rate	Divisor Used to Generate 16 x Clock	Percent Error Difference Between Desired and Actual
50	3840	–
75	2560	–
110	1745	0.026
134.5	1428	0.034
150	1280	–
300	640	–
600	320	–
1200	160	–
1800	107	0.312
2000	96	–
2400	80	–
3600	53	0.628
4800	40	–
7200	27	1.23
9600	20	–
19200	10	–
38400	5	–

Fig. 1 and 2 show the typical application circuits of the UM8250's clock generation.

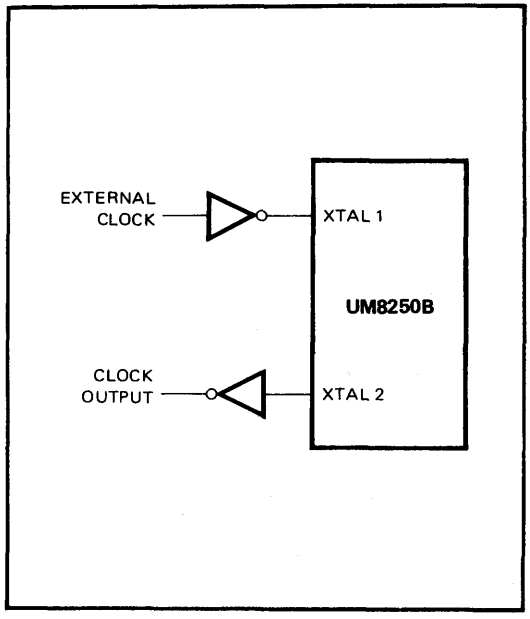
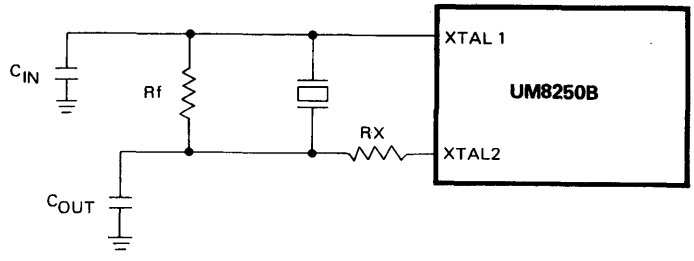


Figure 1. Clock Circuit with External Clock Signal



Component Values:

Crystal Frequency	Rf	Rx	C_{IN}	C_{OUT}
3.1 MHz	1 MΩ	1.5 K	10 ~ 30 pF	40 ~ 60 pF
1.8 MHz	1 MΩ	1.5 K	10 ~ 30 pF	40 ~ 60 pF

Figure 2. Clock Circuit with Crystal Oscillator

Line Status Register

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of the Line Status Register are indicated in Table 3 and are described below.

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 may be reset to a logic 0 either by the CPU reading the data in the Receiver Buffer Register or by writing a logic 0 into it from the CPU.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level).

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits).

*Note: BI and FE are reset whenever the CPU reads the contents of the Line status indicator.

*Note: Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the UM8250B is ready to accept a new character for transmission. In addition, this bit causes the UM8250B to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is concurrently reset to logic 0 with the loading of the Transmitter Holding Register by the CPU.

Bit 6: This bit is the Transmitter Shift Register Empty (TSRE) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Shift Register is idle. It is reset to logic 0 upon transfer of data from the Transmitter Holding Register to the Transmitter Shift Register. Bit 6 is a read-only bit.

Bit 7: This bit is permanently set to logic 0.

Interrupt Identification Register

The UM8250B has an on-chip interrupt capability that allows flexibility in interfacing popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the UM8250B prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3) and Modem Status (priority 4).

Information indicating that a prioritized interrupt is pending and the type of that interrupt is stored in the Interrupt Identification Register (refer to Table 6). The Interrupt Identification Register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The contents of the IIR are indicated in Table 3 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table 6.

Table 6 Interrupt Control Functions

Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 2	**Bit 1**	**Bit 0**	**Priority Level**	**Interrupt Type**	**Interrupt Source**	**Interrupt Reset Control**
0	0	1	—	None	None	—
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Received Line Signal Detect	Reading the MODEM Status Register

Bits 3 through 7: These five bits of the IIR are always set at logic 0.

Interrupt Enable Register

This 8-bit register enables the four types of interrupts of the UM8250B to separately activate the chip interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are indicated in Table 3 and are described below.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always set at logic 0.

MODEM Control Register

This 8-bit register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in Table 3 and are described below.

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to logic 1, the $\overline{DTR}$ output

is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1. The $\overline{DTR}$ output of the UM8250B may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described for bit 0.

Bit 2: This bit controls the Output 1 ($\overline{OUT\ 1}$) signal, which is an auxiliary user-designated output. Bit 2 affects the $\overline{OUT\ 1}$ output in a manner identical to that described for bit 0.

Bit 3: This bit controls the Output 2 ($\overline{OUT\ 2}$) signal, which is an auxiliary user-designated output. Bit 3 affects the $\overline{OUT\ 2}$ output in a manner identical to that described for bit 0.

Bit 4: This bit provides a local loopback feature for diagnostic testing of the UM8250B. When bit 4 is set to logic 1, the following occurs: the transmitter Serial Output (SOUT) is set to the Marking (logic 1) state, the receiver Serial Input (SIN) is disconnected, the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input, the four MODEM Control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$) are disconnected, and the four MODEM Control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT\ 1}$, and $\overline{OUT2}$) are internally connected to the four MODEM Control inputs, and the MODEM Control output pins are forced to their inactive state (high). In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit- and received-data paths of the UM8250B.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational, but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

The UM8250B interrupt system can be tested by writing into the lower six bits of the Line Status Register and the lower four bits of the MODEM Status Register. Setting any of these bits to a logic 1 generates the appropriate interrupt (if enabled). The resetting of these interrupts is the same as in normal UM8250B operation. To return to normal operation, the registers must be reprogrammed for normal operation and then bit 4 of the MODEM control Register must be reset to logic 0.

Bits 5 through 7: These bits are permanently set to logic 0.

MODEM Status Register

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in Table 3 and are described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the Chip has changed states since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from a low state to a high state.

Bit 3: This bit is the Delta Data Carrier Detector (DDCD) indicator. Bit 3 indicates the $\overline{DCD}$ input to the chip has changed states.

*Note that whenever bit 0, 1, 2 or 3 is set at logic 1, a MODEM Status interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send ($\overline{CTS}$) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.

Bit 5: This bit is the complement of the Data Set Ready (DSR) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to DTR in the MCR.

Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 1 in the MCR.

Bit 7: This bit is the complement of the Data Carrier Detect ($\overline{DCD}$) input. If bit 4 of the MCR is set to a 1. This bit is equivalent to OUT 2 of the MCR.

Ordering Information

Part No.	Package
UM8250B	40L DIP
UM8250BL	44L PLCC

PC Mainboard II

Part No.	Description	Page
UM82C206	Integrated Peripheral Controller	6-3
UM82C210 Series	386SX-286 AT Chip Set	6-67
UM82C211	System Controller	6-69
UM882C212	Memory Controller	6-74
UM82C215	Data/Address Buffer	6-85
UM82C230 Series	286 PC/AT Chip Set	6-87
UM82C231	System/Memory Controller	6-90
UM82C232	Data Buffer	6-116
UM82C380 Series	386 PC/AT Chip Set	6-130
UM82C381	System Controller	6-136
UM82C382	Address Buffer	6-146
UM82C383	Data Buffer	6-149
UM82C384	Memory Controller	6-154
UM82C388	INTEL Cache Interface	6-165
UM82C389	AUSTEK Cache Interface	6-177

UMC

UM82C206

INTEGRATED PERIPHERAL CONTROLLER

PRELIMINARY

FEATURES

- Fully compatible with PC/AT architecture
- Fully compatible with 8237 DMA controller, 8259 interrupt controller, 8254 timer/counter, and 146818 real time clock
- Provides 7 DMA channels, 13 interrupt request channels, 2 timer/counter channels, and a real time clock
- Built in 74LS612 memory mapper for DMA page address
- Provides 114 bytes of CMOS RAM memory
- 8 MHz DMA clock with programmable internal divider for 4 MHz operation
- 16M byte DMA address space
- Programmable wait states for the DMA cycle
- Reduced recovery time (120ns) between I/O operations

GENERAL DESCRIPTION

The UM82C206 Integrated Peripheral Controller includes two 8237 DMA controllers, two 8259 interrupt controllers, one 8254 timer/counter, one MC146818 compatible real time clock,an additional 64 bytes CMOS RAM, one 74LS612 memory mapper, and some top level decoder/configuration logic circuits. It is a single chip integration of all main peripheral parts attached to the X bus of PC/AT architecture. While providing full compatibility with PC/AT architecture, the UM82C206 also offers some enhanced features and improved speed performance. These include an additional 64 bytes of user definable CMOS RAM in real time clock and drastically reduced recovery time for the 8237, 8259 and 8254. Programmable wait state option is provided for the DMA cycles and CPU I/O cycles accessing this chip. This chip also provides programmable 8 or 4 MHz DMA clock selection. The UM82C206 is implemented using advanced 1.5u CMOS design technology and is packaged in an 84-pin PLCC.

PIN CONFIGURATION

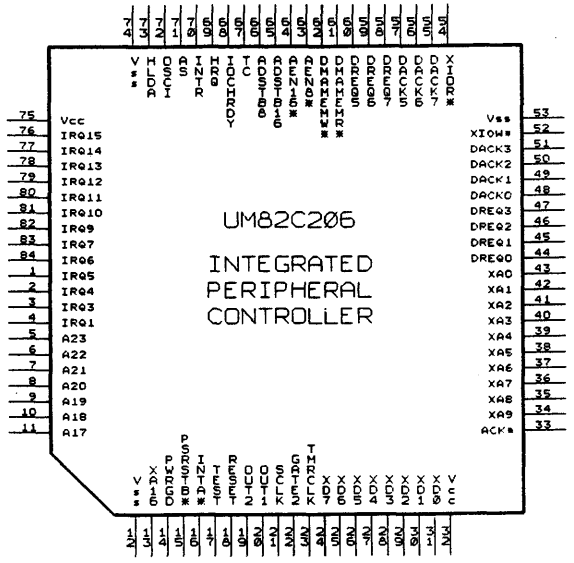


Figure 1. Pin Assignment

BLOCK DIAGRAM

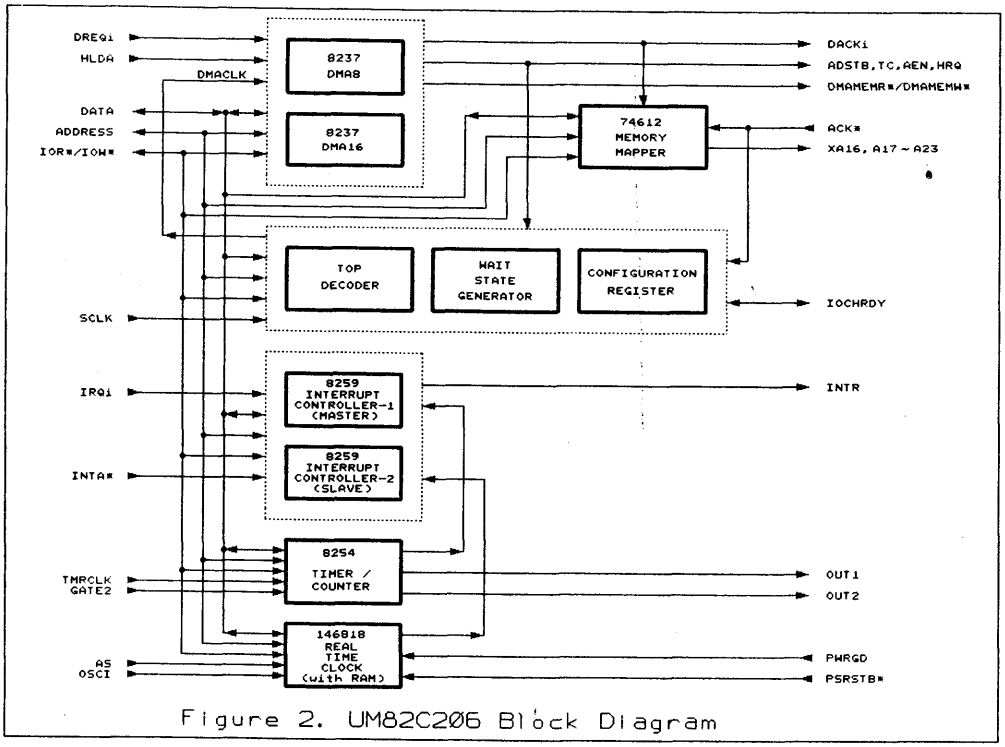


Figure 2. UM82C206 Block Diagram

PIN DESCRIPTION

Pin No.	Symbol	I/O	Description
Clock and Control			
21	SYSCLK	I	CLOCK INPUT is used to generate the timing signals for DMA operation. This pin can be driven to 10 MHz frequency. The internal clock used for DMA operation is either SYSCLK or SYSCLK/2 which is a programmable option.
72	OSCI	I	OSCILLATOR INPUT is used to generate the time base for the time function of real time clock. External square waves of 32.768 KHz may be connected to this pin.
18	RESET	I	RESET is an active high input which affects the following registers: DMA controller: Clears the command, status, request, temporary registers, byte pointer flip flop. Sets the mask register. Following reset, DMA controller is in the idle state. INTERRUPT controller: Clears the edge sense circuit, mask registers, all ICW4 functions. IRQ0 is assigned the highest priority. Slave address is set to 7. Special mask mode is disable and status read is set to IRR.
68	IOCHRDY	I/O	I/O CHANNEL READY is a bidirectional pin. In the input mode, it is used to extend the memory read or write pulses for the DMA controller to access slow memories or I/O devices. It must satisfy setup and hold times with respect to the DMA internal clock in order to work reliably. A low on IOCHRDY causes the internal DMA ready signal to go low asynchronously. When IOCHRDY goes high, one DMA clock cycle will elapse before internal DMA ready signal goes high. In the output mode, it is an open drain output and provides an active low output whenever a UM82C206 internal register is accessed. It will remain low for a pre-programmed number of DMA internal clock cycles (as controlled by bits 7 and 6 of UM82C206 configuration register) and then goes high. In this way, IOCHRDY can insert wait states (as counted by DMA internal clock cycles) when CPU accesses the UM82C206 internal registers. This pin must be pulled up by an external resistor. In a PC/AT architecture based design this pin should be wire-ORed to the PC/AT's IOCHRDY signal.

Pin No.	Symbol	I/O	Description
24-31	XD7-XD0	I/O	X DATA BUS are 3-state bidirectional pins which are connected to the XD bus in PC/AT architecture design. During CPU I/O read cycles, these they are output pins to read out the contents of UM82C206 internal registers. During CPU I/O write cycles, these are input pins to let CPU program the contents of UM82C206 internal registers. During DMA cycles, the most significant 8 bits of the address are ouput onto these pins to be strobed into an external latch by ADSTB8 or ADSTB16. During DMA memory-to-memory transfers, data from the memory comes into the DMA controller via these pins and stores in the internal temporary register during read from the memory partial cycle. In the write to memory partial cycle, the data stored in the temporary register will output via these pins again and write into the new memory location. During the interrupt acknowledge cycle, the interrupt controllers output the interrupt vector byte via these pins. These pins are also used as the multiplexed address/data bus for the real time clock and the CMOS RAM accesses.
35-43 34	XA8-XA0 XA9	I/O I	X ADDRESS BUS are connected to the XA bus in PC/AT architecture design. XA8-XA0 pins are bidirectional pins. XA9 is an input only pin. During CPU I/O accesses to the UM82C206, XA9-XA0 are used to address configuration register and the internal registers of 8237s, 8259s, 8254, MC146818, CMOS RAM, 74LS612. During a CPU cycle, XA3-XA0 pins are used by the CPU to address the registers of the DMA controller corresponding to DMA channels 0-3. XA4-XA1 pins are used by the CPU to address the registers of the DMA controller corresponding to DMA channels 5-7. During a DMA cycle, XA7-XA0 pins are outputs and carry address information for DMA channels 0-3. XA8-XA1 pins are outputs and carry address information for DMA channels 5-7.

Pin No.	Symbol	I/O	Description
54	XIOR*	I/O	X I/O READ is a bidirectional active low 3-state pin. In a non DMA or non interrupt cycle, it is an input control signal used by the CPU to read the UM82C206 internal registers. In an active DMA cycle, it is an output control signal used by the DMA controller to access data from a peripheral during a DMA write memory transfer.
52	XIOW*	I/O	X I/O WRITE is a bidirectional active low 3 state pin. In a non DMA or non interrupt cycle, it is an input control signal used by the CPU to write the UM82C206 internal registers. In an active DMA cycle, it is an output control signal used by the DMA controller to write data to a peripheral during a DMA read memory transfer.
61	DMAMEMR*	O	DMA MEMORY READ is an active low 3-state output pin used to access data from the selected memory location during DMA read memory or memory-to- memory transfer.
62	DMAMEMW*	O	DMA MEMORY WRITE is an active low 3-state output pin used to write data to the selected memory location during DMA write memory or memory-to- memory transfer.
73	HLDA1	I	HOLD ACKNOWLEDGE 1 is an active high signal from the UM82C211C to indicate that the CPU has relinquished control of the system busses.
69	HRQ	O	HOLD REQUEST is an active high output to the UM82C211C to request control of the system bus. When a DREQ occurs and the corresponding mask bit is clear, or a software DMA request is made, the DMA controller issues HRQ to the UM82C211C. After CPU releases the system bus, the UM82C211C then issues a HLDA1 back to the UM82C206 if DMA has been permitted to control the system bus.
44-47 60-58	DREQ0-DREQ3 DREQ5-DREQ7	I	DMA REQUEST is an asynchronous DMA channel request input for each DMA channel. In fixed priority, DREQ0 has the highest priority and DREQ7 has the lowest priority. A peripheral device will activate a DREQ line if it needs a DMA service. DACK will acknowledge the recognition of DREQ request. DREQ must be maintained until the corresponding DACK goes active. DREQ will not be recognized while the DMA clock is stopped. Unused DREQ inputs should be kept inactive and the corresponding mask bit should be set to avoid an undesired DMA function. Polarity of DREQ is programmable. Reset initializes these lines to active high. DREQ0-DREQ3 support 8-bit transfers between 8-bit I/O device and 8 or 16-bit system memory. DREQ5-DREQ7 support 16-bit transfers between 16-bit I/O device and 16-bit system memory. DREQ4 is not externally available and is used to cascade DREQ0-DREQ3.

Pin No.	Symbol	I/O	Description
67	TC	O	TERMINAL COUNT is an active high signal. It indicates the completion of DMA services. A pulse is generated by the DMA controller when terminal count for any channel is reached except for channel 0 in memory-to-memory transfer mode. During memory-to-memory transfer terminal count will be generated when the terminal count for channel 1 occurs. When a TC pulse occurs, the DMA controller will terminate the service, and if auto-initialize is enabled, the base registers will be written to the current registers of that channel. The mask bit and TC bit in the status register will be set for the currently active channel unless the channel is programmed for auto-initialization. In that case, the mask bit remains clear.
48-51 57-55	DACK0- DACK3 DACK5- DACK7	O	DMA ACKNOWLEDGE is used to notify the individual peripherals when one has been granted a DMA cycle. Because these signals are used internally for cascading the DMA channels and for DMA page register selection, they must be programmed to active low and cannot be changed. Reset initializes them to active low.
66	ADSTB8	O	ADDRESS STROBE 8 is an active high output. It is used to latch the upper address byte XA8-XA15 for 8-bit peripheral devices. During DMA block transfers, ADSTB8 will only be issued when the upper address byte must be updated, thus speeding transfer through elimination of S1 states of DMA cycles. ADSTB8 is active for DMA channels 0-3.
65	ADSTB16	O	ADDRESS STROBE 16 is an active high output. It is used to latch the upper address byte XA9-XA16 for 16-bit peripheral devices. During DMA block transfers, ADSTB16 will only be issued when the upper address byte must be updated, thus speeding transfer through elimination of S1 states of DMA cycles. ADSTB16 is active for DMA channels 5-7.
63	AEN8*	O	ADDRESS ENABLE 8 is an active low output. It is used to enable the latch of the upper address byte XA8-XA15 for 8-bit peripheral devices. It is inactive when external bus master controls the system bus. AEN8* is active for DMA channels 0-3.
64	AEN16*	O	ADDRESS ENABLE 16 is an active low output. It is used to enable the latch of the upper address byte XA9-XA16 for 16-bit peripheral devices. It is inactive when external bus master controls the system bus. AEN16* is active for DMA channels 5-7.

Pin No.	Symbol	I/O	Description
33	ACK* (MSE)	I	MODULE SELECT ENABLE is a two purpose input. When high, it enables the chip select function on one of the modules of UM82C206 for the CPU programming functions. When low, the UM82C206 is essentially disconnected from the system bus and is capable of performing an active DMA or an interrupt cycle. In a PC/AT architecture design, it is tied to ACK* signal of main board.
11-5 13	A23-A17 XA16	O	A23-A17 and XA16 are 3-state output pins. A23- A17 are the upper 7 bits of the DMA page register. XA16 is the least significant bit of the DMA page register and is used for DMA transfers for 8-bit peripheral devices only. XA16 is not used for 16-bit DMA transfers as XA16-XA9 being provided by demultiplexing the data bus.
76- 82 83 84 1- 3 4	IRQ15- IRQ9 IRQ7 IRQ6 IRQ5- IRQ3 IRQ1	I	INTERRUPT REQUESTS are asynchronous inputs. When 8259 is operating in edge triggered mode, an interrupt request is executed by raising an IRQ input low to high and holding it high until it is acknowledged by CPU. When 8259 is operating in level triggered mode, an interrupt request is executed by raising an IRQ input high and holding it high until it is ack nowledged by CPU.
16	INTA*	I	INTERRUPT ACKNOWLEDGE is an active low input. It is used to enable the interrupt controllers to output the vector data on to the data bus by an interrupt acknowledge sequence from the CPU.
70	INTR	O	INTERRUPT REQUEST is an active high output pin. It is connected to the CPU's interrupt pin and is used to interrupt the CPU when an interrupt request occurs.
23	TMRCLK	I	TIMER CLOCK is an input clock for 8254 counter 0, counter 1 and counter 2. In PC/AT architecture design, it is approximately 1.19 MHz.
22	GATE2	I	GATE 2 is a gate input for 8254 counter 2. In PC/AT architecture design, the counter 2 is used for tone generation for speaker. It is driven by bit 0 of I/O port 61h.
20	OUT1	O	OUT 1 is an output of 8254 counter 1. In PC/AT architecture design, the counter 1 is programmed as a rate generator to produce a 15 usec period signal for DRAM refresh.
19	OUT2	O	OUT 2 is an output of 8254 counter 2. In PC/AT architecture design, counter 2 is used for tone generation for speaker.

Pin No.	Symbol	I/O	Description
71	AS	I	ADDRESS STROBE is an active high input. It is pulsed by UM82C211C when CPU accesses the real time clock or CMOS RAM of the UM82C206. The falling edge of this pulse latches the address from the XD bus.
15	PSRSTB*	I	POWER SUPPLY STROBE is an active low input. It is used to establish the condition of the control registers of real time clock when power is applied to the device. In PC/AT architecture design, it should be tied to the battery back-up circuit. When PSRSTB* and TEST are both low, the following occurs: (a) Periodic Interrupt Enable (PIE) bit is cleared to zero. (b) Alarm Interrupt Enable (AIE) bit is cleared to zero. (c) Update ended Interrupt Enable (UIE) bit is cleared to zero. (d) Update ended Interrupt Flag (UF) bit is cleared to zero. (e) Interrupt Request status Flag (IRQF) is cleared to zero. (f) Periodic Interrupt Flag (PF) bit is cleared to zero. (g) The part is not accessible. (h) Alarm interrupt Flag (AF) bit is cleared to zero. (i) Square Wave output enable bit is cleared to zero.
14	PWRG	I	POWER GOOD is an active high input and is connected to the power good of the power supply in PC/AT architecture design. It must be high for bus cycles in which the CPU accesses the real time clock. When it is low, all address, data, data strobe and R/W pins are disconnected from the processor.
17	TEST	I	TEST is an active high input to enable the chip testing for production. It should be tied low for normal operation.
32,75	VDD		POWER SUPPLY
12,53, 74	VSS		GROUND

FUNCTIONAL/REGISTER DESCRIPTION

TOP LEVEL DECODER AND CONFIGURATION REGISTER

The UM82C206 top level decoder provides 8 separate enables to various subsystems of the device. Table 1. contains a truth table for the top level decoder. The enabling of the UM82C206 XD0-XD7 output buffers is also controlled by this section. The output buffers are enabled whenever an enable is generated to an internal subsystem and the XIOR* signal is also asserted. The decoder is enabled by signals ACK*, XA9, XA8. To enable any internal subsystem ACK* must be '1' and both XA9 and XA8 must be '0'.

Table 1. UM82C206 Internal Decode

ACK*	XA9	XA8	XA7	XA6	XA5	XA4	XA3	XA2	XA1	XA0	ADDRESS RANGE(HEX)	SELECTED DEVICE
1	0	0	0	0	0	0	X	X	X	X	000-00F	DMA8
1	0	0	0	0	1	0	0	0	0	X	020-021	INTC1
1	0	0	0	0	1	0	0	0	1	X	022-023	CONFIG
1	0	0	0	1	0	0	0	0	X	X	040-043	CTC
1	0	0	0	1	1	1	0	0	0	1	071	RTC
1	0	0	1	0	0	0	X	X	X	X	080-08F	DMAPAGE
1	0	0	1	0	1	0	0	0	0	X	0A0-0A1	INTC2
1	0	0	1	1	0	X	X	X	X	X	0C0-0DF	DMA16
0	X	X	X	X	X	X	X	X	X	X		DISABLED
X	1	X	X	X	X	X	X	X	X	X		DISABLED
X	X	1	X	X	X	X	X	X	X	X		DISABLED

Configuration Register

Index register port : 22H
Data register port : 23H
Index : 01H

Bits	Function
7-6	These bits contain the information of wait states inserted when the CPU accesses the registers of UM82C206. Wait states are counted as SYSCLK clock cycles and are not affected by the DMA clock selection.

7	6	Register I/O R/W wait states
0	0	1
0	1	2
1	0	3
1	1	4 (default)

Bits	Function
5-4	These bits contain the information of wait states inserted in 16 bit DMA cycles. Further control of the DMA cycle length is available through the use of the IOCHRDY pin of the UM82C206. During DMA cycle this pin is used as an input to the wait state generation logic to extend the cycle if necessary.

5	4	16 bit DMA wait states
0	0	1 (default)
0	1	2
1	0	3
1	1	4

Bits	Function
3-2	These bits contain the information of wait states inserted in 8 bit DMA cycles. Further control of the DMA cycle length is available through the use of the IOCHRDY pin of the UM82C206. During DMA cycle this pin is used as an input to the wait state generation logic to extend the cycle if necessary.

3	2	8 bit DMA wait states
0	0	1 (default)
0	1	2
1	0	3
1	1	4

Bits	Function
1	EMR bit enables the early DMAMEMR* function. In IBM PC/AT design DMAMEMR* is delayed one clock cycle later than XMEMR*. If set to 1, it will start DMAMEMR* at the same time as XMEMR*. If set to 0, it will start DMAMEMR* as an IBM PC/AT design (default).
0	CLK bit selects the DMA clock. If this bit set to 0, the SYSCLK input is divided by two and is used to drive both the 8-bit and 16-bit DMA subsystems (default). If this bit is set to 1, the SYSCLK will directly drive the DMA subsystems. Whenever the state of this bit is changed, an internal synchronizer controls the actual switching of the clock to prevent a short clock pulse from causing a DMA malfunction

DMA SUBSYSTEM

The UM82C206 contains two 8237 DMA controllers. Each controller is a four channel DMA device which will generate the memory addresses and control signals necessary to transfer data between a peripheral device and memory directly. The two DMA controllers are internally cascaded to provide four DMA channels for transfers to 8-bit peripherals (DMA8), and three channels for transfers to 16-bit peripherals (DMA16). The channel 0 of DMA16 provides the cascade interconnection of the two DMA devices, thereby maintaining PC/AT compatibility. Hereinafter, the description of the DMA subsystem pertains to both DMA8 and DMA16 unless otherwise noted.

DMA I/O Address Map

The I/O address map of the DMA subsystem of UM82C206 is listed in Table 2. The mapping is fully compatible with PC/AT architecture.

Table 2. DMA Subsystem I/O Address Map

ADDRESS DMA8	ADDRESS DMA16	OPERATION XIOR*	OPERATION XIOW*	BYTE POINTER	REGISTER FUNCTION
000H	0C0H	0	1	0	Read channel 0 current address low byte
		0	1	1	Read channel 0 current address high byte
		1	0	0	Write channel 0 base and current address low byte
		1	0	1	Write channel 0 base and current address high byte
001H	0C2H	0	1	0	Read channel 0 current word count low byte
		0	1	1	Read channel 0 current word count high byte
		1	0	0	Write channel 0 base and current word count low byte
		1	0	1	Write channel 0 base and current word count high byte
002H	0C4H	0	1	0	Read channel 1 current address low byte
		0	1	1	Read channel 1 current address high byte
		1	0	0	Write channel 1 base and current address low byte
		1	0	1	Write channel 1 base and current address high byte
003H	0C6H	0	1	0	Read channel 1 current word count low byte
		0	1	1	Read channel 1 current word count high byte
		1	0	0	Write channel 1 base and current word count low byte
		1	0	1	Write channel 1 base and current word count high byte
004H	0C8H	0	1	0	Read channel 2 current address low byte
		0	1	1	Read channel 2 current address high byte
		1	0	0	Write channel 2 base and current address low byte
		1	0	1	Write channel 2 base and current address high byte
005H	0CAH	0	1	0	Read channel 2 current word count low byte
		0	1	1	Read channel 2 current word count high byte
		1	0	0	Write channel 2 base and current word count low byte
		1	0	1	Write channel 2 base and current word count high byte
006H	0CCH	0	1	0	Read channel 3 current address low byte
		0	1	1	Read channel 3 current address high byte
		1	0	0	Write channel 3 base and current address low byte
		1	0	1	Write channel 3 base and current address high byte

DMA8 DMA16	XIOR* XIOW*	POINTER	FUNCTION
007H 0CEH	0 1	0	Read channel 3 current word count low byte
	0 1	1	Read channel 3 current word count high byte
	1 0	0	Write channel 3 base and current word count low byte
	1 0	1	Write channel 3 base and current word count high byte
008H 0D0H	0 1	X	Read status register
	1 0	X	Write command register
009H 0D2H	0 1	X	Read DMA request register
	1 0	X	Write DMA request register
00AH 0D4H	0 1	X	Read command register
	1 0	X	Write single bit DMA request mask register
00BH 0D6H	0 1	X	Read mode register
	1 0	X	Write mode register
00CH 0D8H	0 1	X	Set byte pointer flip/flop
	1 0	X	Clear byte pointer flip/flop
00DH 0DAH	0 1	X	Read temporary register
	1 0	X	Master clear
00EH 0DCH	0 1	X	Clear mode register counter
	1 0	X	Clear all DMA request mask register bits
00FH 0DEH	0 1	X	Read all DMA request mask register bits
	1 0	X	Write all DMA request mask register bits

DMA Operation

During normal operation of the UM82C206, the DMA subsystem will be in either the idle condition, the program condition or the active condition. When DMA controller is in the idle condition, it only executes the SI idle state cycles. The DMA controller will remain in the idle condition unless it has been initialized to work and one of the DMA request pins has been asserted. In that case, the DMA controller will exit the idle condition and enter the active condition. The DMA controller will also exit the idle condition and enter the program condition when CPU attempts to access its internal registers.

Idle Condition

When no peripherals request service, the DMA subsystem will enter the idle condition and perform only the SI idle states. During this time the UM 82C206 will sample the DREQ input pins every clock cycle to determine if any peripheral is requesting a DMA service. The internal select from the top level decoder and HLDA1 input pin will also sample at the same time to determine if the CPU is attempting to access the internal registers. With either of the above two conditions satisfied, the DMA subsystem will exit the idle condition and enter the program condition or the active condition. Note that the program condition has priority over the active condition since a CPU cycle has already started before DMA has been granted use of the bus.

Program Condition

The DMA subsystem will enter the program condition whenever HLDA1 input pin is inactive and an internal select from top level decoder is active. During this time, the address lines XA0-XA3 become inputs if DMA8 is selected, or XA1-XA4 become inputs if DMA16 is selected. These address inputs are used to decode the DMA controller registers which are to be accessed. The XIOR* and XIOW* are used to select and time the CPU reads or writes. When DMA16 is selected, the XA0 is not used to decode and is ignored. Due to the large number and size of the internal registers of the DMA subsystem, an internal byte pointer flip/flop is used to supplement the addressing of the 16-bit word count and address registers. This byte pointer is used to determine the upper or lower byte of the word count and address registers. This byte pointer flip/flop is cleared by hardware RESET or a master clear command. It may also be set or cleared by the CPU's 'set byte pointer flip/flop' or clear byte pointer flip/flop' commands. There are special commands supported by the DMA subsystem in the program condition. These commands do not use the data bus but are derived from a set of addresses, the internal select and XIOR* or XIOW*. These commands are listed at the end of table 2. Erratic operation of the UM82C206 can occur if a request for service occurs on an unmasked DMA channel which is being programmed. The channel should be masked or the DMA should be disabled to prevent the UM82C206 from attempting to service a peripheral with a channel which is only partially programmed.

Active Condition

The DMA subsystem will enter the active condition whenever a software request occurs or a DMA request occurrs on an unmasked channel which has already been programmed. When a DREQ occurs and the corresponding mask bit is clear, or a software DMA request is made, the DMA subsystem issues HRQ to the UM82C211C. After CPU releases the system bus, the UM82C211C then issues a HLDA1 back to the UM82C206 if DMA has been permitted to control the system bus. After being granted control of the bus, the DMA subsystem will then begin a DMA transfer cycle. Take DMA read cycle as an example. After receiving a DREQ,

the UM82C206 will issue a HRQ to the UM82C211C. Until a HLDA1 is returned, the DMA subsystem will remain in an idle condition. On the next clock cycle the DMA will exit idle and enter S0 state. During S0 the DMA will resolve priority and issue DACK on the highest priority channel which is requesting service. The DMA will then enter S1 state where the multiplexed addresses are output and latched. The DMA will then enter S2 State where the UM82C206 asserts DMAMEMR* command. The DMA will then enter S3 state where the UM82C206 asserts XIOW* command. The DMA will then remain in S3 until the wait state counter has expired and IOCHRDY is high. Note that at least one additional S3 will occur unless compressed timing is programmed. Once a ready condition is detected, the DMA will enter S4 where DMAMEMR* and XIOW* are deasserted. In compressed mode and demand mode, subsequent transfers will begin in S2 unless the intermediate addresses require updating. In these subsequent transfers the lower addresses are changed in S2.

Transfer Modes

There are four transfer modes supported by the DMA. They are single transfer mode, block transfer mode, demand transfer mode and cascade mode. The DMA can be programmed on a channel by channel basis to operate in one of these four modes.

Single Transfer Mode - In this mode the DMA will execute only one cycle at a time. DREQ must be held active until DACK becomes active in order to be recognized. If DREQ is held active throughout the single transfer, the UM82C206 will deassert HRQ and release the bus to the system once the transfer is complete. After HLDA1 has gone inactive the UM82C206 will again assert HRQ and execute another transfer on the same channel unless a request from a higher priority channel has been received. In single transfer mode the CPU is ensured of at least one full machine cycle execution between DMA transfers. Following each transfer the word count register is decreased and the address register is increased or decrased depending on the DEC bit of mode register. When the word count decrements from 0000H to FFFFH the terminal count bit in the status register is set and a pulse is output to TC pin. If the autoinitialization is selected, the channel will reinitialize itself for the next service. Otherwise, the DMA will set the cor_ responding DMA request bit mask and suspend transferring on that channel.

Block Transfer Mode - In this mode the DMA will begin transfers in response to either a DREQ or a software request. If DREQ starts the transfers, it need only be held active until DACK becomes active. The transfers will continue until the word count decrements from 0000H to FFFFH, at which time TC pin is pulsed and the terminal count bit of status register is set. Again, an autoinitialization will occur at the end of the last service if the channel has been programmed to do so.

Demand Transfer Mode - In this mode the DMA will begin transfers in response to the assertion of DREQ and will continue until either terminal count is reached or DREQ becomes inactive. This mode is normally used for peripherals which have limited buffering capacity. The peripheral can initiate a transfer and continue until its buffer capacity is exhausted. The peripheral may then re-establish service by again asserting DREQ. During idle periods between transfers the CPU is released to operate and can monitor the operation by reading intermediate values from the address and word count register. Once DREQ has been deasserted, higher priority channels are allowed to intervene. Reaching terminal count will result in the generation of a pulse on TC pin, the setting of the terminal count bit in the status register and autoinitialization if programmed to do so.

Cascade Mode - This mode is used to interconnect more than one DMA controller, to extend the number of DMA channels while

preserving the priority chain. In cascade mode the master DMA controller does not generate address or control signals. The DREQ and DACK signals of the master are used to interface the HRQ and HLDA1 signals of the slave DMA devices. Once the master has received a HLDA1 from the CPU in response to a DREQ caused by the HRQ from a slave DMA controller, the master DMA controller will ignore all inputs except HLDA1 from the CPU and DREQ on active channel. This prevents conflicts between the DMA devices.

Figure 3. shows the cascade interconnection for two levels of DMA devices. Note that channel 0 of DMA16 is internally connected for cascade mode to DMA8. Additional devices can be cascaded to the available channels in either DMA8 or DMA16 since cascade is not limited to two levels of DMA controllers.

When programming cascaded controllers, begin with the device which is actually generating HRQ to the system (first level device) and then proceed to the second level devices. RESET causes the DACK* outputs to become active low and are placed in the inactive state. To allow the internal cascade between DMA8 and DMA16 to function correctly, the active low state of DACK* should not be modified. The first level device's DMA request mask bits will prevent second level cascaded devices from generating unwanted hold requests during the initialization process.

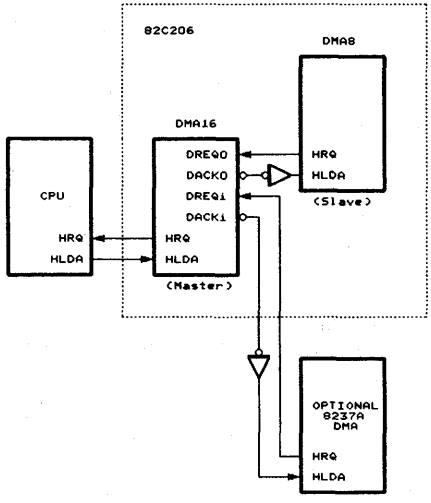


Figure 3. Cascade Mode Interconnect

Transfer Types

Single transfer mode, block transfer mode and demand transfer mode can perform any of the three transfer types. These three transfer types are read , write and verify transfers.

Read Transfers - These transfers move data from memory to an I/O peripheral by generating the memory address and asserting DMAMEMR* and XIOW* during the same transfer cycle.

Write Transfers - These transfers move data from an I/O peripheral to memory by generating the memory address and asserting DMAMEMW* and XIOR* during the same transfer cycle.

Verify Transfers - The verify transfers are pseudo transfers. In this type of transfer the DMA will operate as in read or write transfers by generating HRQ, DACK, memory addresses and respond to the terminal count. But it does not activate the memory and I/O command signals. Since no transfer actually takes place IOCHRDY is also ignored during verify transfers.

Memory-to-Memory Transfers - In addition to the above three transfer types, there is also a memory-to-memory transfer which can only be used on DMA channel 0 and channel 1. The memory-to-memory transfer is used to move a block of memory from one location in memory to another. DMA channels 0 and 1 may be programmed to operate as memory-to-memory channels by setting a bit in the DMA command register. Once programmed to do so the transfer can be started by generating either a software or an external request to channel 0. During the transfer, channel 0 provides the address for the source block during the memory read portion of the transfer, channel 1 generates the address for the destination block during the memory write portion of the same transfer. During the read portion transfer, a byte of data is latched in the internal temporary register of DMA. The contents of this register are then output on the XD0-XD7 output pins during the write portion of the transfer and subsequently written to memory location. Channel 0 may be programmed to maintain the same source address on every transfer. This allows the CPU to initialize large blocks of memory with the same value. The DMA subsystem will continue performing transfers until channel 1 reaches the terminal count.

Autoinitialization

The mode register of each DMA channel contains a bit which will cause the channel to reinitialize after reaching terminal count. During autoinitialization , the base address and base word count registers, which were originally programmed by the CPU, are reloaded into the current address and current word count registers. The base registers remain unchanged during DMA active cycles and can only be changed by the CPU. If the channel has been programmed to autoinitialize, the request mask bit will remain cleared upon reaching terminal count. This allows the DMA to continue operation without CPU intervention. In memory-to-memory transfers the word count registers of both channel 0 and channel 1 must be programmed with the same starting value for full autoinitialization.

DREQ Priority

The UM82C206 supports two types of priority schemes which are software programmable. They are fixed priority and rotating priority. Fixed priority assigns priority based on channel position. In this method channel 0 is assigned the highest priority and channel 3 is the lowest priority. After the recognition of any one channel for service, the other channels are prevented from interfering with that service until it is completed. In rotating priority, the ordering of priority from channel 0 to channel 3 is maintained but the actual assignment of

priority changes. The channel most recently serviced will be assigned the lowest priority and since the order of priority assignment remains fixed, the remaining three channels rotate accordingly. The rotating priority assignment is illustrated in Figure 4. In instances where multiple requests occur at the same time, the UM82C206 will issue a HRQ but will not freeze the priority logic until HLDA1 is returned. Once HLDA1 becomes active the priority logic is frozen and DACK is asserted on the highest requesting channel. Priority will not be reevaluated until HLDA1 has been deactivated.

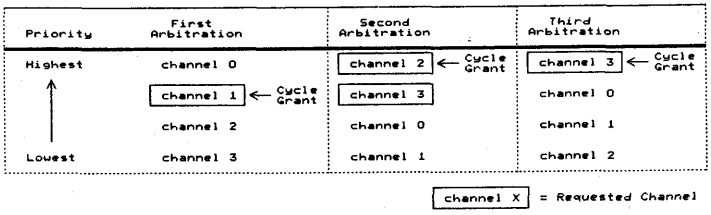


Figure 4. Rotating Priority Scheme

Address Generation

Eight intermediate bits of the address are multiplexed onto the data lines during active cycles of the DMA. This reduces the number of pins required by the DMA subsystem. During S1 state, the intermediate addresses are out- put on data lines XD0-XD7. These addresses should be externally latched and used to drive the system address bus. Since DMA8 is used for 8-bit transfers and DMA16 is used for 16-bit transfers, a 1-bit skew occurs in the intermediate address fields. DMA8 will therefore output addresses A8-A15 on the data bus at this time whereas DMA16 will output A9-A16. A separate set of latch and enable signals are provided for both DMA8 and DMA16 to accommodate the address skew.

During 8-bit DMA transfers, in which DAM8 is active, the UM82C206 will out- put the lower 8-bits of address on XA0-XA7. The intermediate 8-bits of add- ress will be output on XD0-XD7 and ADSTB8 will be asserted for one DMA clock cycle. The falling edge of ADSTB8 is used to latch the intermediate address- es A8-A15. An enable signal, AEN8, issued to control the output drivers of the external latch. A16-A23 are also generated at this time from a DMA page register in the UM82C206. Note that A16 is output on the XA16 pin of the device.

During 16-bit DMA transfers, in which DAM16 is active, the UM82C206 will output the lower 8-bits of address on XA1-XA8. The intermediate 8-bits of address A9-A16 will be output on XD0-XD7 and ADSTB16 will be asserted for one DMA clock cycle. The falling edge of ADSTB16

is used to latch the in- termediate addresses A9-A16. An enable signal, AEN16, issued to control the output drivers of the external latch. A17-A23 are also generated at this time from a DMA page register in the UM82C206. Note that XA0 and XA16 remain 3-state during 16-bit DMA transfers.

The DMA page registers are a set of 16 8-bit registers in the UM82C206 which are used to generate the high order addresses during DMA cycles. Only 8 of the registers are actually used but all 16 were included to maintaim PC/AT compatibility. Each DMA channel has a page register associated with it with the exception of channel 0 of DMA16 which is used for internal cascading to DMA8. Assignment of each of these registers is shown in Table 3. along with its CPU I/O read/write address.

During demand and block transfers, the UM82C206 generates multiple sequen- tial transfers. For most of these transfers the information in the external address latches will remain the same, eliminating the need to be relatched. Since the need to update the latches occurs only when a carry or borrow from the lower 8-bits of the address counter exists, the UM82C206 will only update the latch contents when necessary. The UM82C206 will therefore only execute S1 state when necessary and improve the overall system throughput.

Table 3. DMA Page Register I/O Address Map

I/O ADDRESS	TYPE	REGISTER FUNCTION
080H	R/W	Unused
081H	R/W	DMA8 channel 2 (DACK2)
082H	R/W	DMA8 channel 3 (DACK3)
083H	R/W	DMA8 channel 1 (DACK1)
084H	R/W	Unused
085H	R/W	Unused
086H	R/W	Unused
087H	R/W	DMA8 channel 0 (DACK0)
088H	R/W	Unused
089H	R/W	DMA16 channel 2 (DACK6)
08AH	R/W	DMA16 channel 3 (DACK7)
08BH	R/W	DMA16 channel 1 (DACK5)
08CH	R/W	Unused
08DH	R/W	Unused
08EH	R/W	Unused
08FH	R/W	DRAM refresh cycle

Compressed Timing

The DMA subsystem in the UM82C206 can be programmed to transfer a word in as few as 2 DMA clock cycles. Normal transfers require 4 DMA clock cycles since S3 is executed twice due to the one wait state insertion. In systems capable of supporting higher throughput, the UM82C206 can be programmed to omit one S3 and assert both commands in S2. S2 begins the cycle by generat- ing the address and asserting both commands. One S3 cycle is executed and the cycle terminates in S4. If compressed timing is selected, TC will be output in S2 and S1 cycles will be executed as necessary to update the address latch. Note that compressed timing is not allowed for memory-to- memory transfers.

Register Description

Current Address Register

Each DMA channel has a 16-bit current address register which holds the address used during transfers. Each channel can be programmed to increment or decrement this register whenever a transfer is completed. This register can be read or written by the CPU in consecutive 8-bit bytes. If autoinitialization is selected, this register will be reloaded from the base address register upon reaching terminal count in the current word count register. Channel 0 can be prevented from incrementing or decrementing by setting the address hold bit in the command register.

Current Word Count Register

Each channel has a current word count register which determines the number of transfers. The actual number of transfers performed will be one greater than the value programmed into the register. The register is decremented after each transfer until it goes from zero to FFFFH. When this roll-over occurs the UM82C206 will generate TC and either suspend operation on that channel and set the appropriate request mask bit or autoinitialize and continue.

Base Address Register

Associated with each Current Address Register is a Base Address Register. This is a write only register which is loaded by the CPU when writing to the Current Address Register. The purpose of this register is to store the initial value of the Current Address Register for autoinitialization. The contents of this register are loaded into the Current Address Register whenever terminal count is reached and the Autoinitialize Bit is set.

Base Word Count Register

This register preserves the initial value of the Current Word Count Register. It is also a write only register which is loaded by writing to the Current Word Count Register. This register is loaded into the Current Word Count Register during autoinitialization.

Command Register

This register controls the overall operation of a DMA subsystem. The register can be read or written by the CPU and is cleared by either RESET or a Master Clear command.

Command Register Format (Read/Write)

Bits	Function
7	DAK - Writing a "0" to this bit makes DACK an active low out- pin. Writing a "1" to this bit makes DACK an active high output pin.
6	DRQ - Writing a "0" to this bit makes DREQ an active high input pin. Writing a "1" to this bit makes DREQ an active low input pin.
5	EW - Writing a "1" to this bit enables Extended Write feature. It causes the write command to be asserted one DMA cycle earlier during a transfer. Thus read and write commands both begin in state S2 when enabled.
4	RP - Writing a "1" to this bit selects a Rotating Priority scheme for honoring DMA requests. The default condition is fixed priority.
3	CT - Writing a "1" to this bit enables the Compressed Timing. The default condition causes the DMA to operate with normal timing.
2	CD - Controller Disable. Writing a "1" to this bit disables the DMA subsystem (DMA8 or DMA16). This function is normally used whenever the CPU needs to reprogram one of the channels to prevent DMA cycles from occuring.
1	AH - Writing a "1" to these bit enables the address hold feature in Channel 0 when performing memory-to-memory transfer.
0	M-M - Writing a "1" to this bit enables Channel 0 and Channel 1 to be used for memory-to memory transfers.

Mode Register

Each DMA channel has a Mode Register associated with it. All four Mode Registers reside at the same I/O address. Bits 0 and 1 of the Write Mode Register command determine which channel Mode Register gets written. The remaining six bits control the mode of the selected channel. Each channel Mode Register can be read by sequentially reading the Mode Register location. A Clear Mode register Counter command is provided to allow the CPU to restart the mode read process at a known point. During mode read operations, bit 0 and 1 will both be 1.

Mode Register Format (Read/Write)

<table>
<tr><th>Bits</th><th>Function</th></tr>
<tr><td>7-6</td><td>These bits contain the information of mode selection for each channel :
<table>
<tr><th>7</th><th>6</th><th>Function</th></tr>
<tr><td>M1</td><td>M0</td><td>Mode Select</td></tr>
<tr><td>0</td><td>0</td><td>Demand Mode</td></tr>
<tr><td>0</td><td>1</td><td>Single Cycle Mode</td></tr>
<tr><td>1</td><td>0</td><td>Block Mode</td></tr>
<tr><td>1</td><td>1</td><td>Cascade Mode</td></tr>
</table></td></tr>
<tr><td>5</td><td>DEC - Writing a "1" to this bit DECrements the address after each transfer.</td></tr>
<tr><td>4</td><td>AI - Writing a "1" to this bit enable Auto_Initialization function.</td></tr>
<tr><td>3-2</td><td>These bits control the type of transfer which is to be performed.
<table>
<tr><th>3</th><th>2</th><th>Function</th></tr>
<tr><td>TT1</td><td>TT2</td><td>Transfer Type Select</td></tr>
<tr><td>0</td><td>0</td><td>Verify Transfer</td></tr>
<tr><td>0</td><td>1</td><td>Write Transfer</td></tr>
<tr><td>1</td><td>0</td><td>Read Transfer</td></tr>
<tr><td>1</td><td>1</td><td>Illegal</td></tr>
</table></td></tr>
<tr><td>1-0</td><td>These bits determine which channel's Mode Register will be written. Read back of a mode register will cause these bits to both be "1".
<table>
<tr><th>1</th><th>0</th><th>Function</th></tr>
<tr><td>CS1</td><td>CS0</td><td>Channel Selection</td></tr>
<tr><td>0</td><td>0</td><td>select Channel 0</td></tr>
<tr><td>0</td><td>1</td><td>select Channel 1</td></tr>
<tr><td>1</td><td>0</td><td>select Channel 2</td></tr>
<tr><td>1</td><td>1</td><td>select Channel 3</td></tr>
</table></td></tr>
</table>

Request Register

This is a four bit register used to generate software requests (DMA service can be requested either externally or under software control). Request Register bits can be set or reset independently by the CPU. The Register Mask has no effect on software generated requests. All four bits are read in one operation, and appear in the lower four bits of the byte. Bits 4 through 7 are read as ones . All four request bits are cleared to zero by RESET.

Request Register Write Format

Bits	Function
7-3	Don't care.
2	RB - Writing a "1" to this bit sets the Request Bit.
1-0	RS1-RS0 - Channel Request Select. These bits determine which channel's Request bit will be set.

1	0	Function
RS1	RS0	Channel Selection
0	0	select Channel 0
0	1	select Channel 1
1	0	select Channel 2
1	1	select Channel 3

Request Register Read Format

Bits	Function
7-4	Always reads "1".
3-0	RC3-RC0 - These bits contain the state of the request bit associated with each Request Channel. The bit position corresponds to the channel number.

Request Mask Register

The Request mask register is a set of four bits which are used to inhibit external DMA requests from generating transfer cycles. This register can be programmed in two ways. Each channel can be independently masked by writing to the Write Single Mask Bit location. The data format for this operation is shown below.

Request Mask Register Set/Reset Format

Bits	Function
7-3	Don't care.
2	MB - Writing a "1" to this bit set the request Mask Bit and inhibits external requests.
1-0	MS1-MS0 - Channel request Mask Select. These bits determine which channel's Request Mask bit will be set.

1	0	Function
MS1	MS0	Channel Selection
0	0	select Channel 0
0	1	select Channel 1
1	0	select Channel 2
1	1	select Channel 3

Alternatively all four mask bits can be programmed in one operation by writing to the Write All Mask Bits address. Data format for this and the Read All Mask Bits function is shown below.

Request Mask Register Read/Write Format

Bits	Function
7-4	Always reads "1".
3-0	MB3-MB0 - These bits contain the state of the request Mask Bit associated with each request channel. The bit position corresponds to the channel number.

All four mask bits are set following a RESET or a Master Clear command. Individual channel mask bits will be set as a result of terminal count being reached, if autoinitialize is disabled. The entire register can be cleared, enabling all four channels by performing a Clear Mask Register operation.

Status Register

The status of all four channels can be determined by reading the Status Register. Information is available to determine if a channel has reached Terminal Count and whether an external service request is pending.

Status Register Format (Read)

Bits	Function
7-4	DRQ3-DRQ0 - These bits show the status of each channel request, and are not affected by the state of the Mask Register bits. Reading "1" means "request" occurs, and bits 7,6,5,4 represent channels 3,2,1,0 respectively. These bits can be cleared by RESET, Master Clear or the pending request being deasserted.
3-0	TC3-TC0 - These bits indicate which channel has reached Terminal Count reading "1". These bits can be cleared by RESET, Master Clear or each time a Status Read takes place. The channel number corresponds to the bit position.

Temporary Register

The Temporary Register is used as a temporary holding register for data during memory-to-memory transfers. The register is loaded during the first cycle of a memory-to-memory transfer from XD0-XD7. During the second cycle of the transfer, the data in the Temporary Register is output on the XD0- XD7 pins. Data from the last memory-to-memory transfer will remain in the register.

Special Commands

Five Special Commands are provided to make the task of programming the device easier. These commands are activated as a result of a specific address and assertion of either a XIOR* or XIOW*. For these special commands, the data bus is ignored by the 82C206 whenever an XIOW* activated command is issued. Data returned on XIOR* activated commands is undefined.

1. Clear Byte Pointer Flip-Flop - This command is normally executed prior to reading or writing to the address or word count registers. This initializes the flip-flop to point to the low byte of the register and allows the CPU to read or write the register bytes in correct sequence.

2. Set Byte Pointer Flip-Flop - Setting the Byte Pointer Flip-Flop allows the CPU to adjust the pointer to the high byte of an address or word count register.

3. Master Clear - This command has the same effect as a hardware RESET. The Command Register, Status Register, Request Register, Temporary Register, Mode Register counter and Byte pointer Flip-Flop are cleared and Request Mask Register is set. Immediately following Master Clear or RESET, the DMA will be in the Idle Condition.

4. Clear Request Mask Register - This command enables all four DMA channels to accept requests by clearing the mask bits in the register.

5. Clear Mode Register Counter - In order to allow access to four Mode Registers while only using one address, an internal counter is used. After clearing the counter all four Mode Registers may be read by successive reads to the Mode Register. The order in which the registers will be read is Channel 0 first, Channel 3 last.

INTERRUPT SUBSYSTEM

INTERRUPT CONTROLLLER FUNCTIONAL DESCRIPTION

The programmable interrupt controllers in the UM82C206 function as a system wide interrupt manager in an iPAX86 system. They accept requests from peripherals, resolve priority on pending interrupts and interrupts in service, issue an interrupt request to the CPU, and provide a vector which is used as an index by the CPU to determine which interrupt service routine to execute.

A variety of priority assignment modes are provided, which can be recofigured at any time during system operation, allowing the complete interrupt subsystem to be restructured, based on the system environment.

Overview

Two interrupt controllers, INTC1 and INTC2, are included in the UM82C206. Each of the interrupt controllers is equivalent to an 8259A device operating in iPAX86 Mode. The two devices are interconnected and must be programmed to operate in Cascade Mode (see Figure 5) for proper operation of all 16 interrupt channels. INTC1 is located at addresses 020H-021H and is configured for Master operation (defined below) in Cascade Mode. INTC2 is a Slave device (defined below) and is located at 0A0H-0A1H. The Interrupt Request output signal from INTC2 (INT) is internally connected to the interrupt request input Channel 2 (IR2) of INTC1. The address decoding and Cascade interconnection matches that of the IBM PC/AT.

Two additional interconnections are made to the interrupt request inputs of the interrupt controllers. The output of Timer 0 in the Counter/Timer subsystem is connected to Channel 0 (IR0) of INTC1. Interrupt request from the Real Time Clock is connected to Channel 0 (IR0) of INTC2. Table 4 lists the 16 interrupt channels and their interrupt request source.

Description of the Interrupt Subsystem will pertain to both INTC1 and INTC2 unless otherwise noted. Wherever register addresses are used, the address for the INTC1 register will be listed first and the address for the INTC2 register will follow in parenthesis. Example 02H (0A0H).

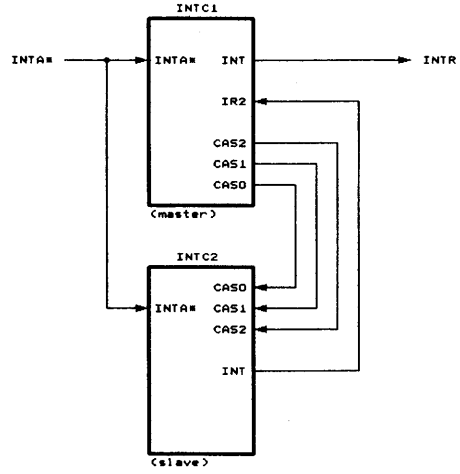


Figure 5. Internal Cascade Interconnect

Table 4. Interrupt Request Source

Controller Number	Channel Name	Interrupt Request Source
INTC1	IR0	Counter/Timer Out0
INTC1	IR1	IRQ1 Input Pin
INTC1	IR2	INTC2 Cascade Interrupt
INTC1	IR3	IRQ3 Input Pin
INTC1	IR4	IRQ4 Input Pin
INTC1	IR5	IRQ5 Input Pin
INTC1	IR6	IRQ6 Input Pin
INTC1	IR7	IRQ7 Input Pin
INTC2	IR0	Real Time Clock IRQ
INTC2	IR1	IRQ9 Input Pin
INTC2	IR2	IRQ10 Input Pin
INTC2	IR3	IRQ11 Input Pin
INTC2	IR4	IRQ12 Input Pin
INTC2	IR5	IRQ13 Input Pin
INTC2	IR6	IRQ14 Input Pin
INTC2	IR7	IRQ15 Input Pin

Controller Operation

Figure 6 is a block diagram of the major elements in the controller. The Interrupt Request Register (IRR) is used to store requests from all of the channels which are requesting service. Interrupt Request Register bits are labeled using the Channel Name IR7-IR0. The In-Service Register (ISR) contains all the channels which are currently being serviced (more than one channel can be in service at a time). In-Service Register bits are labeled IS7-IS0 and correspond to IR7-IR0. The Interrupt Mask Request (IMR)allows the CPU to disable any or all of the interrupt channels. The Priority Resolver evaluates inputs from the above three registers, issues an interrupt request, and latches the corresponding bit into the In-Service Register. During interrupt acknowledge cycles, a master controller outputs a code to the slave device which is compared in the Cascade Buffer/ Comparator with a three bit ID code previously written. if a match occurs in the slave controller, it will generate an interrupt vector. The contents of the Vector Register are used to provide the CPU with an interrupt vector during Interrupt Acknowledge (INTA) cycles.

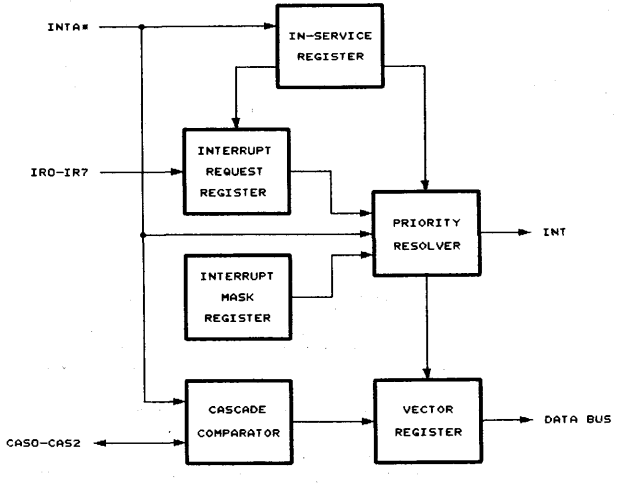


Figure 6. Interrupt Controller Block Diagram

Interrupt Sequence

The UM82C206 allows the CPU to perform an indirect jump to a service routine in response to a request for service from a peripheral device. The indirect jump is based on a vector which is provided by the UM82C206 on the second of two CPU generated INTA cycles (the first INTA cycle is used for resolving priority and the second cycle is for transferring the vector to the CPU , see Figure 7). The events which occur during an interrupt sequence are as follows:

1 - One or more of the interrupt requests (IR7-IR0) becomes active, setting the corresponding IRR bit(s).

2 - The interrupt controller resolves priority based on the state of the IRR, IMR and ISR and asserts the INTR output if appropriate.

3 - The CPU accepts the interrupt and responds with an INTA cycle.

4 - During the first INTA cycle, the highest priority ISR bit is set and the corresponding IRR bit is reset. The internal Cascade address is generated.

5 - The CPU will execute a second INTA cycle, during which the UM82C206 will drive an 8-bit vector onto the data pins XD7-XD0, which is read by the CPU. The format of this vector is shown in Table 5. Note that V7-V3 in Table 5 are programmable by writing to Initialization Control Word 2 (see Initialization Command Words section below).

6 - At the end of the second INTA cycle, the ISR bit will be cleared if the Automatic End Of Interrupt mode is selected (see End Of Interrupt section below). Otherwise, the ISR bit must be cleared by an End Of Interrupt (EOI) command from the CPU at the end of the interrupt service routine to allows further interrupts. If no interrupt request is present at the beginning of the first INTA cycle (i.e. a spurious interrupt), INTC1 will issue an interrupt level 7 vector during the second INTA cycle.

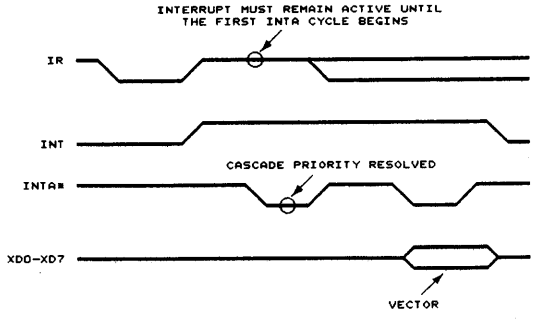


Figure 7. Interrupt Sequence

End Of Interrupt

EOI is defined as the condition which causes an ISR bit to be reset. Determination of which ISR bit is to be reset can be done by a CPU command (specific EOI) or, the Priority Resolver can be instructed to clear the highest priority ISR bit (non-specific EOI). The UM82C206 can determine the correct ISR bit to reset when operated in modes which do not alter the fully nested structure, since the current highest priority ISR bit is necessarily the last level acknowledged and serviced. In conditions where the fully nested structure is not preserved, a specific EOI must be generated at the end of the interrupt service routine. An ISR bit that is masked, in Special Mask Mode by an IMR bit, will not be cleared by a non- specific EOI command. The interrupt controller can optionally generate an Automatic End Of Interrupt (AEOI) on the trailing edge of the second INTA cycle.

Priority Assignment

Assignment of priority is based on an interrupt channel's position relative to the other channels in the interrupt controller. After the initialization sequence, IR0 has the highest priority, IR7 the lowest, and priority assignment is fixed (Fixed Priority Mode). Priority assignment can be rotated either manually (Specific Rotation Mode) or automatically (Automatic Rotation Mode) by programming Operational Command Word 2 (OCW2).

Fixed Priority Mode - This is the default condition which exists unless rotation (either manual or automatic) is enabled, or the controller is programmed for Polled Mode. In Fixed Priority Mode, interrupts are fully nested with priority assigned as shown:

	Lowest							Highest
Priority Status	7	6	5	4	3	2	1	0

Nesting allows interrupts of a higher priority to generate interrupt requests prior to the completion of the interrupt in service. When an interrupt is acknowledged, priority is resolved, the highest priority request's vector is placed on the bus and the ISR bit for that channel is set. This bit remains set until an EOI (automatic or CPU generated) is issued to that channel. While the ISR bit is set, all interrupts of equal or lower priority are inhibited. Note that a higher priority service routine will only be acknowledged if the CPU has internally re-enabled interrupts.

Specific Rotation Mode - Specific Rotatior allows the system software to re-assign priority levels by issuing a command which redefines the highest priority channel.

Before Rotation

	Lowest							Highest
Priority Status	7	6	5	4	3	2	1	0

(SPEcific Rotation command issued with Channel 5 specificed)

After Rotation

	Lowest							Highest
Priority Status	5	4	3	2	1	0	7	6

Automatic Rotation Mode - In applications where a number of equal priority peripherals are requesting interrupts, Automatic Rotation may be used to equalize the priority assignment. In this mode a peripheral, after being serviced, is assigned the lowest priority. All peripherals connected to the controller will be serviced at least once in 8 interrupt requests to the CPU from the controller. Automatic rotation will occur, if enabled, due to the occurrance of EOI (automatic or CPU generated).

Before Rotation (IR3 is highest priority request being serviced)

ISR Status Bit	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
	1	1	0	0	1	0	0	0
	Lowest							Highest
Priority Status	7	6	5	4	3	2	1	0

(SPEcific Rotation command issued with Channel 4 specificed)

After Rotation ISR Status Bit	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
	1	1	0	0	0	0	0	0
	Lowest							Highest
Priority Status	3	2	1	0	7	6	5	4

Programming The Interrupt Controller

Two type of commands are used to control the UM82C206 interrupt controllers, Initialization Command Words (ICWs) and Operational Command Words (OCWs).

Initialization Command Words

The initialization process consists of writing a sequence of 4 bytes to each interrupt controller. The initialization sequence is started by writing the first Initialization Command Word (ICW1) to address 020H (0A0H) with a 1 on bit 4 of the data byte. The interrupt controller interprets this as the start of an initialization sequence and does the following:

1 - The Initialization Command Word Counter is reset to zero.

2 - ICW1 is latched into the device.

3 - Fixed Priority Mode is selected.

4 - IR0 is assigned the highest priority.

5 - The Interrupt Mask Register is cleared.

6 - The Slave Mode Address is set to 7.

7 - Special Mask Mode is disabled.

8 - The IRR is selected for Status Read operations.

The next three I/O writes to address 021H (0A1H) will load ICW2-ICW4. See Figure 8 for a flow chart of the initialization sequence. The initialization sequence can be terminated at any point (all 4 bytes must be written for the controller to be properly initialized) by writing to address 02H(0A0H) with a 0 in data bit 4. Note, this will cause OCW2 or OCW3 to be written.

Table 5. Interrupt Vector Byte

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	V7	V6	V5	V4	V3	1	1	1
IR6	V7	V6	V5	V4	V3	1	1	0
IR5	V7	V6	V5	V4	V3	1	0	1
IR4	V7	V6	V5	V4	V3	1	0	0
IR3	V7	V6	V5	V4	V3	0	1	1
IR2	V7	V6	V5	V4	V3	0	1	0
IR1	V7	V6	V5	V4	V3	0	0	1
IR0	V7	V6	V5	V4	V3	0	0	0

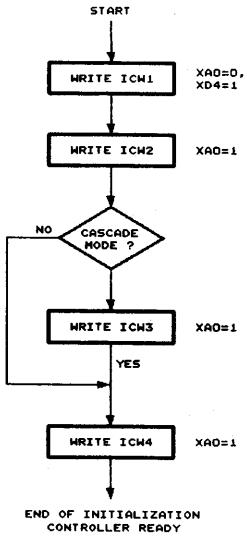


Figure 8. Initialization Sequence

ICW1 - Address 020H (0A0H)
- Write Only

Bits	Function
7-5	Don't care.
4	Must set "1" for ICW1, Since ICW1, OCW2 and OCW3 share the same address,(020H, 0A0H).
3	LTM - Bit 3 selects Level Triggered Mode or Edge triggered Mode input to the IR. If a "1" is written to LTM, a high level on the IR input will generate an interrupt request and the IR must be removed prior to EOI to prevent another interrupt. In Edge Triggered Mode, a low to high transition will generate an interrupt request. In either mode, IR must be held high until the first INTA cycle is started in order to generate the proper vector. IR7 vector will be generated if the IR input is deasserted early.
2	Don't care.
1	SM - This bit selects between Single Mode and Cascade Mode. Single Mode is used whenever only one interrupt controller (INTC1) is used and is not recommended for this device. Cascade Mode allows the two interrupt controllers to be connected through IR2 of INTC1. INTC1 will allow INTC2 to generate its own interrupt vectors if Cascade Mode is selected and the highest priority IR pending is from an INTC2 input. INTC1 and INTC2 must be programmed for Cascade Mode for both devices to operate.
0	Don't care.

ICW2 - Address 021H (0A1H)
- Write Only

Bits	Function
7-3	V7-V3 - These bits are the upper 5 bits of the interrupt vector and are programmable by the CPU. INTC1 and INTC2 need not be programmed with the same value in ICW2, usually INTC1 is programmed with a value of 08H ,and INTC2 is programmed with a value of 70H.
2-0	The lower three bits of the vector are generated by the Priority Resolver during INTA (ses Table 5).

ICW3 - Format for INTC1 - Address 021H
- Write Only

Bits	Function
7-0	S7-S0 - Selects which IR inputs have Slave Mode controllers connected. ICW3 in INTC1 must be written with a 04H(IRQ2) for INTC2 to function correctly.

ICW3-Format for INTC1-Address 0A1H
-Write Only

Bits	Function
7-3	Don't care.
2-0	ID2-ID0 - Determines the Slave Mode address the controller will respond to during the cascade INTA sequence. ICW3 in INTC2 should be written with a 02H(IRQ2 of INTC1) for Cascade Mode operation.

ICW4 - Address 021H (0A1H)
- Write Only

Bits	Function
7-5	Don't care.
4	EMI - this bit will Enable Multiple Interrupts from the same channel in Fixed Priority Mode. This allows INTC2 to fully nest interrupts, when Cascade Mode with Fixed Priority Mode are both selected, without being blocked by INTC1. Correct handling of this mode requires the CPU to issue a non-specific EOI command to zero, when exiting an interrupt service routine. If zero, a non-specific EOI command should be sent to INTC1. If non-zero, no command is issued.
3-2	Don't care.
1	AEOI - Auto End Of Interrupt is enabled when ICW4 is written with a one in bit 1. The interrupt controller will perform a non-specific EOI on the trailing edge of the second INTA cycle. Note, this function should not be used in a device with fully nested interrupts unless the device is a cascade Master.
0	Don't care.

Operational Command Words

Operational Command Words (OCWs) allow the UM82C206 interrupt controllers to be controlled or reconfigured at any time while operating. Each interrupt has 3 OCWs which can be programmed to affect the proper operating configuration and a Status Register to monitor controller operation.

Operational Command Word 1 (OCW1) is located at address 021H (0A1H) and may be written any time the controller is not in Initialization Mode. Operational Command Words 2 and 3 (OCW2, OCW3) are located at address 020H (0A0H). Writing to address 020H (0A0H) with a 0 in bit 4 will place the controller in operational mode and load OCW2 (if data bit 3 = 0) or OCW3 (if data bit 3 = 1).

OCW1 - Address 021H (0A1H)
- Read/Write

OCW2 - Address 020H (0A0H)
- Write Only

Bits	Function
7-5	R,SL,EOI - These bits selects operational function. Writing a "1" in bit 7 causes one of the rotate functions to be selected. Writing a "1" in bit 6 causes a specific or immediate function to occur. All specific commands require L2-L0 to be valid except no operation. Writing a "1" in bit 5 causes a function related to EOI to occur.

7	6	5	Function
R	SL	EOI	operational function
0	0	0	Clear rotate in auto EOI mode
0	0	1	Non-specific EOI Command
0	1	0	No operation
0	1	1	Specific EOI Command *
1	0	0	Set rotate in auto EOI mode
1	0	1	Rotate on non-specific EOI Command
1	1	0	Set priority Command *
1	1	1	Rotate on specific EOI Command *

* L2-L0 are used by these commands.

4-3	These bits must be set "0" to indicate that OCW2 is selected, because ICW1, OCW2 and OCW3 share the same address, (020H, 0A0H).
2-0	L2-L0 - These three bits are internally decoded to select which interrupt channel is to be affected by the Specific command. L2-L0 must be valid during three of the four specific cycles.

OCW3 - Address 020H (0A0H)
- Write Only

Bits	Function
7	This bit must be set "0".
6-5	ESMM - Writing a 1 in this bit position Enables the set/reset Special Mask Mode Function controlled by bit 5 (SMM). ESMM allows the other functions in OCW3 to be accessed and manipulated without affecting the Special Mask Mode state. SMM - During Special Mask Mode, writing a 1 to any bit position of OCW1 inhibits interrupts and a 0 enables interrupts on the associated channel by causing the Priority Resolver to ignore the condition of the ISR.

6	5	Function
ESMM	SMM	Mask mode enable/select
0	X	No operation
1	0	Reset special mask mode to normal mask mode
1	1	Set special mask mode

4-3	These bits must be set "0" to indicate that OCW3 is selected, because ICW1, OCW2 and OCW3 share the same address, (020H, 0A0H).
2	PM - Writing a "1" to this bit of OCW3 enables Polled Mode. Writing OCW3 with poll mode acts like the first INTA cycle, freezing all interrupt request lines and resolving priority. The next read operation to the controller acts like a second INTA cycle and polled vector is output to data bus. The format of polled vector is described later (see Poll Mode Read).
1-0	RR - Writing a "1" to this bit enable the contents of IRR or ISR (determined by RIS) to be placed on XD7-XD0 when reading the Status Port at address 020H (0A0H). Asserting PM forces RR reset.

1	0	Function
RR	RIS	select next read register
0	X	No operation
1	0	Read IRR on next read
1	1	Read ISR on next read

IRR, ISR and Poll Vector

IRR, ISR and Poll Vector share the same address (020H, 0A0H). The selection of the registers depends on the programming of ITC. If the latest OCW3 issued poll command, (PM=1), the poll vector is selected for the next read. Before another poll command is issued, subsequent read to the address will select IRR or ISR depending on the latest OCW3, if RR=1 and RIS=0, ISR is selected. Note that poll command is cleared after the first read to the ITC. After initialization (ICW1 or RESET), IRR is selected.

IRR-Address 020H(0A0H)

Bits	Function
7-0	IR7-IR0 - These bits corresponds to the interrupt request bit of Interrupt Request Register. A "1" on these bits indicate that an interrupt request is pending on the corresponding line.

ISR-Address 020H(0A0H)

Bits	Function
7-0	IS7-IS0 - These bits correspond to the interrupt service bit of Interrupt Service Register. A "1" on these bits indicate that an interrupt is being serviced on the corresponding line. EOI will clear corresponding IS bit of ISR.

Poll Vector-Address 020H(0A0H)

Bits	Function
7	INT - A "1" in these bits indicates that a pending interrupt is polled. If there is no pending interrupt request or the request is removed before the poll command, this bit is 0.
6-3	Don't care.
2-0	V2-V0 - These bits are the binary encoding of the highest priority level pending interrupt request being polled. If no pending interrupt has been polled, all three bits are equal to 1.

Many registers share the same I/O address of INTC. The following table summarizes the address of each register.

WRITE			
A0	XD4	XD3	Register Selected
0	0	0	OCW2
0	0	1	OCW3
0	1	X	ICW1
1	X	X	ICW2,ICW3,ICW4 during initialization sequence
			OCW1 (Mask Register) after initialization sequence

READ	
A0	Register Selected
0	IRR, ISR or Poll Vector
1	OCW1 (Mask Register)

COUNTER/TIMER SUBSYSTEM

COUNTER/TIMER
FUNCTIONAL DESCRIPTION

The UM82C206 contains a 8254 compatible counter/timer(CTC). The counter/ timer can be used to generate accurate time delays under software control. It contains 3 16-bit counters (counters 0-2) which can be programmed to count in binary or binary-coded decimal (BCD). Each counter operates inde- pendently of the other and can be programmed for operation as a timer or a counter.

All counters in this subsystem are controlled by a common control logic as shown in Figure 9. The control logic decodes and generates the necessary commands to load, read, configure and control each counter. Counter 0 and counter 1 can be programmed for all six modes, but mode 1 and mode 5 have limited usefulness because their gate is hardwired to VCC internally. Counter 2 can be programmed to operate in any of the six modes as listed below:

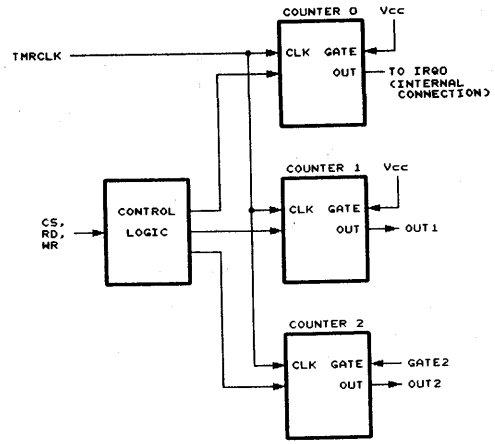


Figure 9. Counter/Timer Block Diagram

Mode 0	Interrupt on terminal count
Mode 1	Hardware retriggerable one-shot
Mode 2	Rate generator
Mode 3	Square wave generator
Mode 4	Software triggered strobe
Mode 5	Hardware retriggerable strobe

All three counters in this subsystem are driven from a common clock input pin (TMRCLK) which is different from other clock inputs to the UM82C206. Counter 0's output (OUT0) is internally connected to IR0 of INTC1 and may be used as an interrupt to the system for time keeping and task switching. Counter 1 may be programmed to generate pulses or square waves for external devices. Counter 2 is a full function counter/timer. It can be used as an interval timer, a counter, or as a gated rate/pulse generator. In PC/AT compatible design, counter 0 is used as a system timer, counter 1 is used as a DRAM refresh rate generator, and counter 2 is used for speaker sound generation.

Counter Description

Each counter in this subsystem contains a control register, a status register, a 16-bit counting element, a pair of 8-bit counter input latchs, and a pair of 8-bit counter output latches. Each counter shares the same clock input (TMRCLK). GATE0, GATE1 and OUT0 are not externally accessible. This is fully compatible with PC/AT. Output of OUT0 is dependent on the counter mode. (see Mode Definitions)

The control register stores the mode and command information used to control the counter. It may be loaded by writing a byte to the write control word at port 043H. The status register allows the software to monitor counter condition and read back the contents of the control register.

The 16-bit counting element is a loadable synchronous down counter. It is loaded or decremented on the falling edge of TMRCLK. The counting element contains a maximum count when a 0 is loaded, which is equivalent to 65536 in binary operation or 10000 in BCD. The counting element does not stop when it reaches 0. In modes 2 and 3 the counting element will be reloaded and in all other modes it will wrap around to 0FFFFH in binary operation or 9999 in BCD.

The counting element is indirectly loaded by writing one or two bytes (optional) to the counter input latches, which are in turn loaded into the counting element. Thus the counting element can be loaded or reloaded in one TMRCLK cycle. The counting element is also read indirectly by reading the contents of the counter output latches. The counter output latches are transparent latches which can be read while transparent or latched (see latch counter command).

Programming The Counter/Timer

After system reset the contents of control registers, counter registers, counting elements, and the output of all counters are undefined. Each counter must be programmed before it can be used. Each counter is programmed by writing its control register with a control word and then giving an initial count to its counting element. Table 6 lists the I/O address map used by the counter/timer subsystem.

Table 6. Counter/Timer I/O Address Map

Address	Function
040H	Counter 0 Read/Write
041H	Counter 1 Read/Write
042H	Counter 2 Read/Write
043H	Control Register Write Only

Read/Write Counter Command

Each counter has a write only control register. This control register is written with a control word to the I/O address 043H. The control word format is described here.

Control Word Format (Write Only)

Bits	Function
7-6	SC1-SC0 - Select which counter this control word is written to.

7	6	
SC1	SC0	Function
0	0	select counter 0
0	1	select counter 1
1	0	select counter 2
1	1	reserved for read-back command

Bits	Function
5-4	RW1-RW0 - Determine the counter read/write word size.

5	4	
RW1	RW0	Function
0	0	reserved for counter latch command
0	1	read/write LSB only
1	0	read/write MSB only
1	1	read/write LSB first, then MSB

MSB = most significant byte
LSB = least significant byte

<table>
<tr><th>Bits</th><th>Function</th></tr>
<tr><td>3-1</td><td>M2-M0 - Select the counter operating mode.
<table>
<tr><td>3</td><td>2</td><td>1</td><td></td></tr>
<tr><td>M2</td><td>M1</td><td>M0</td><td>Function</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>select mode 0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>select mode 1</td></tr>
<tr><td>X</td><td>1</td><td>0</td><td>select mode 2</td></tr>
<tr><td>X</td><td>1</td><td>1</td><td>select mode 3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>select mode 4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>select mode 5</td></tr>
</table></td></tr>
<tr><td>0</td><td>BCD - During read/write counter commands control word writing, a "1" selects binary coded decimal counting format. A "0" selects binary counting format. During read-back command word writing, this bit must be 0.</td></tr>
</table>

When programming to a counter, the below sequences must be followed: First, each counter's control register must be written with a control word before the initial count is written. Second, writing the initial count must follow the format specified in the control word (least significant byte only, most significant byte only, or least significant byte and then most significant byte). A new initial count can be written into the counter at any time after programming without rewriting the control word.

Counter Latch Command

When a counter latch command is issued, the counter's output latches latch the current state of the counting element. The counter's output latches remain latched until read by the CPU or the counter is reprogrammed. After that the output latches then return to a "transparent" condition. Counter latch commands may be issued to more than one counter before reading the first counter to which this commannd was issued. Also, multiple counter latch commands issued to the same counter without reading the counter will cause all but the first command to be ignored. Below describes the counter latch command format.

Counter Latch Command Format (Write Only)

Bits	Function
7-6	SC1-SC0 - Select which counter is being latched.

7	6	
SC1	SC0	Function
0	0	select counter 0
0	1	select counter 1
1	0	select counter 2
1	1	reserved for read-back command

5-4	These two bits must be zero for the counter latch command.
3-0	These four bits are don't care bits.

Read-Back Command

The read-back command allows the user to check the count value, mode, and state of the OUT signal and null count flag of the selected counter(s). The format of the read-back command is described below.

Read-Back Command Format (Write Only)

Bits	Function
7-6	These two bits must be "1" for the read-back command.
5	LCOUNT - A "0" in this bit will latch the count of the counting element of the selected counter(s).
4	LSTATUS - A "0" in this bit will latch the status information of the selected counter(s).
3-1	C2-0 - These three bits select which counter(s) the read-back command is applied to.

3	2	1	
C2	C1	C0	Function
0	X	X	select counter 2
X	0	X	select counter 1
X	X	0	select counter 0

Each counter's latches remain latched until either the latch is read or the counter is reprogrammed. If both LSTATUS and LCOUNT are "0", status will be returned on the next read from the counter. The next one or two reads (depending on whether the counter is programmed to transfer one or two bytes) from the counter result in the count being returned. Multiple read-back commands issued to the same counter without reading the counter will cause all but the first command to be ignored. The status read from each counter is described below.

Status Format

Bits	Function
7	OUT - This contains the state of the OUT signal of the counter.
6	NC - This contains the condition of the null count flag. This flag is used to indicate that the contents of the counting element are valid. It will be set to a "1" during a write to the control register or the counter. It is cleared to a "0" whenever the counter is loaded from the counter input register.
5-4	RW1-0 - These two bits indicate the counter read/write word size. This information is useful in determining where the high byte, the low byte or both must be transferred during counter read/write operations.
3-1	M2-0 - These bits reflect the operating mode of the counter and are interpreted in the same manner as in the write control word format.
0	BCD - This bit indicates the counting element is operating in binary format or BCD format.

Counter Operation

Because counter 0 and counter 1 have limitations in some of their operating modes, we will use counter 2 to describe the various counter operating modes. But the description of modes 0, 2, 3 and 4 is suitable for all counters. The following terms are defined for describing counter/timer operation.

TMRCLK pulse - A rising edge followed by a falling edge of the UM82C206 TMRCLK input.

trigger - The rising edge of the GATE2 input.

counter load - The transfer of the 16-bit value in counter input latches to to the counting element.

initialized - A control word written and the counter input latches loaded.

Counter 2 can operate in one of the following modes:
Mode 0 - Interrupt on terminal count
Mode 1 - Hardware retriggerable one-shot
Mode 2 - Rate generator
Mode 3 - Square wave generator
Mode 4 - Software triggered strobe
Mode 5 - Hardware triggered strobe

Mode 0 - Interrupt on terminal count

Mode 0 is usually used for event counting. After the counter being written with the control word, OUT2 of the counter goes low and remains low until the counting element reaches 0 at which time it goes back high and remains high until a new count or control word is written. Counting is enabled when GATE2 = 1 and disabled when GATE2 = 0. GATE2 has no effect on OUT2.

The counting element is loaded at the first TMRCLK pulse after the control word and initial count are loaded. When both initial count bytes are required, the counting element is loaded after the high byte is written. This TMRCLK pulse does not decrement the count, so for an initial count of N, OUT2 does not go high until N+1 TMRCLK pulses after initialization. Writing a new initial count to the counter reloads the counting element on the next TMRCLK pulse and counting continues from the new count. If an initial count is written with GATE2 = 0, it will still be loaded on the next TMRCLK pulse. But counting does not progress until GATE2 = 1. When GATE2 goes high, OUT2 will go high after N TMRCLK pulses later.

Mode 1 - Hardware retriggerable one-shot

Writing the control word causes OUT2 to go high initially. Once initialized the counter is armed and a trigger causes OUT2 to go low on the next TMRCLK pulse. OUT2 then remains low until the counter reaches 0. An initial count of N results in a one-shot pulse N TMRCLK cycles long. Any subsequent triggers while OUT2 is low cause the counting element to be reloaded, extending the length of the pulse. Writing a new count to counter input latches will not affect the current one-shot pulse unless the counter is retriggered. In the latter case, the counting element is loaded with the new count and the one-shot pulse continues until the new count expires.

Mode 2 - Rate generator

This mode functions as a divide-by-N counter. After writing the control word during initialization the counter's OUT2 is set to high.

When the initial count is decremented to 1, OUT2 goes low on the next TMRCLK pulse. The following TMRCLK pulse returns OUT2 high, reloads the CE and the process is repeated. In Mode 2 the counter continues counting (if GATE2 = 1) and will generate an OUT2 pulse every N TMRCLK cycles. Note that a count of 1 is illegal in Mode 2.
GATE2 = 0 disables counting and forces OUT2 high immediately. A trigger reloads the CE on the next TMRCLK pulse. Thus GATE2 can be used to synchronize the counter to external events.

Writing a new count while counting does not affect current operation unless a trigger is received. Otherwise, the new count will be loaded at the end of the current counting cycle.

Mode 3 - Square wave generator

Mode 3 is similar to Mode 2 in every respect except for the duty cycle of OUT2. OUT2 is set high initially and remains high for the first half of the count. When the first half of the initial count expires, OUT2 goes low for the remainder of the count.
If the counter is loaded with an even count, the duty cycle of OUT2 will be 50% (high = low = N/2). For odd count values, OUT2 is high one TMRCLK cycle longer than it is low. Therefore, high = (N+1)/2 and low = (N-1)/2.

Mode 4 - Software triggered strobe

Writing the Control Word causes OUT2 to go high initially. Expiration of the initial count causes OUT2 to go low for one TMRCLK cycle. GATE2 = 0 disables counting but has no effect on OUT2. Also, a trigger will not reload the CE.

The counting sequence is started by writing the initial count. The CE is loaded on the TMRCLK pulse after initialization. The CE begins decrementing one TMRCLK pulse later OUT2 will golow for one TMRCLK cycle, (N+1) cycles after the initial count is written.

If a new initial count is written during a counting sequence, it is loaded into the CE on the next TMRCLK pulse and the sequence continues from the new count. This allows the sequence to be "retriggerable" by software.

Mode 5 - Hardware triggered strobe

Writing the Control Word causes OUT2 to go high initially. Counting is started by trigger. The expiration of the initial count causes OUT2 to go low for one TMRCLK cycle. GATE2 = 0 disables counting.

The CE is loaded on the TMRCLK pulse after a trigger. Since loading the CE inhibits decrementing, OUT2 will go low for one TMRCLK cycle, (N+1) TMRCLK cycles after the trigger.

If a new count is loaded during counting, the current counting sequence will not be affected unless a trigger occurs. A trigger causes the counter to be reloaded from CIL and CIH, making the counter "retriggerable".

Table 7. Gate Pin Function

Mode	Gate		
	Low	Rising	High
0	Disables Counting	---	Enables Counting
	---	a) Initiates Counting	---
	---	b) Resets Out Pin	---
2	a) Disables Counting	Initiates Counting	Enables Counting
	b) Forces Out Pin High		
3	a) Disables Counting	Initiates Counting	Enables Counting
	b) Forces Out Pin High		
4	Disables Counting	---	Enables Counting
5	---	Initiates Counting	---

GATE2

In Modes 0,2,3 and 4 GATE2 is level sensitive and is sampled on the rising edge of TMRCLK. In Modes 1, 2, 3 and 5 the GATE2 input is rising-edge sensitive. This rising edge sets an internal flip-flop whose output is sampled on the next rising edge of TMRCLK. The flip-flop resets immediately after being sampled. Note that in Modes 2 and 3 the GATE2 input is both edge and level sensitive.

REAL TIME CLOCK SUBSYSTEM

REAL TIME CLOCK FUNCTIONAL DESCRIPTION

This subsystem of the UM82C206 integrates a complete time-of-day real time clock with alarm, one hundred year calendar, a programmable periodic interrupt, and 114 bytes of CMOS static RAM. The UM82C206 is designed to operate in a low power (battery powered) mode and protects the contents of both the CMOS static RAM and clock from change during system power up and down.

Power-Up/Down

Most applications will require the real time clock to remain active whenever the system power is turned off. To accomplish this the user must provide an alternate source of power to the UM82C206. This alternate source of power is normally provided by connecting a battery to the Vcc pin to switch from the system power supply to the battery. A circuit implementing such a function is shown in Figure 10. It is used to eliminate power drain on the battery when the entire UM82C206 is active. It will also make a clean and reliable transition between system and battery power without drawing too much battery power.

The PWRGD pin is provided on the device to protect the contents of RAM and the real time clock. It is also used to reduce power consumption whenever the system is powered down. This pin should be low whenever the system power supply is not within specifications for proper operation of the system. This pin may be driven by circuitry in either the power supply or on the system board. When the PWRGD input is low, it will disable all unnecessary inputs and outputs. In this way it will prevent noise on the inactive pins and reduce leakage current when the system is powered down. This pin must therefore be at high level for the remainder of the device to operate properly when system power is applied.

The PSRSTB* pin is provided to initialize the device whenever power is applied to the UM82C206. This pin will not alter the RAM or real time clock contents but it will initialize the necessary control register bits. A low on PSRSTB* pin disables the generation of interrupts and sets a flag indicating that the contents of the device may not be valid. A recommended circuit for controlling the PSRSTB* input is shown in Figure 10.

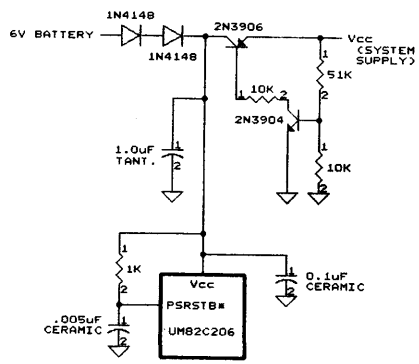


Figure 10. Power Conversion and Reset Circuitry

Register Access

Reading and writing to the 128 locations in this subsystem is accomplished by first placing the index address of the location you wish to access on the data input pins XD0-XD6 and then strobing the AS input pin. The address will then be latched into the index address register on the falling edge of AS. The index address register is then used as a pointer to the specific byte in this subsystem, which may be read or written by asserting XIOR* or XIOW* with an address of 071H on the XA9-XA0 input pins.

In PC/AT compatible design, the AS is generated by an I/O write operation to port 070H. To avoid the unintentional change of the contents of real time clock and CMOS RAM, it is recommended that an address of 070H be applied to the XA9-XA0 inputs of UM82C206 during the AS asserted time.

Address Map

Table 8 illustrates the internal register/RAM organization of the real time clock subsystem of the UM82C206. The 128 addressable locations in this subsystem are divided into 10 bytes which normally contain the time, calendar, alarm setting and four control and status bytes and 114 general purpose CMOS RAM bytes. All 128 bytes are readable by the CPU. The CPU may also write to all locations except registers 0CH, 0DH, bit 7 of register 0AH and bit 7 of the register 00H which is always 0.

Table 8. Address Map for Real Time Clock Subsystem

Index	Function
00H	SECONDS
01H	SECONDS ALARM
02H	MINUTES
03H	MINUTES ALARM
04H	HOURS
05H	HOURS ALARM
06H	DAY OF WEEK
07H	DAY OF MONTH
08H	MONTH
09H	YEAR
0AH	REGISTER A
0BH	REGISTER B
0CH	REGISTER C
0DH	REGISTER D
0EH	USER RAM
0FH	USER RAM
. . .	
7EH	USER RAM
7FH	USER RAM

Time/Calender and Alarm Bytes

The CPU can obtain the time and calendar information by reading the appropriate locations in the real time clock. Initialization of the time, calendar and alarm information is accomplished by writing to these bytes. Data stored in these locations are in binary-coded decimal (BCD) format.

Before initialization of the internal registers of the real time clock, the SET bit in register 0BH should be set to a "1" to prevent real time clock from updating. The CPU then initializes the first 10 locations in BCD format. The SET bit should then be cleared to allow updating. After initialized and enabled, the real time clock will perform clock/calendar updates at a 1.024 KHz rate in PC/AT compatible design.

Table 9. Time, Calendar, Alarm Data Format

Index Register Address	Function	BCD Range
00H	Seconds	00-59
01H	Seconds of Alarm	00-59
02H	Minutes	00-59
03H	Minutes of Alarm	00-59
04H	Hours (12 hour mode) Hours (24 hour mode)	01-12 (AM) 81-92 (PM) 00-23
05H	Hours of Alarm (12 hour mode) Hours of Alarm (24 hour mode)	01-12 (AM) 81-92 (PM) 00-23
06H	Day of Week	01-07
07H	Day of Month	01-31
08H	Month	01-12
09H	Year	00-99

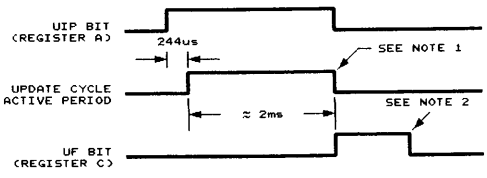
The alarm bytes can be programmed to generate an interrupt at a specific time or they can be programmed to generate a periodic interrupt. To generate an interrupt at a specific time, the user need only program the time that the interrupt is to occur into the 3 alarm bytes. Alternately, a periodic interrupt can be generated by setting the high order two bits in an alarm register to a "1", which turns that byte into a "don't care". For instance, an interrupt can be generated once a second by programming the same value into all three alarm registers.

Table 9 shows the format for the ten clock, calendar and alarm registers. The 24/12 bit in Register 0BH determines whether the hour locations will be updated using a 1-12 or 0-23 format. After initialization the 24/12 bit cannot be changed without reinitializing the hour locations. In 12 hour format the bit 7 of the hours byte in both the time and alarm bytes will indicate PM when it is a "1".

Update Cycle

During normal operation the real time clock will perform an update cycle, assuming one of the proper time bases is chosen, the divider bits DV2-DV0 isn't reset and the SET bit in register 0BH is cleared. The function of the update cycle is to increment the clock/calendar registers and compare them to the alarm registers. If a match or don't care condition occurs between the two sets of registers, an alarm is issued and an interrupt control bits are enabled.

During an update cycle, the lower 10 registers are not accessible by the CPU. By this way it can prevent the possible corruption of data in the real time clock registers or the reading of incorrect data. To avoid contention between the



NOTE:
1. REGISTER 0-9 ARE UNAVAILABLE FOR READ OR WRITE THIS TIME.
2. UF BIT CLEARED BY READING REGISTER C.

Figure 11. Update Cycle

real time clock and the CPU, a flag is provided in register 0AH to alert the user of an update in progress cycle. This update in progress bit (UIP) is asserted 244us before the actual start of the cycle and is maintained until the cycle is complete. Once the cycle is complete the UIP bit will be cleared and the update flag (UF) in register 0CH will be set. Figure 11 illustrates the update cycle. CPU access is always allowed to registers 0AH through 0DH during update cycles.

Two recommended methods can be used for reading and writing to the real time clock in a PC/AT compatible design. Both of them will allow the user to avoid contention between the CPU and the real time clock for access to the time and date data.

The first method is to read register 0AH, determine the state of the UIP bit and if it is "0", perform the read or write operation. For this method to work successfully the entire read or write operation (including any interrupt service routines which might occur) must not require longer than 244us to complete from the beginning of the read of register 0AH to the completion of the last read or write operation to the clock calendar registers.

The second method of accessing the lower 10 registers is to read register 0CH once and disregard the contents. Then subsequently continue reading this register until the UF bit is a "1". This bit will become true immediately after an update cycle has been completed. The user then has to complete a read or write operation before the next update cycle.

Control and Status Registers

The UM82C206 contains four registers used to control the operation and monitor the status of the real time clock. The CPU can access these registers at any time with index address at 0AH-0DH.

REGISTER 0AH

Index register port : 70H
Data register port : 71H
Index : 0AH (Read/Write register except UIP)

REGISTER 0AH

Bits	Function
7	UIP - Update in progress flag is a status bit used to indicate when an update cycle is about to take place. A "1" indicates that an update cycle is taking place or is imminent. UIP will go active (HIGH) 244us prior to the start of an update cycle and will remain active for an additional 2ms while the update is occurring. The UIP bit is read only and is not affected by reset. Writing a "1" to the SET bit in register 0BH will clear the UIP status bit.
6-4	DV2-DV0 - These three bits are used to control the Divider/Prescaler on the real time clock. While the UM82C206 can operate at frequencies higher than 32.768 KHz, this is not recommended for battery powered operation due to the increased power consumption at these higher frequencies.

Bits	Function

6	5	4	Divider Options	
DV2	DV1	DV0	OSCI Freq.	Mode
0	0	0	4.194304MHz	Operate
0	0	1	1.048576MHz	Operate
0	1	0	32.768KHz	Operate
1	1	X	Reset Divider	

3-0 RS3-RS0 - These four bits control the periodic interrupt rate. The periodic interrupt is derived from the divider/prescaler in the real time clock and is separated from the alarm interrupt. Both the alarm and periodic interrupts do, however, use the same interrupt channel in the interrupt controller. Use of the periodic interrupt allows the generation of interrupts at rates higher than once per second. Below are the interrupt rates for which the real time clock can be programmed.

3	2	1	0	Periodic Interrupt Rate	
RS3	RS2	RS1	RS0	4.194304MHz time base 1.048576MHz time base	32.768KHz time base
0	0	0	0	None	None
0	0	0	1	30.517 us	3.90625 ms
0	0	1	0	61.035 us	7.8125 ms
0	0	1	1	122.070 us	122.070 us
0	1	0	0	244.141 us	244.141 us
0	1	0	1	488.281 us	488.281 us
0	1	1	0	976.562 us	976.562 us
0	1	1	1	1.953125 ms	1.953125 ms
1	0	0	0	3.90625 ms	3.90625 ms
1	0	0	1	7.8125 ms	7.8125 ms
1	0	1	0	15.625 ms	15.625 ms
1	0	1		31.25 ms	31.25 ms
1	1		1	62.5 ms	62.5 ms
1	1	0	1	125 ms	125 ms
1	1	1	0	250 ms	250 ms
1	1	1	1	500 ms	500 ms

REGISTER 0BH

Index register port : 70H
Data register port : 71H
Index : 0BH (Read/Write register)

Bits	Function
7	SET - Writing a "0" to this bit enables the Update Cycle and allows the Real Time Clock to function normally. When set to a "1" the Update Cycle is inhibited and any cycle in progress is aborted. The SET bit is not affected by the RESET input pin.
6	PIE - The Periodic Interrupt Enable Bit controls the generation of interrupts based on the value programmed into the RS3-RS0 bits of Register 0AH. This allows the user to disable this function without affecting the programmed rate. Writing a "1" to this bit enables the generation of periodic interrupts. This bit is cleared to "0" by Reset.
5	AIE - The generation of alarm interrupts is enabled by setting this bit to a "1". Once this bit is enabled the Real Time Clock will generate an alarm whenever a match occurs between the programmed alarm and clock information. If the don't care condition is programmed into one or more of the Alarm Registers, this will enable the generation of periodic interrupts at rates of one second or greater. This bit is cleared by Reset.
4	UIE - The update ended interrupt enable bit is used to enable the update end flag (UF) bit in register 0CH to generate an interrupt. A "1" in this bit enables the interrupt generating. A "0" disables it. This bit is cleared by reset. It is also cleared when the SET bit goes high.
3	SQWE - The square wave enable bit is always fixed to 0. It will disable the square wave generation.
2	DM - The data mode bit is always fixed to 0. It will always select the BCD format for real time clock.
1	24/12 - The 24/12 control bit is used to establish the format of both the Hour and Hour Alarm bytes. If this bit is a "1", the Real Time Clock will interpret and update the information in these two bytes using the 24 hour mode. This bit can be read or written by the CPU and is not affected by Reset.
0	DSE - The Real Time Clock can be instructed to handle daylight savings time changes by setting this bit to a "1". This enables two execeptions to the normal time keeping sequence to occur. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. Setting this bit to a "0" disables the execution of these two exceptions. RESET has no effet on this bit.

REGISTER 0CH

Index register port : 70H
Data register port : 71H

Bits	Function
7	IRQF - The interrupt request flag bit is set to a "1" when any of the conditions which can cause an interrupt is true and the interrupt enable for that condition is true. The condition which causes this bit to be set, also generates an interrupt. The logic expression for this flag is : IRQF = PF & PIE + AF & AIE + UF & UIE This bit and all other active bits in this register are cleared by reading the register or by activating the PSRSTB* input pin. Writing to this register has no effect on the contents.
6	PF - The periodic interrupt flag is set to a "1" when a transition, which is selected by RS3-RS0, occurs in the divider chain. This bit will become active, independent of the condition of the PIE control bit. The PF bit will then generate an interrupt and set IRQF if PIE is a "1".
5	AF - A "1" appears in the AF bit whenever a match has occured between the time registers and alarm registers during an update cycle. This flag is also independent of it's enable (AIE) and will generate an interrupt if AIE is true.
4	UF - A "1" appears in the UF bit whenever an update cycle is ended. This flag is also independent of it's enable (UIE) and will generate an interrupt if UIE is true.
3-0	Not used - All unused bits will be "0" when read and are not writeable.

REGISTER 0DH

Index register port : 70H
Data register port : 71H
Index : 0DH (Read Only register)

Bits	Function
7	VRT - The valid CMOS RAM and time bit indicates the condition of the contents of the RAM and real time clock. This bit is cleared to a "0" whenever the PSRSTB* input pin is low. This is normally derived from the power supply which supplies Vcc to the device and will allow the user to determine whether the registers have been initialized since power was applied to the device. Reset has no effect on this bit and it can only be set by reading register 0DH.
6-0	Not used - All unused bits will be "0" when read and are not writeable.

CMOS Static RAM

The 114 bytes of RAM from index address 0EH to 7FH are not affected by the real time clock. They are accessible during the update cycle and may be used for whatever the designer wishes. Typical applications will use these as nonvolatile storage for system configuration parameters. They are normally battery powered when the system is turned off.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	VCC	-0.3	+6.7	V
Input Voltage	Vi	-0.3	+6.7	V
Output Voltage	Vo	-0.3	Vcc+0.3	V
Operating Temperature	Top	-20	+70	°C
Storage Temperature	Tstg	-55	+125	°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are a stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC ELECTRICAL CHARACTERISTICS
(Vcc = 4.75 to 5.25V, Ta = -20 to +70°C)

Symbol	Parameter	Min.	Max.	Unit	Test Condition	Note
ViL	Input Low Voltage	-0.3	+0.8	V		
ViH	Input High Voltage	+2.2	Vcc+0.3	V		
VoL	Output Low Voltage (Iol=8mA)	-	0.5	V		
VoH	Output High Voltage (Ioh=-2mA)	3.5	-	V		
IiL	Input Leakage Current	-	1	uA		
Iozi	Output High-Z Leakage Current	-	1	uA		
Iccsb	Standby Power Supply Current	-	10	uA		

AC ELECTRICAL CHARACTERISTICS (8 MHz)
(Vcc = 4.75 to 5.25V, Ta = -20 to +70°C)

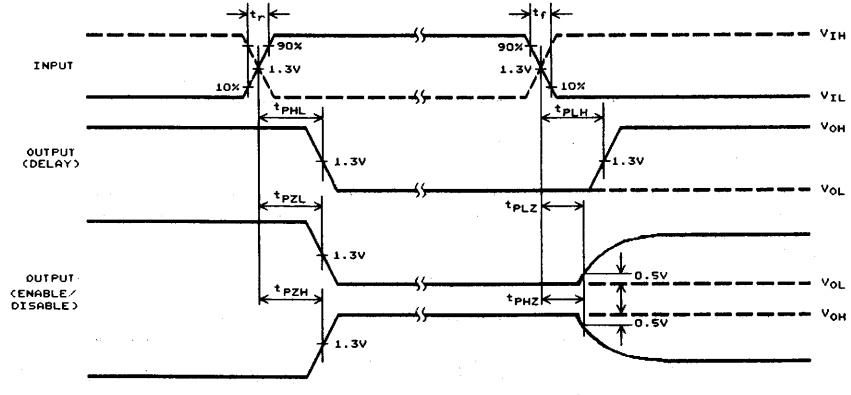
Symbol	Description	Min.	Typ.	Max.	Unit	Test Condition	Note
t1	Address setup to command active	25			ns		
t2	Command active period			200	ns		
t3	Address hold time from command inactive	0			ns		
t4	Data valid delay	160			ns		
t5	Data hold time from XIOR* inactive	10			ns		
t6	XD0-XD7 active from XIOR*	5		40	ns		
t7	Data setup to XIOW* inactive	160			ns		
t8	Data hold time from XIOW* inactive	0			ns		
t9	Command recovery time	120			ns		
t10	Interrupt request low width	100			ns		
t11	Interrupt request high width	200			ns		
t12	INTR output delay			300	ns		
t20	Real time clock cycle time			500	ns		
t21	AS pulse width	160			ns		
t22	Data valid setup to AS inactive	160			ns		
t23	Data hold time from AS inactive	0			ns		
t24	OSCI period	500			ns		
t25	OSCI high time	200			ns		
t26	OSCI low time	200			ns		
t27	PSRSTB high delay from VCC	5			us		
t28	PSRSTB low pulse width	5			us		
t29	VRT bit valid delay			2	ns		
t40	TMRCLK period	125			ns		

Symbol	Description	Min.	Typ.	Max.	Unit	Test Condition	Note
t41	TMRCLK low time	50			ns		
t42	TMRCLK high time	50			ns		
t43	GATE2 setup to TMRCLK	50			ns		
t44	GATE2 hold time from TMRCLK	50			ns		
t45	GATE2 low time	50			ns		
t46	GATE2 high time	50			ns		
t47	OUT2 delay from TMRCLK			120	ns		
t48	OUT2 delay from GATE2			120	ns		
t50	SYSCLK period (DMA clock = SYSCLK)	125			ns		
t50a	SYSCLK period (DMA clock = SYSCLK/2)	62			ns		
t51	SYSCLK low time (DMA clock = SYSCLK)	43			ns		
t51a	SYSCLK low time (DMA clock = SYSCLK/2)	22			ns		
t52	SYSCLK high time (DMA clock = SYSCLK)	55			ns		
t52a	SYSCLK high time (DMA clock = SYSCLK/2)	27			ns		
t53	DREQi setup to SYSCLK	0			ns		
t54	HRQ valid from SYSCLK			75	ns		
t55	HLDA1 setup to SYSCLK	45			ns		
t56	AENi valid delay from SYSCLK			105	ns		

Symbol	Description	Min.	Typ.	Max.	Unit	Test Condition	Note
t57	AENi invalid delay from SYSCLK			80	ns		
t58	ADSTBi valid delay from SYSCLK			50	ns		
t59	ADSTBi invalid delay from SYSCLK			120	ns		
t60	XD0-XD7 active delay from SYSCLK			60	ns		
t61	XD0-XD7 valid setup to ADSTBi low	65			ns		
t62	XD0-XD7 hold time from ADSTBi low	25			ns		
t63	XD0-XD7 tristate delay from SYSCLK			135	ns		
t64	Address valid delay from SYSCLK			60	ns		
t65	Address hold time from DMAMEMR high	50			ns		
t66	Address tristate delay from SYSCLK			55	ns		
t67	DACKi delay from SYSCLK			105	ns		
t68	Command enable delay from SYSCLK			90	ns		
t69	Command active delay from SYSCLK			120	ns		
t70	Write command inactive delay from SYSCLK			80	ns		
t71	Address hold time from write command high	75			ns		
t72	Command tristate delay from SYSCLK			75	ns		
t73	Read command inactive delay from SYSCLK TC delay from SYSCLK			115	ns		
t74	TC delay from SYSCLK			60	ns		
t75	XD0-XD7 setup to read command inactive	90			ns		

Symbol	Description	Min.	Type	Max.	Unit	Test Condition	Note
t76	XD0-XD7 hold time from read command inactive	0			ns		
t77	XD0-XD7 valid delay from SYSCLK			120	ns		
t78	XD0-XD7 hold from write command inactive	15			ns		
t79	IOCHRDY input setup to SYSCLK	35			ns		
t80	IOCHRDY input hold time from SYSCLK	20			ns		

TIMING WAVEFORMS



V_{IH} = 3V, V_{IL} = 0V, $t_r \leq 10ns$, $t_f \leq 5ns$

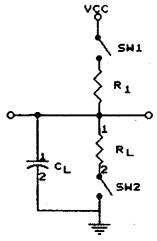
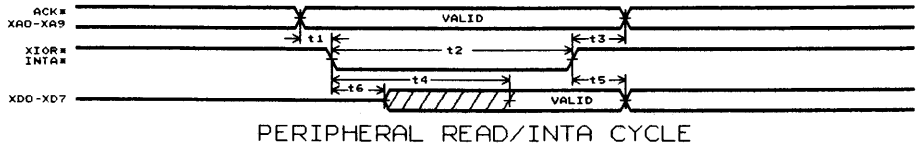
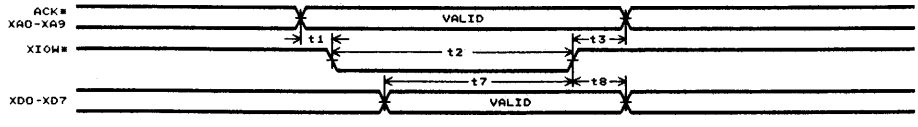


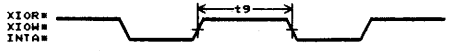
Figure 12. AC Characteristics Measurement Waveform and Load Circuit



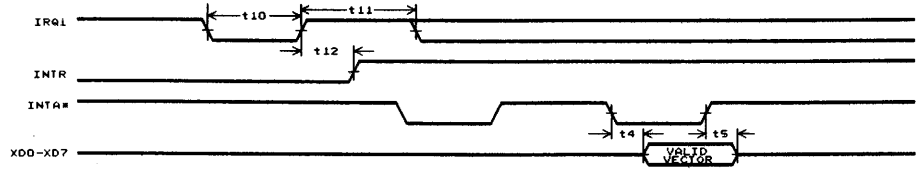
PERIPHERAL READ/INTA CYCLE



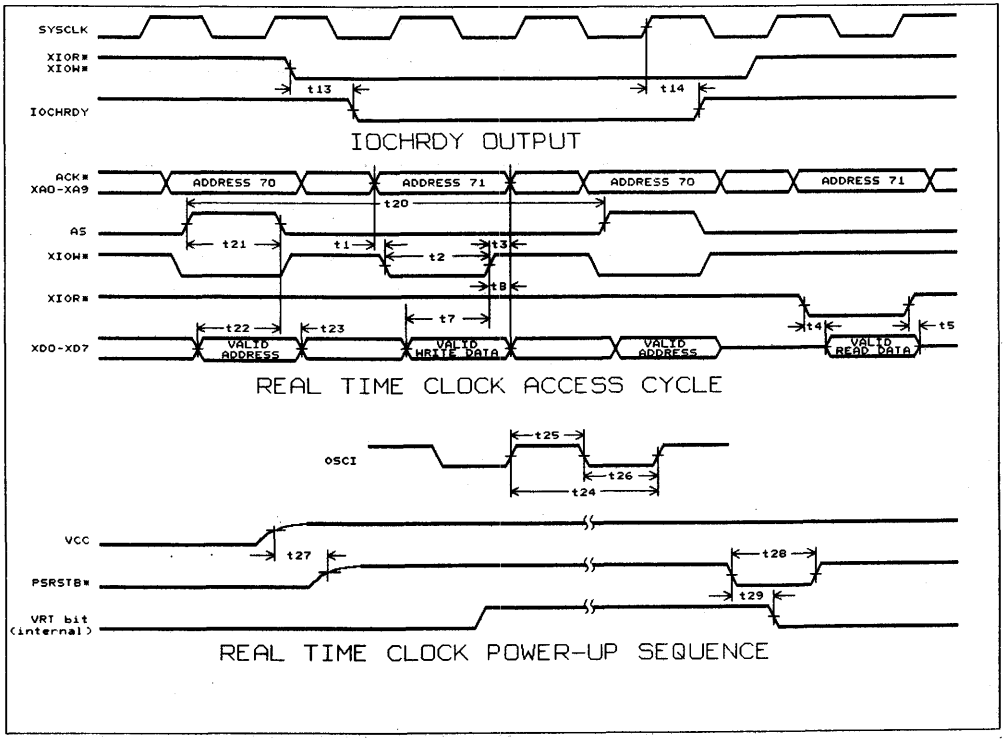
PERIPHERAL WRITE CYCLE

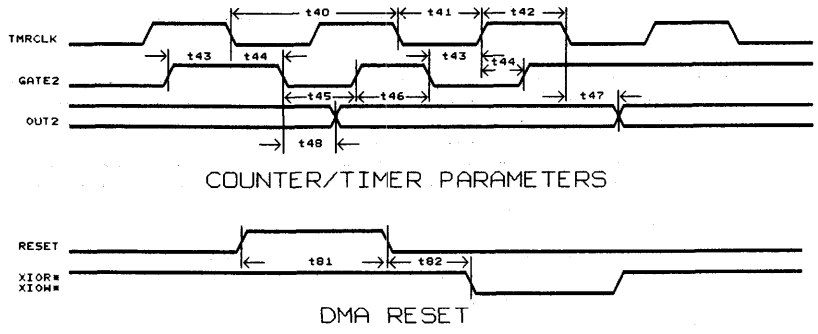


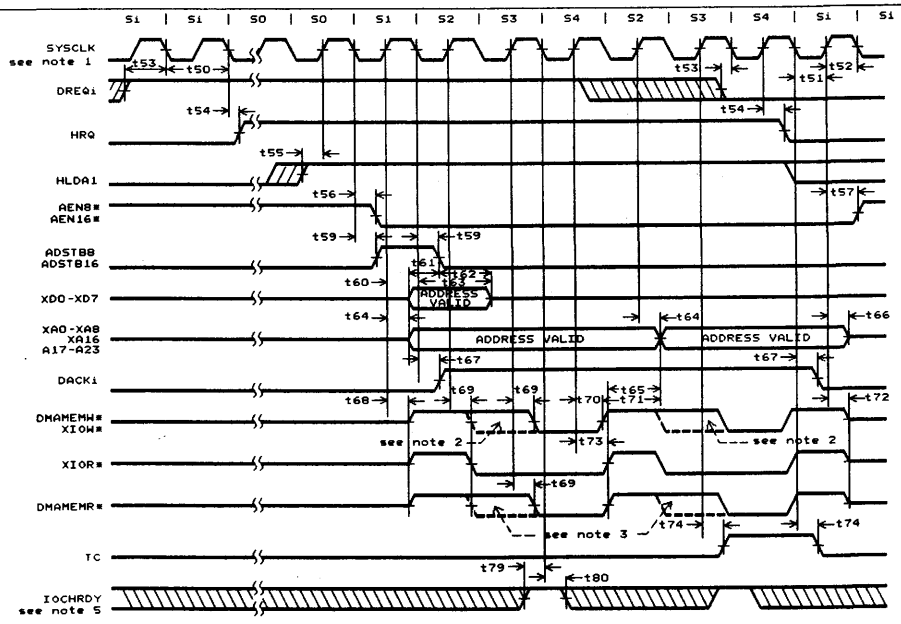
COMMAND RECOVERY



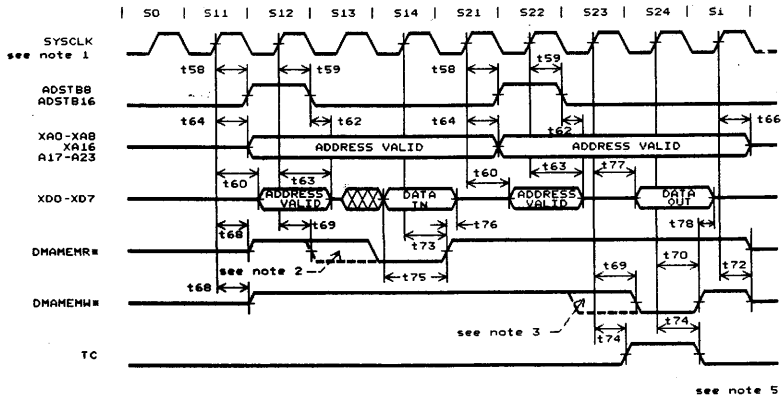
INTA SEQUENCE


SYSCLK
XIOR#
XIOW#
t13
t14
IOCHRDY
IOCHRDY OUTPUT
ACK#
XA0-XA9
ADDRESS 70
ADDRESS 71
ADDRESS 70
ADDRESS 71
t20
AS
t21
t1
t3
t2
XIOW#
t8
XIOR#
t22
t23
t7
t4
t5
XD0-XD7
VALID ADDRESS
VALID WRITE DATA
VALID ADDRESS
VALID READ DATA
REAL TIME CLOCK ACCESS CYCLE
OSCI
t25
t26
t24
VCC
t27
t28
PSRSTB#
t29
VRT bit (internal)
REAL TIME CLOCK POWER-UP SEQUENCE

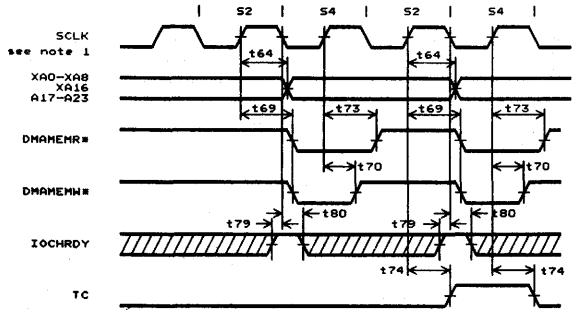

t40
t41
t42
TMRCLK
t43
t44
t43
t44
GATE2
t45
t46
t47
OUT2
t48
COUNTER/TIMER PARAMETERS
RESET
t81
t82
XIOR#
XIOW#
DMA RESET



DMA Transfer Timing



Memory - to - Memory Transfer



Compressed Transfer

NOTES:

1. All timings referenced to SCLK are independent of the state of the clock select bit in the configuration register. SCLK shown in this diagram is the undivided clock directly from the input.

2. Extended Write mode selected.

3. Extended Read mode selected.

4. IOCHRDY Input Timing.

5. DMA wait states are added between S3,S4 in normal timing; between S2,S4 in compressed timing; between S13, S14 and S23, S24 in memory-to-memory timing.

UMC

UM82C210 Series
386SX/286 AT Chip Set

Features

* 100% PC/AT compatible enhanced chip set for 12 Mhz, 16 Mhz and 20 Mhz systems.
* Supports Page Interleaved Mode & Single Bank Page Mode for memory access.
* Supports 16 Mhz 80286/80386SX systems with 100 ns DRAMs and 20 Mhz systems with 80 ns DRAMs.
* Separated CPU and AT Bus clocks.
* Supports LIM EMS 4.0.
* Programmable memory configuration , Command Delays , and Wait States.
* Supports Shadow RAM for Video ROM and BIOS.
* Optimized for OS/2 operation.

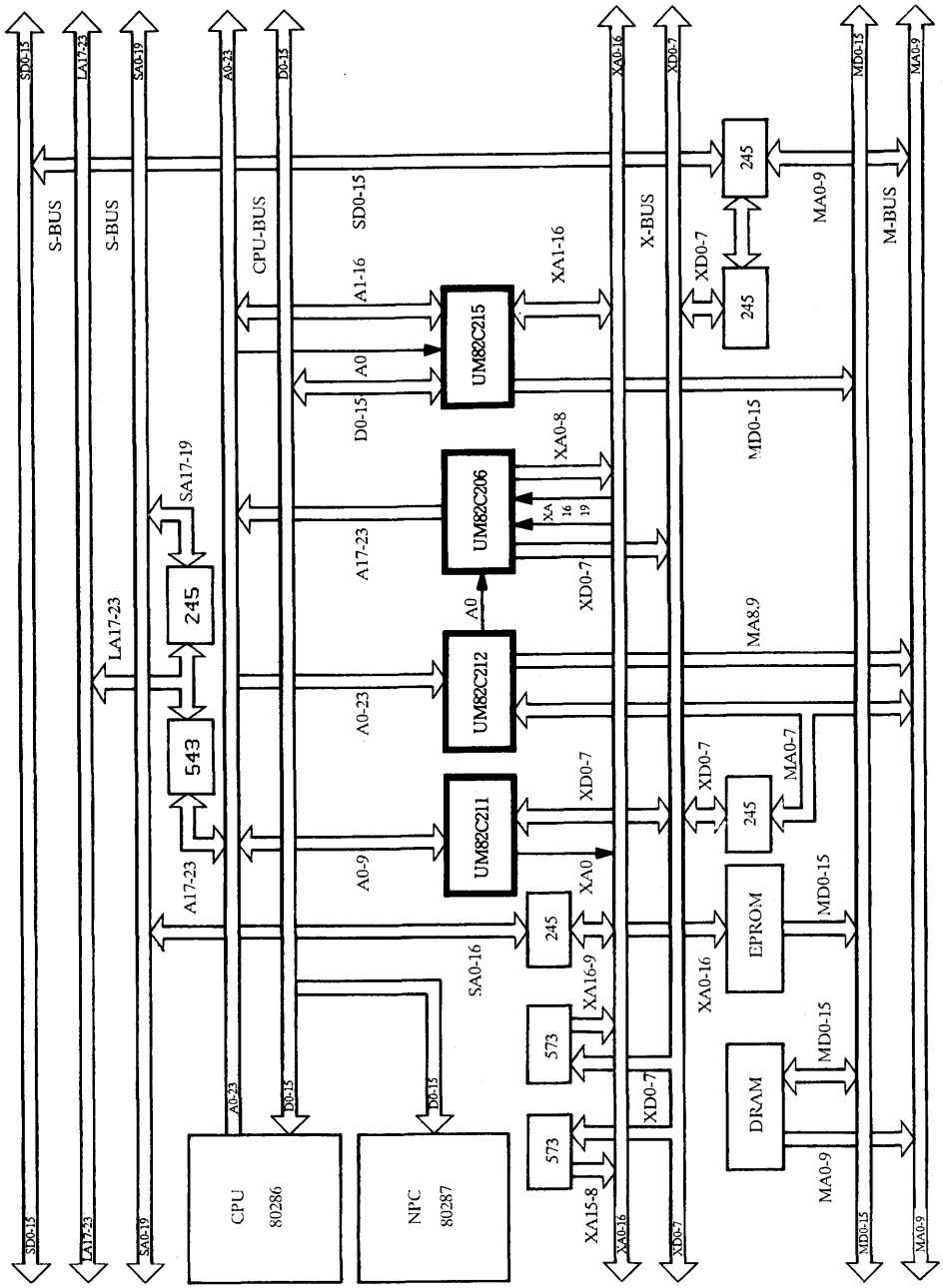
General Description

The UM82C210 is an enhanced PC/AT compatible chip set which is a highly integrated VLSI implementation of the control logic used in the IBM AT. Due to its flexible architecture, the UM82C210 can be used in any 80286 based systems. The UM82C210 chip set consists of three chips which are: UM82C211 (System Controller), UM82C212 (Memory Controller) , and UM82C215 (Data /Address Buffer).

The UM82C211 , System controller, provides all control signals for AT bus including bus synchronization. In order to meet timing requirements for different peripheral boards, the UM82C211 provides programmable command delays and wait states.

The UM82C212 , Memory Controller, provides both conventional memory access and Page Interleaved memory access. The UM82C212 also has LIM EMS features that support up to 8 MB of on-board DRAMs. In addition, the Shadow RAM feature of the UM82C212 allows faster execution BIOS codes.

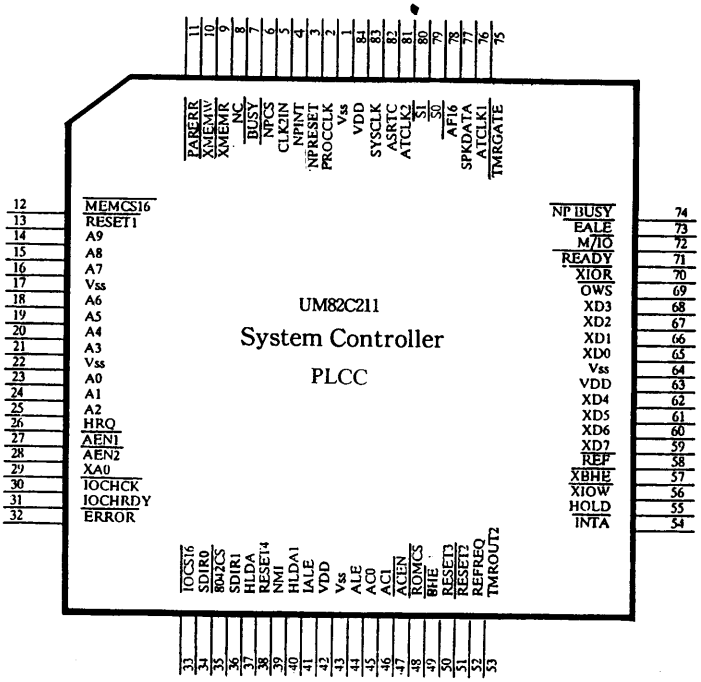
The UM82C215, Data/Address Buffer, provides buffering and latching functions between address buses and data buses. It also generates the parity bit and detects parity errors.



16/20-MHZ AT System Block Diagram

1. UM82C211 SYSTEM CONTROLLER

The UM82C211 highly integrates CPU interface and bus control logic. Most of the system functions, except memory access, are taken care of by the UM82C211. The main functions of the UM82C211 are reset and shutdown, clock generation, clock speed selection, CPU state machine, AT bus state machine, bus arbitration , action code generation, Port B and NMI generation, DMA, refresh, numeric coprocessor interface, etc.



1.1 Operation Modes of the UM82C211

There are 4 operation modes provided by the UM82C211 for different CPU and AT bus clock selections. These 4 modes are Normal, Quick, Delayed, and External Modes.

1.1.1 Normal Mode

The clock selections in Normal Mode are:

PROCCLK = CLK2IN and
SYSCLK = CLK2IN / 4

Because the PROCCLK and SYSCLK are both derived from the CLK2IN, the Normal Mode is asynchronous mode. In the Normal Mode, the ALE and commands ($\overline{\text{XMEMR}}$, $\overline{\text{XMEMW}}$, $\overline{\text{XIOR}}$, $\overline{\text{XIOW}}$) are issued for AT bus cycle only, and have nothing to do with the local cycles.

1.1.2 Quick Mode

The clock selections in Quick Mode are:

PROCCLK = CLK2IN and
SYSCLK = CLK2IN / 2

Since the PROCCLK and SYSCLK are both derived from the CLK2IN, the Quick Mode is a synchronous mode also. One of the differences between the Normal Mode and the Quick Mode is that the ALE signal is generated on the AT bus for both AT bus cycle and local bus cycle in the Quick Mode while the ALE is generated for only AT bus cycle in the Normal Mode. However, the commands (XMEMR, XMEMW, XIOR, XIOW) are still not issued for local bus cycles in the Quick Mode.

1.1.3 Delayed Mode

The clock selections in Delayed Mode are:

PROCCLK = CLK2IN and
SYSCLK = CLK2IN / 2

This mode is a synchronous mode also. The clock selections for the Delayed Mode are the same as the selections for the Quick Mode. However, this mode is enabled when the Quick Mode is disabled. In the Delayed Mode, the ALE and commands are generated for AT bus cycle only, and not generated for any local bus cycle.

1.1.4 External Mode

The clock selections in External Mode are :

PROCCLK = CLK2IN and
SYSCLK = ATCLK / 2

Since the ATCLK is running asynchronously to CLK2IN and the SYSCLK is derived from ATCLK, the External Mode is an asynchronous mode.

1.2 Configuration Registers

There are three 8-bit registers provided in the UM82C211 for configuration purposes. In order to reduce the number of I/O ports required to access all the registers used in the UM82C210 chip set, the index access is used. To access a particular register, the index address is placed at address port and data is located at data port.

The first register, R11, is used for PROCCLK selections, time out enable, NMI enable, and CPU software reset. The second register, R12, is used for command delay selections , hold time delay, and Quick Mode enable. The third register ,R13, is used for SYSCLK selections, wait state selections.

R11 : (Index Address 60H)

Bits	Function
7,6	UM82C211 revision number.
5	CPU reset.
4	Processor clock selection.
3	Reserved.
2	$\overline{\text{READY}}$ timeout NMI enable.
1	Reserved.
0	$\overline{\text{READY}}$ timeout.

R12 : (Index Address 61H)

Bits	Function
7	Address hold time delay.
6	Quick Mode enable.
5,4	AT Bus 16 bit memory command delay.
3,2	AT Bus 8 bit memory command delay.
1,0	AT Bus I/O cycle command delay.

R13 : (Index Address 62H)

Bits	Function
7,6	Reserved.
5,4	Wait state selection for 16 bit AT cycle.
3,2	Wait state selection for 8 bit AT cycle.
1,0	Bus clock selection.

1.3 Action Codes

In order to convert 16-bit operations to 8-bit operations for CPU to access 8-bit AT bus devices, the UM82C211 generates Action Code Enable and action codes to control the buffers in the UM82C215 for the bus conversion. Table 1.1 defines the Action Code Enable and Action Codes.

Operation	$\overline{ACEN}$	AC1	AC0	Function
DMA/MASTER	0	0	0	16 & 8-bit R/W operations
	0	0	1	Reserved
	0	1	0	Write, MD0-7 to MD8-15
	0	1	1	Read, MD8-15 to MD0-7
CPU(AT BUS)	0	0	0	16 & 8-bit W/O operations
	0	0	1	16 & 8-bit R/O operations
	0	1	0	8-bit write (high byte)
	0	1	1	8-bit read (high byte)
CPU(local)	1	X	X	No conversion

Table 1.1 Functions of Action Codes.

1.4. Numeric Coprocessor Interface

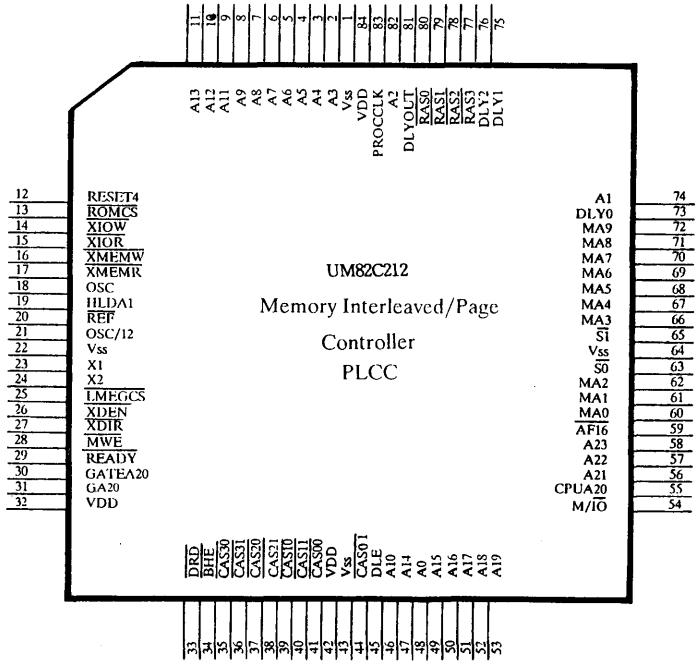
The UM82C211 provides necessary interface circuitry between 80286 and its coprocessor 80287. The major functions of the interface circuitry are as follows:

1) Numeric Coprocessor chip selection decoding.
2) Resetting Numeric Coprocessor.
3) Handling $\overline{NPBUSY}$ and $\overline{ERROR}$ signals from 80287 to the CPU.
4) Generating interrupt signals for error conditions.

2. UM82C212 MEMORY CONTROLLER

The UM82C212 performs the memory control functions in the UM82C210 system. Several distinquished features are integrated in the UM82C212 that makes the UM82C210 system become one of the most advanced 80286 AT compatible systems available. First of all, the UM82C212 provides Page Mode to access the memory with interleaved memory banks. By using this Page-Interleaved scheme, the UM82C212 provides higher performance over conventional DRAM accessing schemes. As a result, the UM82C212 can support a 16 Mhz system with 100 ns DRAM by the use of the Page-Interleaved mode.

The UM82C212 also supports up to 8 Mbytes of on board memory. Also, the UM82C212 will automatically re-map the RAM resident in 640 Kbytes to 1 Mbytes area to the top of the 1 Mbyte address space. In order to access the memory resident beyond the 1 Mbyte address space, the UM82C212 provides address translation logic to support the LIM-EMS 4.0. The shadow RAM feature is also integrated into the UM82C212 for efficient and fast BIOS execution. The UM82C212 also provides OS/2 optimization that allows faster switching between the real mode and protected mode. A staggered DRAM refresh scheme is also included to reduce power supply noise.



2.1 Memory Array Configuration

The memory configuration required by the 80286 PC/AT systems is organized as banks with widths of 18 bits. Sixteen bits are used as data words split into high and low order bytes. The other 2 bits are used as parity bits, one for each byte. Since the UM82C212 also provides conventional memory accessing, the minimum memory configuration can be a single bank for non-interleaved mode and page mode. However, at least two identical memory banks are required for the operation of the Interleaved mode. Table 2.1 shows the commonly used memory configurations.

	DRAM Type				Total Memory	EMS Range
	Bank0	Bank1	Bank2	Bank3		
1	256K	0	0	0	512Kb	0
2	1M	0	0	0	2Mb	1Mb to 2Mb
3	256K	256K	0	0	1Mb	1Mb to 1.384Mb
4	1M	1M	0	0	4Mb	1Mb to 4Mb
5	256K	256K	256K	256K	2Mb	1Mb to 2Mb
6	256K	256K	1M	1M	5Mb	1Mb to 5Mb
7	1M	1M	1M	1M	8Mb	1Mb to 8Mb

Table 2.1 Commonly Used Memory Configurations

As mentioned above, the possible memory configurations for Page-Interleaved mode are No. 3, 4, 5, 6, and 7 in Table 2.1. Others for Single Bank Page Mode.

2.2 Page/Interleaved Operation

Besides conventional memory accessing, there are several different accessing modes available that make the memory access time much shorter than the access time of the conventional mode. Three most commonly used modes are Interleaved Mode, Page Mode, and Page-Interleaved Mode.

Basically, the Page-Interleaved Mode takes the advantages of combining the operations of Interleaved Mode and Page Mode. It allows the memory to be interleaved at page boundary instead of 2 bytes boundary. Figure 2.1 shows the sequence diagram of the Page-Interleaved operation.

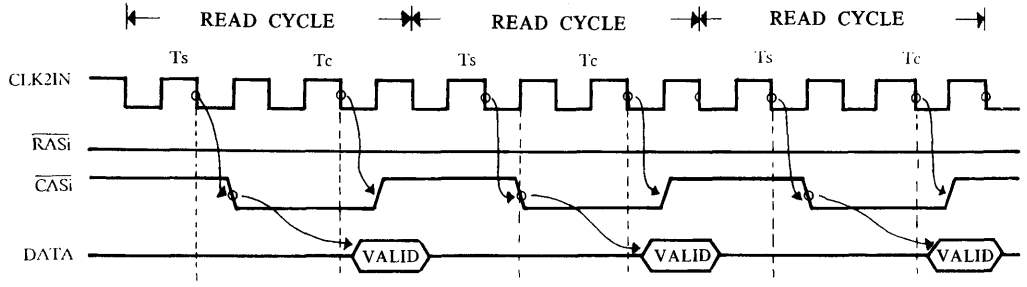


Figure 2.1 Page Mode Operation (Read Cycle)

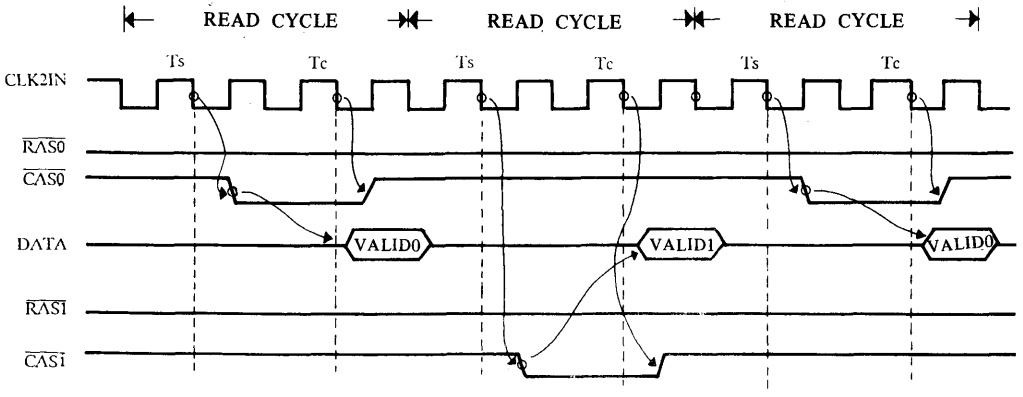


Figure 2.2 Page-Interleaved Mode Operation (Read Cycle)

2.3 Enhanced Functions

Besides the standard PC/AT functions, several new functions have been included in the UM82C210 chip set. These enhanced functions are OS/2 operation optimization, memory relocation, shadow RAM, EMS, etc.

2.3.1 OS/2 Operation Optimization

In order to switch CPU into protected mode for standard PC/AT architectures, the CPU has to issue two commands to the keyboard controller to reset the CPU and to activate GATEA20. The UM82C210 provides another method to handle the mode switching for OS/2 optimization. UM82C210 uses two I/O write operations; the CPU will be reset and GATEA20 will be enabled. Since this method involves two I/O writes only, it makes mode switching much faster.

2.3.2 Memory Relocation

Normally, the memory space from address 640K to 1M is reserved for EPROM use. However, if the system is equipped with 1 Mbyte DRAM, the memory with the addresses higher than 640K has to be relocated in order not to conflict with the EPROM addresses. The UM82C212 provides this kind of mapping. DRAM addresses from 640K to 1M will be translated to new addresses from 1M to 1.384M.

2.3.3 Shadow RAM

For the purpose of efficiency, it is preferable to execute BIOS codes through the DRAM accesses rather than through slower EPROM accesses. The UM82C212 provides the shadow RAM feature that allows the system to copy the BIOS codes from the EPROMs to the DRAMs with the same physical addresses and disable the EPROMs. This feature improves the performance of BIOS call intensive application programs significantly.

2.3.4 Expanded Memory System (EMS)

Due to the limitation of the DOS, the memory space with addresses higher than 1M can not be accessed in the real mode of the 80286 CPU. However, the EMS is a memory mapping scheme that provides a method for the system to access the memory beyond 1 Mbytes address. The EMS is used to map a 64 Kbyte block of memory within the area C0000H-EFFFFH to anywhere in the 1 Mbyte to 8 Mbyte area. This 64 Kbyte block is divided into four 16 Kbyte pages. Each 16 Kbyte segment can be mapped to anywhere independently through the translation table. The UM82C212 provides all the necessary logic with the translation table for the EMS operation.

In the case of using EMS mapper chip, the EMS is used to map a 64K byte block of memory within the area 40000H-7FFFFH & C0000H-EFFFFH to anywhere in the 1M byte to 8M byte area.

2.4 Configuration Registers

There are twelve 8-bit registers, R21-R2C provided in the UM82C212 for configuration purposes. In order to reduce the number of I/O ports required to access all the registers used in the UM82C210 chip set, the index access scheme is used. To access a particular register, the index address is placed at address port and the data is located at data port.

R21 : (Index address 64H)

Bits	Function
0-4	Reserved.
5,6	Revision number.
7	Chip identifier.

R22 : (Index address 65H)

Bits	Function
0	ROM disabled at F0000H-FFFFFH.
1	ROM disabled at E0000H-EFFFFH.
2	ROM disabled at D0000H-DFFFFH.
3	ROM disabled at C0000H-CFFFFH.
4	Write protection. Shadow RAM at F0000H-FFFFFH.
5	Write protection. Shadow RAM at E0000H-EFFFFH.
6	Write protection. Shadow RAM at D0000H-DFFFFH.
7	Write protection. Shadow RAM at C0000H-CFFFFH.

R23 : (Index address 66H)

Bits	Function
0-4	Reserved.
5	Reflects the 0-256K memory status for supporting EMS 4.0
6	Reflects the 256K-512K memory status for supporting EMS 4.0
7	Enable RAM on system board at 80000H-9FFFFH.

R24 : (Index address 67H)

Bits	Function
0	Enable Shadow RAM at B0000H-B3FFFH.
1	Enable Shadow RAM at B4000H-B7FFFH.
2	Enable Shadow RAM at B8000H-BBFFFH.
3	Enable Shadow RAM at BC000H-BFFFFH.
4	Enable Shadow RAM at A0000H-A3FFFH.
5	Enable Shadow RAM at A4000H-A7FFFH.
6	Enable Shadow RAM at A8000H-ABFFFH.
7	Enable Shadow RAM at AC000H-AFFFFH.

R25 : (Index address 68H)

Bits	Function
0	Enable Shadow RAM at C0000H-C3FFFH.
1	Enable Shadow RAM at C4000H-C7FFFH.
2	Enable Shadow RAM at C8000H-CBFFFH.
3	Enable Shadow RAM at CC000H-CFFFFH.
4	Enable Shadow RAM at D0000H-D3FFFH.
5	Enable Shadow RAM at D4000H-D7FFFH.
6	Enable Shadow RAM at D8000H-DBFFFH.
7	Enable Shadow RAM at DC000H-DFFFFH.

R26 : (Index address 69H)

Bits	Function
0	Enable Shadow RAM at E0000H-E3FFFH.
1	Enable Shadow RAM at E4000H-E7FFFH.
2	Enable Shadow RAM at E8000H-EBFFFH.
3	Enable Shadow RAM at EC000H-EFFFFH.
4	Enable Shadow RAM at F0000H-F3FFFH.
5	Enable Shadow RAM at F4000H-F7FFFH.
6	Enable Shadow RAM at F8000H-FBFFFH.
7	Enable Shadow RAM at FC000H-FFFFFH.

R27 : (Index address 6AH)

Bits	Function
0-4	Reserved.
5	Enable two banks of memory.
6,7	Type of DRAM : 0 0 : Disabled 1 0 : 256K and 64K bit DRAMs used. 0 1 : 256K bit DRAMs used. 1 1 : 1M bit DRAMs used

R28 : (Index address 6BH)

Bits	Function
0,1	ROM access wait state.
2,3	EMS memory access wait states.
4	EMS enable.
5	RAM access wait states.
6	RAM relocation (640K-1M).
7	Page-Interleaved mode enable.

R29 : (Index address 6CH)

Bits	Function
0-3	Reserved.
4	2-way/4-way page interleaved selection.
5	Number of local RAM banks used.
6,7	Local DRAM type : 0 0 : none. 1 0 : Reserved. 0 1 : 256 Kbit. 1 1 : 1 Mbit.

R2A : (Index address 6DH)

Bits	Function
0-3	EMS page register I/O base address. 0 0 0 0 : 208H/209H 1 0 0 0 : 218H/219H 1 0 1 0 : 258H/259H 0 1 1 0 : 268H/269H 0 1 0 1 : 2A8H/2A9H 1 1 0 1 : 2B8H/2B9H 0 1 1 1 : 2E8H/2E9H
4-7	Expanded memory base address. 0 0 0 0 : C0000H,C4000H,C8000H,CC000 1 0 0 0 : C4000H,C8000H,CC000H,D0000 0 1 0 0 : C8000H,CC000H,D0000H,D4000 1 1 0 0 : CC000H,D0000H,D4000H,D8000 0 1 0 0 : D0000H,D4000H,D8000H,DC000 1 0 1 0 : D4000H,D8000H,DC000H,E0000 0 1 1 0 : D8000H,DC000H,E0000H,E4000 1 1 1 0 : DC000H,E0000H,E4000H,E8000 0 0 0 1 : E0000H,E4000H,E8000H,EC000

R2B : (Index address 6EH)

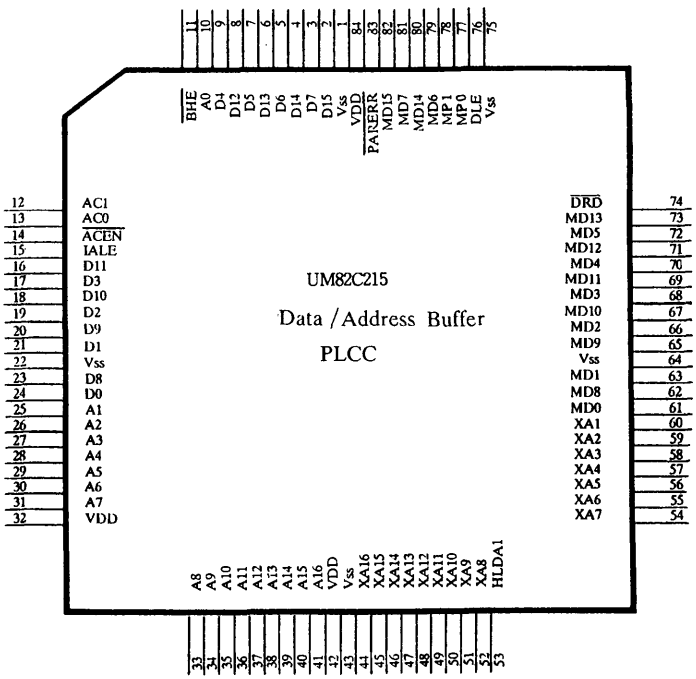
Bits	Function
0,1	EMS block for page 3 : Bit1 Bit0 EMS memory block (A22 A21) 0 0 : 0 - 2 Mbyte 0 1 : 2 - 4 Mbyte 1 0 : 4 - 6 Mbyte 1 1 : 6 - 8 Mbyte
2,3	EMS block for page 2 : Bit3 Bit2 EMS memory block (A22 A21) 0 0 : 0 - 2 Mbyte 0 1 : 2 - 4 Mbyte 1 0 : 4 - 6 Mbyte 1 1 : 6 - 8 Mbyte
4,5	EMS block for page 1 : Bit5 Bit4 EMS memory block (A22 A21) 0 0 : 0 - 2 Mbyte 0 1 : 2 - 4 Mbyte 1 0 : 4 - 6 Mbyte 1 1 : 6 - 8 Mbyte
6,7	EMS block for page 0 : Bit7 Bit6 EMS memory block (A22 A21) 0 0 : 0 - 2 Mbyte 0 1 : 2 - 4 Mbyte 1 0 : 4 - 6 Mbyte 1 1 : 6 - 8 Mbyte

R2C : (Index address 6FH)

Bits	Function
0	Reserved.
1	CPUA20 enable.
2	RAS time-out enable.
3	Reserved.
4	EMS mapper enable
5-7	Size of EMS memory : 0 0 0 : < 1 Mbyte 1 0 0 : 1 Mbyte 0 1 0 : 2 Mbytes 1 1 0 : 3 Mbytes 0 0 1 : 4 Mbytes 1 0 1 : 5 Mbytes 0 1 1 : 6 Mbytes 1 1 1 : 7 Mbytes

3. UM82C215 Data / Address Buffer

The UM82C215 Data/Address buffer, basically, provides the functions of buffering and latching among several buses. The 16 bit to 8 bit bus conversion is also performed by the UM82C215 when the conversion is needed. The parity checking will be performed when the UM82C215 receives data and the parity bit will be generated when the UM82C215 sends data out. The major functions of the UM82C215 are address buffering and latching, data buffering and latching, bus conversion, parity checking and parity bit generation.



3.1 Address Buffers and Latches

The address buffering between the CPU address lines A16-A1 and the X bus address lines XA16-XA1 is provided by the UM82C215. The IALE is used to latch the CPU address lines.

3.2 Data Buffers and Latches

The UM82C215 provides the buffering between the CPU data bus D15-D0 and the memory data bus MD15-MD0. The memory data bus can be latched. However, the latch enable is controlled by the DRD, ACEN, and action codes.

3.3 Bus Conversion

When the 16 bit CPU accesses data from/to 8 bit devices, the function of bus conversion is needed. The UM82C215 provides the bus conversion for the CPU 80286 to read/write data from/to 8 bit devices. The bus conversion for DMA cycles is also provided. All of these conversions are controlled by the action codes.

Table 3.1 Bus Conversion

AC1	AC0	Cycle	Operation
0	0	CPU	Write - 16 Bits
0	1	CPU	Read - 16 Bits
0	0	CPU	Write - 8 Bits (low byte)
0	1	CPU	Read - 8 Bits (low byte)
1	0	CPU	Write - 8 Bits (high byte)
1	1	CPU	Read - 8 Bits (high byte)
1	0	DMA/MASTER	Write - 8 Bits (high byte)
1	1	DMA/MASTER	Read - 8 Bits (high byte)

3.4 Parity Checking and Generation

The UM82C215 checks the parity for each data byte read from local memory. If any parity error is detected, the UM82C215 then activates PARERR. In addition, the UM82C215 generates a parity bit for each data byte which is going to be written to local memory.

1. General Description

The UMC's MORTAR (286AT) Chip Set UM82C230 series provides an economic alternative for building a reliable IBM PC/AT compatible system.

A commercial 12MHZ/O wait state, 4MByte main memory system and math-coprocessor can be easily built by using 3 VLSIs, 8 logic components plus memory and processor.

2. Features

- Fully PC/AT-Compatible for 10MHz and 12MHz systems.
- Guaranteed zero wait state for 80ns DRAMs at 12MHz and one wait state for 120ns DRAMs at 12.5MHz.
- Supports up to 4MB local memory on board.
- Remaps 384KB of top of system local memory space.
- Supports 1M/256K SIM module.
- Supports 12MHz operation with one wait state for 200ns EPROM.
- Commercially available BIOS (Phoenix/Award/AMI) applicable.
- Easy design system board, three VLSI chips and eight TTLs configure all the logic.
- Landmark speed=15.9MHz operating at 12MHz, 16.5MHz operating at 12.5MHz.

The UM82C230 MORTAR chipset consists of the UM82C231 System/Memory Controller, the UM82C232 Data/Address Buffer and the UM82C206 Integrated Peripherals Controller (IPC).

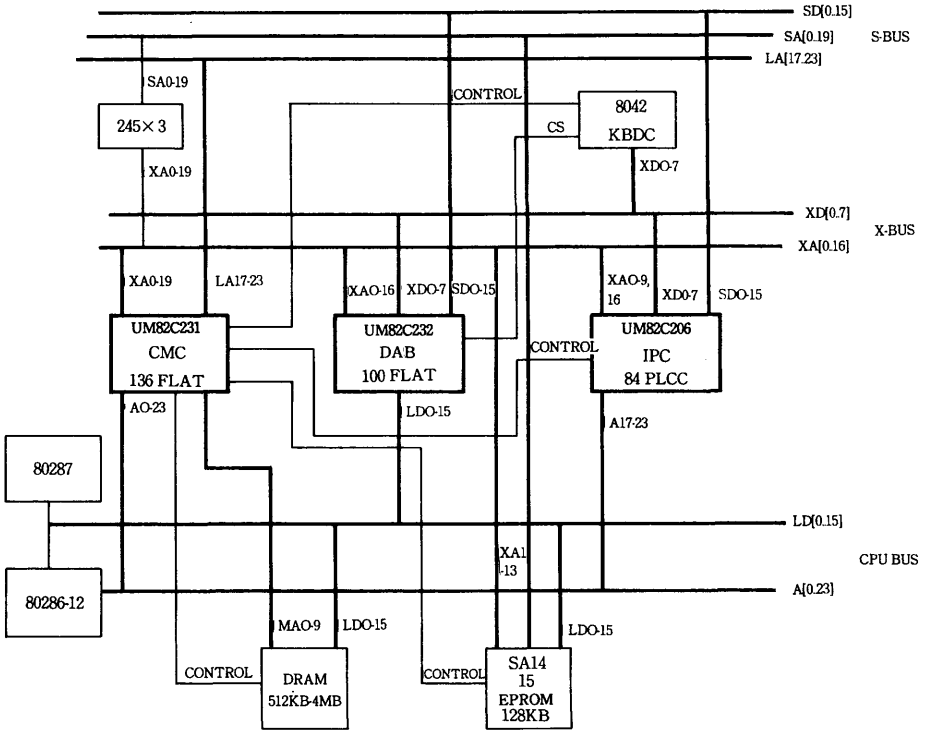
As shown in the System Block Diagram, there are three data buses: local data bus, AT data bus and peripheral data (XD) bus. The local DRAM, EPROM and Numerical Processor are located on the local data bus. The UM82C206 and 8042 Keyboard Controller sit on the XD bus. The AT data bus was driven by the UM82C232 directly which conveys the data to/from the AT Channel Adaptors.

The address bus architecture is also very simple; local CPU address bus, local DRAM address bus (MA), peripheral address bus (XA) and AT address bus. The local address bus is shared between CPU, UM82C231 and UM82C206. The MA bus is used by the local DRAM only. Most of the system board devices are attached to the XA bus, like UM82C232, UM82C206, ROMs and 8042. Some AT address lines are driven by the UM82C231 or UM82C232 directly; the others are buffered.

The UM82C231 provides synchronization and control signals for all buses. The UM82C231 also distinguishes if the current cycle is local memory cycle. Upon detecting that it is a local DRAM cycle, no AT control signals are sent out to the AT channel. The UM82C231 is based on the memory configurations to complete the current cycle with fastest response. If the cycle is AT cycle, the UM82C231 sends out the control signals sequentially which are then used by the adaptors or system board devices to receive the write data or to send the fetched data. Then, depending on the status signals sent back by the adaptors or system board devices, the UM82C231 determines which kind of AT cycles to perform: 8-bit, 16-bit, bus conversion, wait state insert, or 0 wait state cycle.

The UM82C232 Data/Address buffer provides the buffering and latching between the CPU local data bus, AT bus and XD bus. The parity bit generation and parity bit checking logic resides in the UM82C232 also. During DMA cycles, the UM82C232 latches the address from XD, which is sent by the UM82C206, and transfers to XA bus.

MORTAR Chip Set System Diagram



Required IC List :

80286	× 1	74E74	× 1
UM82C231	× 1	74LS08	× 1
UM82C232	× 1	7407	× 1
UM82C206	× 1	14069	× 1
27256	× 2	74ALS04	× 1
8042	× 1	74ALS245	× 3

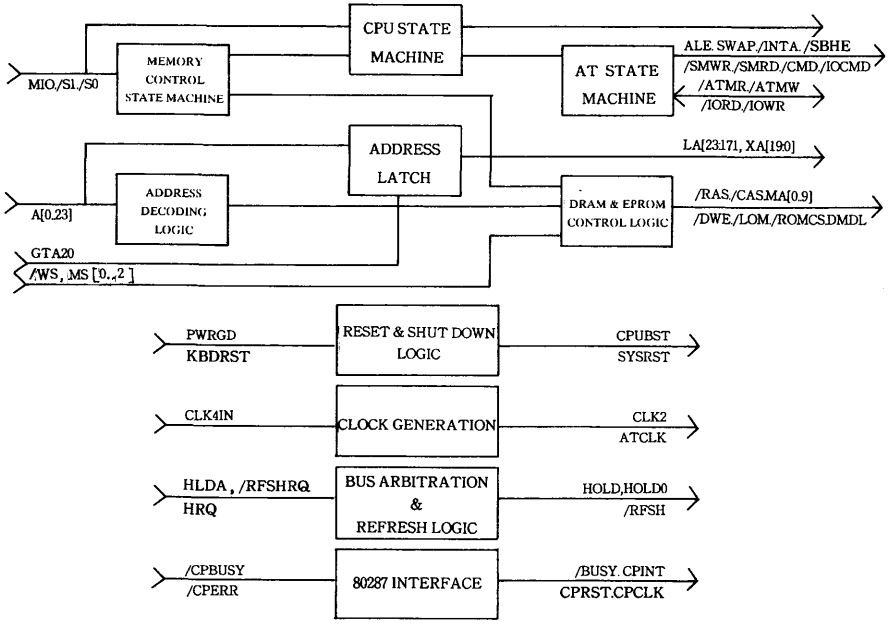
1. General Decription

The UM82C231 is a system/memory controller. It performs the CPU interface, AT system bus interface and memory interface functions.

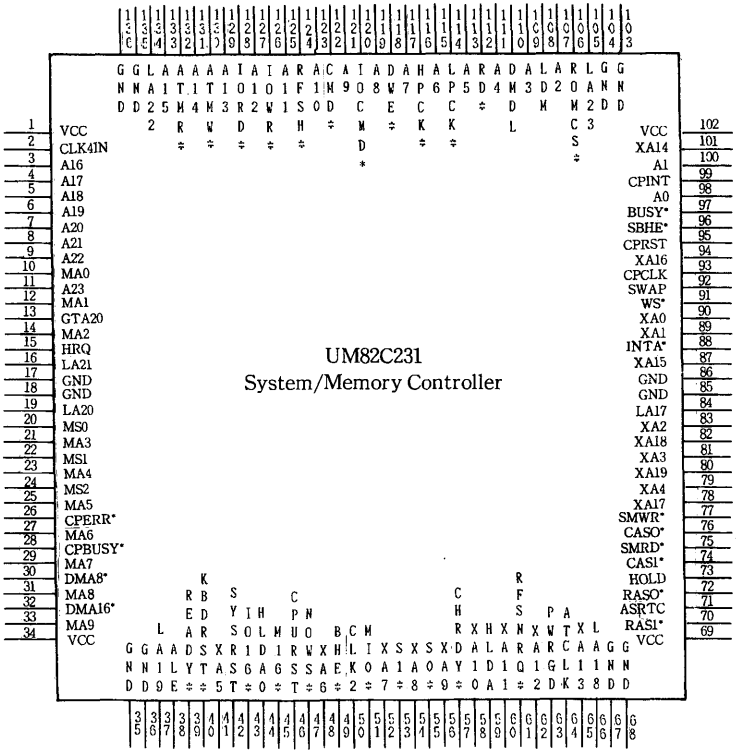
2. Features

- CPU interface and bus control.
- PC/AT expansion bus interface.
- Clock generation.
- Numericl processor 80287 interface.
- Peripheral chip interface.
- Refresh and DMA logic.
- Reset and shut down logic.
- Supports 64K、256K and 1M DRAM
- Supports up to 4M Bytes on board memory.
- Advanced 1.2μ m CMOS technology.
- TTL compatible inputs.
- 136 pin flat package.

3. UM82C231 Block Diagram



4.UM82C231 Pin Configuration



5. 82C231 Pin Description

Pin Name.	Pin Type	Pin No.	Description
A(23:0)	I	11,9,8, 7,6, 5,4, 3,133, 131, 129, 127, 125, 123, 121, 119, 117, 115, 113, 111, 109, 107, 100,98,	Local address lines from CPU; A(23:17) also connected to 82C206 to represent the DMA page address during DMA cycles.
LA(23:17)	B	105,134, 16, 19,37, 66,84	AT bus unlatched address bus Bit 23 - Bit 17; These pins are outputs during CPU or DMA cycles and become inputs during REFRESH or MASTER cycles. They have 24 ma current sinking cabability.
XA(19:17)	TO	80,82,78	AT bus latched address bus Bit 19 - Bit 17. They are activated during CPU and DMA cycles; tri-stated otherwise.
XA(16:1)	B	94, 87, 101, 65, 62, 60, 58, 56, 54, 52, 48, 41, 79,81,83, 89	AT bus latched address bus Bit 16; It is an output pin for CPU or REFRESH cycles and becomes input during DMA or MASTER cycles. XA15 and XA14 have 24 ma current. sinking capability.
XA0	B	90	AT bus latched address bus Bit 0; It is an output pin for CPU, REFRESH or 16-bit DMA cycles and becomes input during 8-bit DMA or MASTER cycles.
GTA20	I	13	AT bus unlatched address bit 20 enable control; the logic low of this signal will force LA20 stay low during CPU cycles.

Pin Name.	Pin Type	Pin No.	Description
M-I/O	I	51	Memory or I/O cycle status signal from CPU.
BHE*	I	49	Byte high enable signal from CPU to indicate that high byte accessing is required for the current cycle.
SBHE*	B	96	System Byte high enable to AT bus through buffer; it is output normally and becomes input when MASTER has the AT bus.
CLK4IN	I	2	OSC. input; divided by two to derive CPU CLK2. This signal is also used to control DRAM access timing.
CLK2	0	50	OSC. output; used as the CPU CLK2 source.
ATCLK	0	64	AT system clock connected to AT bus through buffer. This clock output synchronized with CLK2 and generated from CLK4IN/6.
SO*	I	55	CPU status line 0; normally it indicates that the current cycle is write cycle.
S1*	I	53	CPU status line 1; normally it indicates that the current cycle is read cycle.
INTA*	I	88	Interrupt acknowledge cycle indication; when S0*, S1* and M-I/O are monitored low, this signal will be activated.
READY*	O	39	CPU ready signal; CPU samples this signal at the end of every Tc state. The current cycle will be terminated if sampled low.
HLDA	I	59	Hold acknowledge input from CPU; CPU will relinquish the local buses when this signal is active.

Pin Name.	Pin Type	Pin No.	Description
HRQ	I	15	DMA or MASTER cycle request from 82C206.
RFSHRQ*	I	61	Refresh request signal from 82C206's timer 1 output. normally this signal is activated around 15.6 micro second.
HOLD	O	73	Hold request to CPU; either HRQ or RFSHRQ* is arbitrated. Hold will be generated to ask for the buses.
HLDAO	O	44	DMA or MASTER cycle acknowledge signal to 82C206; if HRQ is arbitrated and CPU relinquishes the buses, HLDAO is activated to notice that the DMA controller or MASTER can issue the control signals to perfrom the transactions.
RFSH*	B	124	Refresh cycle indication; it is an output pin normally and become input pin during MASTER cycles.
PWRGD	I	63	Power good or bad indication; if this signal is low, the system will stay at the reset condition.
KBDRST*	I	40	CPU reset request from keyboard controller; when detect a low pulse of this signal, 82C231 will reset CPU.
CPURST	O	46	CPU reset; for both PWRGD and KBDRST* are low, CPURST will be activated.
SYSRST	O	42	System reset; for PWRGD is low Sysrst will be activated.
CPBUSY*	I	28	Co-processor busy signal; which indicates co-processor is accessed.

Pin Name.	Pin Type	Pin No.	Description
CPERR*	I	26	Co-processor error signal; indicates co-processor's accessing has error.
BUSY*	O	97	Busy signal to CPU; which indicates that co-processor is busy or has error.
CPINT	O	99	Co-processor interrupt; which indicates that the co-processor has error and the system software has to do somthing.
CPRST	O	95	Co-processor reset; a system reset or a write to IO address F1 hex will trigger this signal active.
CPCLK	O	93	CLK4IN/3 clock output has 33% duty cycle.
DMA8*	I	30	8-bit DMA cycle indication.
DMA16*	I	32	16-bit DMA cycle indication.
CHRDY*	I	57	Channel ready signal from AT bus; 82C231 monitors this signal to determine that if the accessed device requires more wait states to complete the transaction.
NOWS*	I	47	No wait state signal from AT bus; 82C231 monitors this signal to terminate the current AT cycle immediately.
M16*	I	45	Memory data size 16-bit signal from AT bus; 82C231 monitors this signal to determine the memory slave's data size.
IO16*	I	43	IO data size 16-bit signal from AT bus; 82C231 monitors this signal to determine the IO slave's data size.
ALE	O	38	AT bus address latch enable; 82C231 issues this signal to start the AT cycle.

Pin Name.	Pin Type	Pin No.	Description
RAS*(1:0)	O	70,72	Row address strobes for the local memory; used as bank select.
CAS*(1:0)	O	74,76	Column address strobe for the local memory; used as byte enable.
DWE*	O	118	DRAM write or read control signal.
ROMCS*	O	106	BIOS ROM output enable; this signal is activated when the BIOS area either from 0E0000-0FFFFF or FE0000-FFFFFF address range is accessed.
RD*	O	112	Read cycle status signal for CPU, DMA or MASTER cycle; either IO or memory read in CPU or MASTER cycle, and the the memory read in DMA cycle this signal is activated.
DMDL	O	110	Local DRAM read data latch enable; this signal is used to latch the data and parity bits read from local DRAM by the 82C232.
HPCK*	O	116	High byte parity checking enable; 82C231 issues this signal if to check high byte read data is required.
LPCK*	O	114	Low byte parity checking enable; 82C231 issues this signal if to check low byte read data is required.
LDM*	O	108	Local DRAM accessed indication; when local DRAM is accessed by the bus controllers, 82C231 enables this signal.
ASRTC	O	71	Read Time clock address strobe.
WS*	I	91	Local DRAM wait state control; a low input, 82C231 will insert one wait state.

Pin Name.	Pin Type	Pin No.	Description
ATMW*	B	130	AT bus memory write command signal; it is an output pin during CPU cycle and becomes input during DMA and MASTER cycles.
ATMR*	B	132	AT bus memory read command signal; it is an output pin during CPU and REFRESH cycle and becomes input during DMA and MASTER cycles.
SMWR*	O	77	AT bus memory write command signal when the memory access address is below one mega byte.
SMRD*	O	75	AT bus memory read command signal when the memory access address is below one mega byte.
IOWR*	B	126	AT bus IO write command signal; it is an output pin during CPU cycle and becomes input during DMA and MASTER cycles.
IORD*	B	128	AT bus IO read command signal; it is an output pin during CPU cycle and becomes input during DMA and MASTER cycles.
SWAP	O	92	High byte data and low byte data swapping control signal; the 82C231 monitors the transaction data size and the slave device's data width, then enable this signal if required.
CMD*	O	122	Command signal; for every AT cycle's read or write cycle this signal will be active and has the same timing as read or write command.
IOCMD*	O	120	IO command signal; for every AT IO cycle's read or write cycle this signal will be active.
MA(9: 0)	O	33, 31, 29, 27, 25, 23, 21,14,12, 10	Multiplexed DRAM row and column address for the local memory

Pin Name.	Pin Type	Pin No.	Description
MS(2:0)	I	24,22,20	Local DRAM memory configuration select.
VCC		1,34,69 102	
GND		17,18,35 36, 67,68 85,86, 103, 104, 135 136	
Total Pin		136	

6. Functional Description

The UM82C231 Bus & Memory Controller consists of the following functional sub-modules:

* Reset and Shut Down Logic.

* Clock Generation.

* CPU State Machine, AT Bus State Machine and Memory Control State Machine.

* Bus Abitration Logic, DMA/Master and Refresh Logic.

* Numeric Processor Interface.

* System Control Logic.

* Address Decoding Logic.

* DRAM & EPROM Control Logic.

Overview

The UM82C231 performs the CPU interface, AT system bus interface and the memory control functions. The various functional modules are discussed in this section.

6.1 Reset and Shut Down Logic

Two reset inputs PWRGD and KBDRST# are provided on the UM82C231 chip. PWRGD is the Power Good signal from the power supply. When PWRGD is low, the UM82C231 asserts CPURST for CPU reset and SYSRST for system reset. KBDRST# is generated from the 8042 keyboard controller when a CPU reset is required. CPURST is also activated by the UM82C231 when a shut down condition is detected from CPU status. Both CPURST and SYSRST are asserted for at least 16 CLK2 cycles and are synchronized with respect to CLK2 to meet the setup and hold time requirements of the 80286 CPU.

6.2 Clock Generation

The UM82C231 provides two synchronous clocks CLK2 and ATCLK for the system. There is only one input clock CLK4IN, driven from a TTL crystal oscillator, running at twice of the CPU clock frequency. ATCLK is also derived from CLK4IN at 1/3 of the CPU clock frequency.

6.3 CPU, AT Bus and Memory Control State Machine.

In order to achieve maximum performance of the 80286 CPU and maintain 100% IBM PC/AT compatibity, it is desirable to run the local memory at the rated maximum CPU frequency and the AT bus at a slower clock frequency. The two state machines still maintain a synchronous protocol.

6.3.1 CPU State Machine

Interface to the 80286 requires interpretation of the status lines S0#, S1# and M-I/O from CPU during phase 1 of TS and generation of READY# during TC to the CPU upon completion of the cycle. A(23:0) will be latched during phase 2 of TS for internal use. Address Decoding Logic then activates Memory Control State Machine for a local memory cycle or AT State Machine for AT cycle. Either State Machine terminates itself and CPU State machine upon completion of its function. READY# will be sent out to the 80286 CPU to finish the cycle.

6.3.2 AT Bus State Machine

The At Bus State Machine gains control when Address Decoding Logic decodes a non-local memory cycle. It uses BCLK which is twice the frequency of AT system clock ATCLK, it also performs the necessary synchronization of control and status signals between the AT bus and the processor. The UM82C231 supports 8 and 16 bit memory or I/O devices located on the AT bus.

AT bus cycle is initiated by asserting ALE in AT-TS 1 state. On the trailing edge of ALE, M16# is sampled for a memory cycle to determine the bus size.

It then enters AT-TC state and provides the command signal. For an I/O cycle, IO16* is sampled after the trailing edge of ALE till the end of the command. Typically, the wait state for an AT 8/16 bit transaction is 5/3 respectively. The command cycle is extended when CHRDY is detected inactive, or is terminated when zero wait state request signal NOW# from AT bus is active. Upon expiration of the wait states, AT State Machine terminates itself and passes internal READY to CPU State Machine for outputting synchronous READY# to the 80286.

6.3.3 Memory Control State Machine

Address Decoding Logic activates Memory Control State Machine when local memory is to be accessed. Memory Control State Machine initiates memory interfacing signals by adapting the configuration strap pin MS(2:0) and information from Address Decoding Logic. The definitions of MS(2:0) are given in the following table.

MS2	MS2	MS0	Bank0	Bank1	Total Memory
0	0	0	256k	-	512k
0	0	1	256k	64k	640k
0	1	0	256k	256k	1Meg
0	1	1	1M	-	2Meg
1	1	1	1M	1M	4Meg
1	0	X	Not Valid		
1	1	0	Not Valid		

6.4 Bus Arbitration Logic, DMA/Master and Refresh Logic

The UM82C231 provides arbitration between the CPU, DRAM refresh logic and DMA/Master devices. It handles HRQ and RESHRQ by generating HOLD request to the CPU. CPU will respond to an active HOLD signal by asserting HLDA and placing most of its output and I/O pins in a high impedance state after completing its current bus cycle. After the CPU relinquishes the bus, the UM82C231 responds by issuing RFSH# or HLDA0 depending on the requesting device.

The arbitration between Refresh and DMA/Master is based on FIFO or first come first serve. However, RFSHRQ will be internally latched and served immediately after DMA/Master finishes its request if RFSHRQ is queued behind HRQ. HRQ has to remain active to be served if RFSHRQ comes first.

During a refresh cycle, refresh address is put out on XA0-XA9 and MA0-MA9 address lines, RFSH# and LDM# are asserted, SMRD# is active 2 SYSCLK after RFSH# is active and RAS#(1: 0) are asserted to refresh DRAMS accordingly.

DMA and Bus Master share the same request pin HRQ. After the UM82C231 receives HRQ it asserts HOLD request to the CPU. Upon finishing the current cycle, the CPU relinquishes the bus by asserting HLDA. The UM82C231 issues HLDAO to the requesting device to start gaining control of the bus. During an active HLDAO period the only way to distinguish between DMA and Bus Master request is to monitor the DMA8# and DMA16# signals. DMA8#/DMA16# active indicates an 8-bit/16bit DMA transfer, while both inactive means a Master cycle.

6.5 Numeric Processor Interface

Incorporated in the UM82C231 is the circuitry to interface an 80287 Numeric Coprocessor to 80286. The circuitry handles the decoding required for selecting and resetting the Numeric Coprocessor, handling CPBUSY# and CPERR# signals from the 80287 to the CPU, and generating interrupt signals for error handling.

While executing a task, the 80287 issues a CPBUSY# signal to the UM82C231 and is passed to the CPU as BUSY#. If during this busy period, a numeric coprocessor error CPERR# occurs it results in an internal latching of the BUSY# output and assertion of IRQ13 for a NP exception request. Latched BUSY# stays active until cleared by an I/O write cycle to address 0F0H or 0F1H. IRQ13 is cleared only when CPERR# from 80287. The 80287 is reset through the CPRST output, which can be activated by a system reset or by performing a write operation to I/O port 0F1H.

The 80287 can operate either directly from the CPU clock or with a 33% duty cycle 1/3 the frequency of the CPU clock. The UM82C231 provides both clock, CLK2 and CPCLK, to the 80287.

6.6 System Control Logic

The UM82C231 activates bus swapping control signal SWAP to the UM82C232 to guide the data bus flow during AT bus accessing and high low data byte swapping is required. Other control signals ALE, ATMW#, ATMW#, ATMR#, SMWR#, SMRD#, IOWR#, IORD# , CMD#, IOCMD# and RD# are provided for AT bus interfacing and controlling.

6.7 DRAM & EPROM Control Logic

The DRAM and EPROM control logic in the UM82C231 is responsible for the generation of the RAS#, CAS# and DWE# signals for DRAM accessed and ROMCS# for EPROM accesses. This sub-module also generates READY# to the CPU upon completion of the desired local memory operation. The appropriate number of wait states are inserted, as programmed by strap pins externally.

7. Electrical Characteristics (Vcc=4.75~5.25V, TA=0°C-70°C)

7.1 DC Characteristics

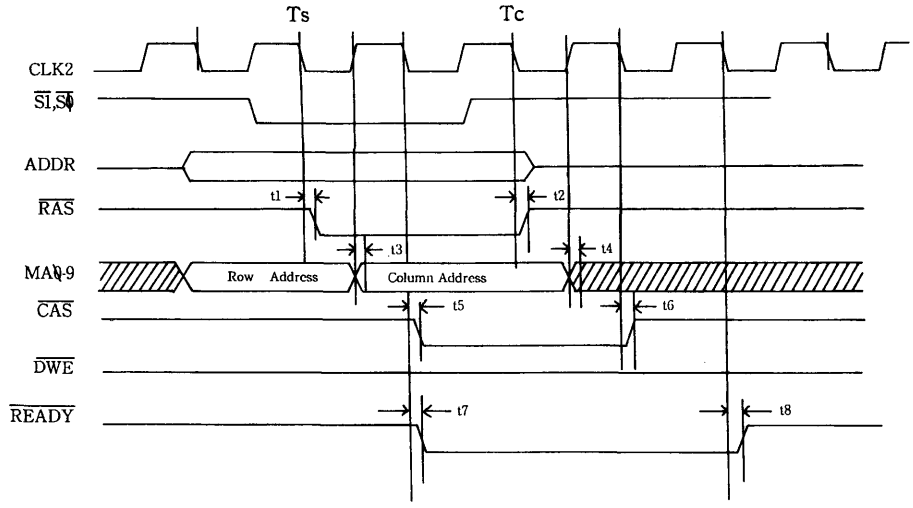
Parameters	Symbol	Min.	Max.	Units
Input Low Voltage	Vil	-	0.8	V
Input High Voltage	Vih	2.0	-	V
Output Low Voltage	Vol	-	0.45	V
Output High Voltage	Voh	2.4V	-	V
Input Current	Iil	-	+-10	ua
Power Supply Current	Icc	-	100-	ma
Output High-Z Current	Ioz	-	+-10	ua
Standby Power Supply Current	Iccsb	-	1	ma

7.2 AC Characteristics

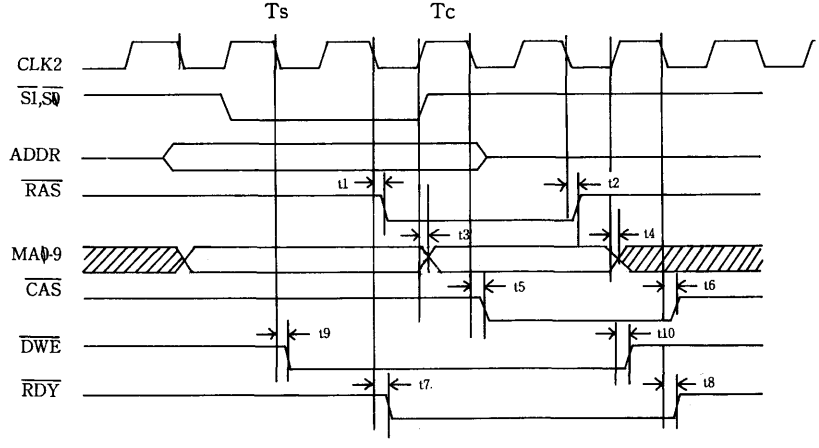
Symbol	Description	MIN	TYP	MAX	UNIT
t1	$\overline{RAS}$ active from CLK2 ↓	8	14	19	ns
t2	$\overline{RAS}$ inactive from CLK2 ↓	10	19	25	ns
t3	Column address valid from CLK2 ↑	8	15	20	ns
t4	Column address invalid from CLK2 ↑	9	18	24	ns
t5	$\overline{CAS}$ active from CLK2 ↓	8	14	19	ns
t6	$\overline{CAS}$ inactive from CLK2 ↓	10	19	25	ns
t7	$\overline{RDY}$ active from CLK2 ↓	11	20	30	ns
t8	$\overline{RDY}$ inactive from CLK2 ↓	13	22	32	ns
t9	$\overline{WE}$ active from CLK2 ↓	8	15	20	ns
t10	$\overline{WE}$ inactive from CLK2 ↑	9	16	21	ns
t11	$\overline{ROMCS}$ active from CLK2 ↓	8	15	20	ns
t12	$\overline{ROMCS}$ inactive from CLK2 ↓	9	16	21	ns
t13	$\overline{RAS}$ active from $\overline{ATMR}$ ↓	6	10	17	ns
t14	$\overline{RAS}$ inactive from $\overline{ATMR}$ ↑	7	12	19	ns
t15	ROW address hold time from $\overline{RAS}$ ↓		1		CLK2
t16	Column address hold time from $\overline{ATMR}$ ↑	6	10	17	ns
t17	Column address setup time from $\overline{CAS}$ ↓	0.5		1	CLK2
t18	$\overline{CAS}$ inactive from $\overline{ATMR}$ ↑	6	10	17	ns

Symbol	Description	MIN	TYP	MAX	UNIT
t19	ALE active delay from ATCLK ↓	0	4	8	ns
t20	ALE inactive delay from ATCLK ↓	0	4	8	ns
t21	COMMAND active delay from ATCLK ↓	0	4	8	ns
t22	COMMAND inactive delay from ATCLK ↓	0	4	8	ns
t23	$\overline{M16}$ set-up time to ATCLK ↑	10			ns
t24	$\overline{M16}$ hold time to ATCLK ↑	4			ns
t25	$\overline{IO16}$ set-up time to ATCLK ↓	10			ns
t26	$\overline{IO16}$ hold time to ATCLK ↓	8			ns
t27	$\overline{NOWS}$ set-yp time to ATCLK ↑	8			ns
t28	$\overline{NOWS}$ hold time to ATCLK ↑	10			ns
t29	IOCHROY set-yp time to ATCLK ↑	10			ns
t30	IOCHROY hold time to ATCLK ↑	4	6	12	ns
t31	CPURST active delay from CLK20 ↓	2	6	16	ns
t32	CPURST inactive delay from CLK20 ↓	2	6	12	ns
t33	SYSRST active delay from CLK20 ↓	2	6	16	ns
t34	SYSRST inactive delay from CLK20 ↓	2			ns
t35	$\overline{READY}$ input set up from CLK20 ↓	12			ns
t36	$\overline{READY}$ input hold from CLK20 ↓	8			ns
t37	HOLD active delay from ATCLK ↑	2	4	8	ns

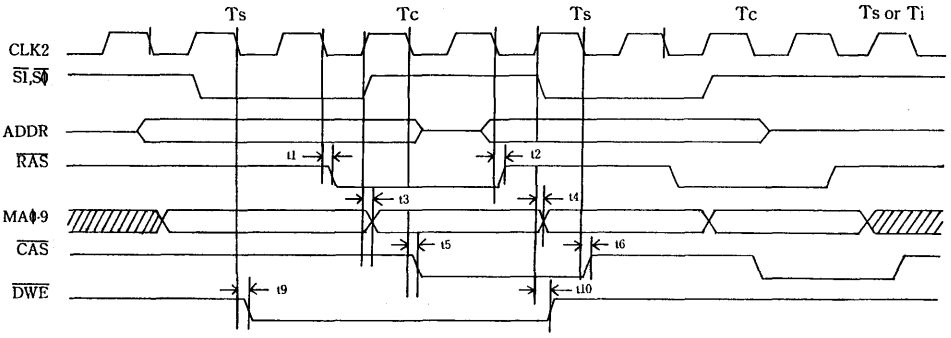
Symbol	Description	MIN	TYP	MAX	UNIT
t38	HOLD inactive delay from ATCLK ↓	2	4	8	ns
t39	$\overline{\text{RFSH}}$ delay from HLDAI	3	7	14	ns
t40	$\overline{\text{RFSH}}$ inactive delsy from ATCLK ↑	2	4	8	ns
t41	$\overline{\text{ATMR}}$ active delay from ATCLK ↑	1	5	9	ns
t42	$\overline{\text{ATMR}}$ inactive delay from ATCLK ↓	2	4	6	ns
t43	HRQ set-yp time to ATCLK ↑	10			ns
t44	HRQ hold time to ATCLK ↑	4			ns
t45	HLDAO active delay from HLDAI	5	9	18	ns
t46	HLDAO inactive delay from HLDAI	5	10	20	ns
t47	overlap of $\overline{\text{CPBUSY}}$ & $\overline{\text{CPERR}}$	8			ns
t48	$\overline{\text{CPBUSY}}$ active pulse	12			ns
t49	IRQ13 active delay from $\overline{\text{CPBUSY}}$, $\overline{\text{CPERR}}$	7	12	16	ns
t50	IRQ13 inactive delay from $\overline{\text{CPERR}}$	3	7	11	ns
t51	$\overline{\text{BUSY}}$ active delay from $\overline{\text{CPBUSY}}$ ↓	4	8	16	ns
t52	$\overline{\text{BUSY}}$ inactive delay from $\overline{\text{CPBUSY}}$ ↑	4	8	16	ns
t53	CPRST active delay from $\overline{\text{ATIOW}}$ ↓	2	5	10	ns
t54	CPRST inactive delay from $\overline{\text{ATIOW}}$ ↑	2	5	10	ns
t55	REFRESH address valid from $\overline{\text{REF}}$ ↓	7	10	15	ns



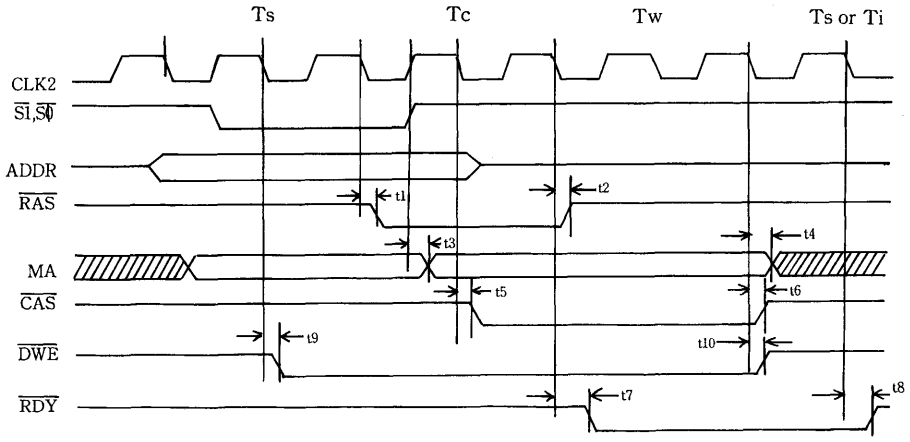
0 W.S. Read



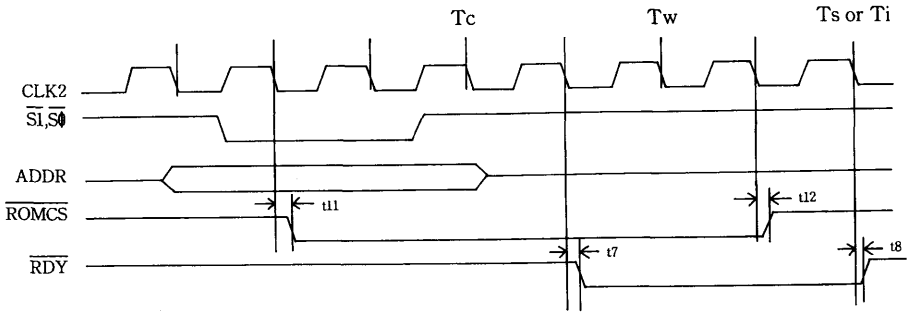
0 W.S. Write



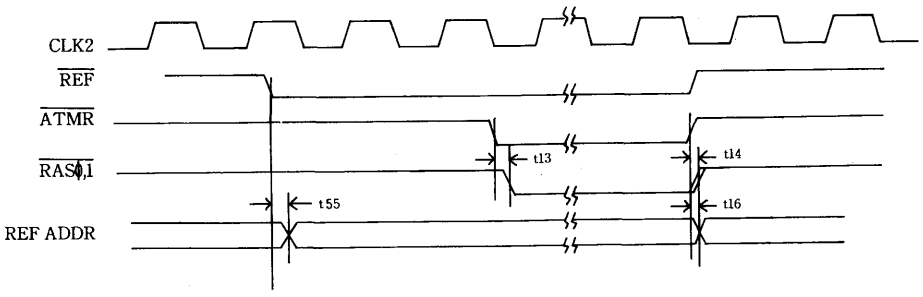
Read after Write 0 W.S.



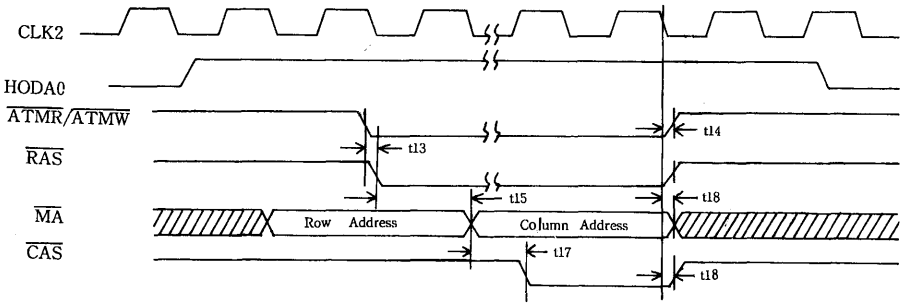
1 W.S. Read/Write



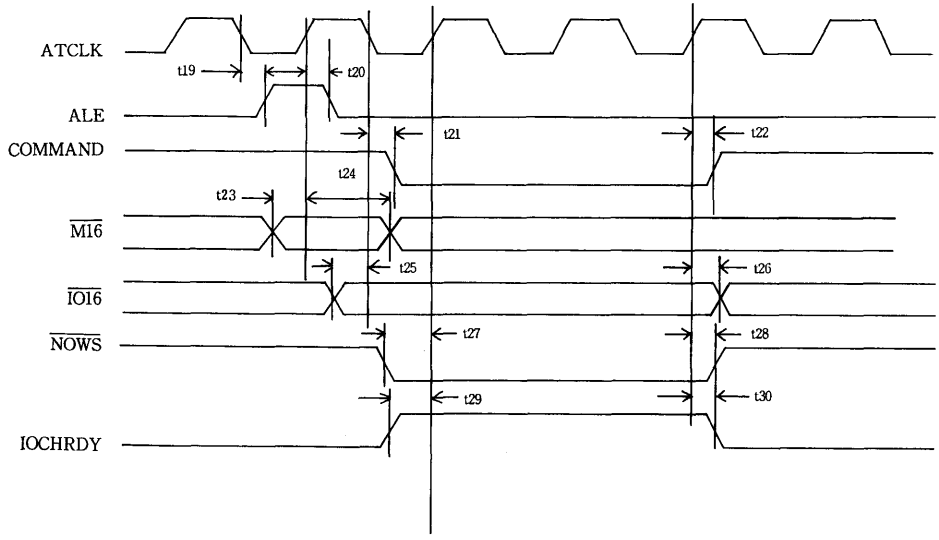
ROM Cycle



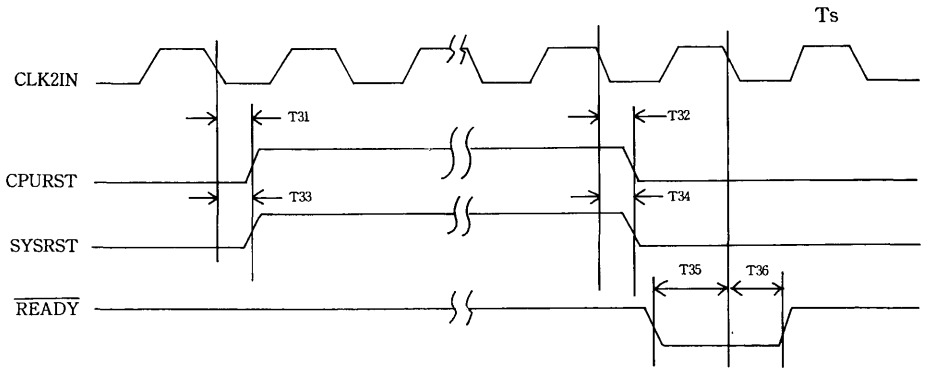
Refresh Cycle



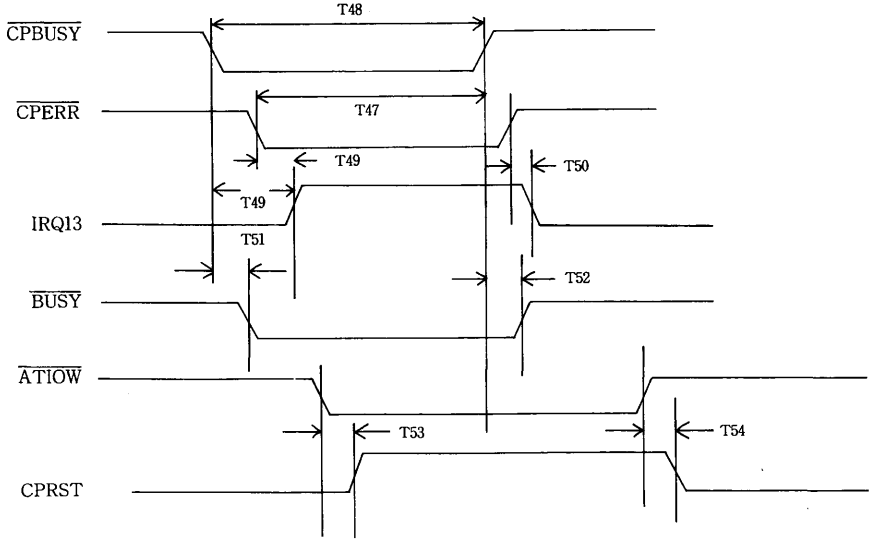
DMA Cycle



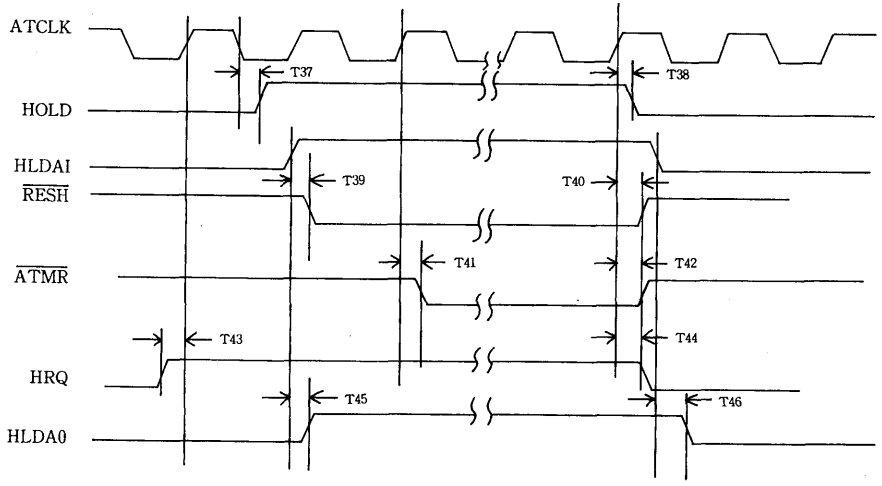
AT BUS TIMING



RESET & $\overline{\text{READY}}$ TIMING



COPROCESSOR SIGNALS TIMING

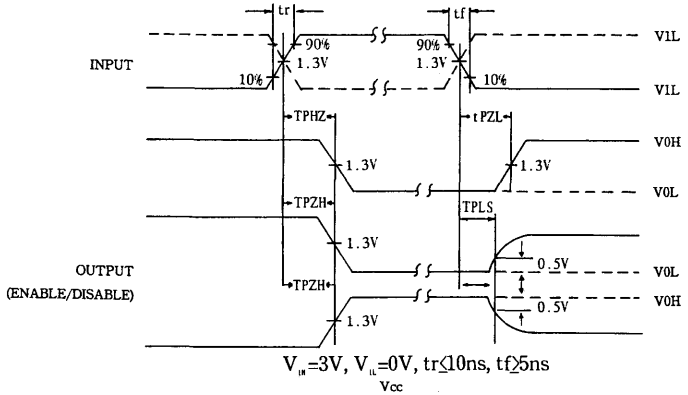


ARBITRATION SIGNALS' TIMING

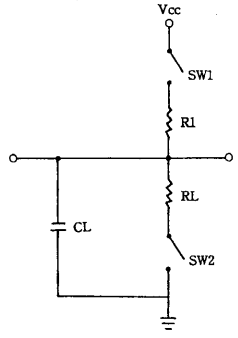
7.3 Testing Conditions

Load Circuit Measurerrient Conditions

Parameter	Output Type	Symbol	CL(pF)	Rt(Ω)	RL(Ω)	SW1	SW2
Propagation Delay Time	Totem pole 3-state Bidirectional	t_{PLH} t_{PHL}	50	—	1.0K	OFF	ON
Propagation Delay Time	Open drain or Open Collector	t_{PLH} t_{PHL}	50	0.5K	—	ON	OFF
Disable Time	3-state Bidirectional	t_{PLZ} t_{PHZ}	5	0.5K	1.0K	ON OFF	ON
Enable Time	3-state Bidirectional	t_{PLZ} t_{PHZ}	50	—	1.0K	ON OFF	ON ON



V_{IH}=3V, V_{IL}=0V, tr≤10ns, tf≤5ns



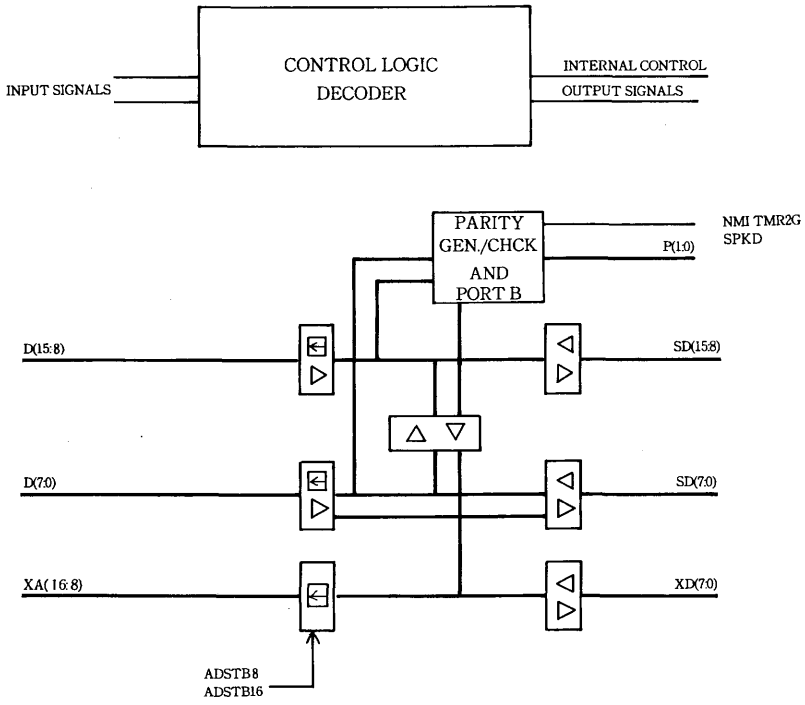
1. General Description:

The UM 82C232 is a data buffer. It is an interface between CPU data bus, system data bus and peripheral data bus.

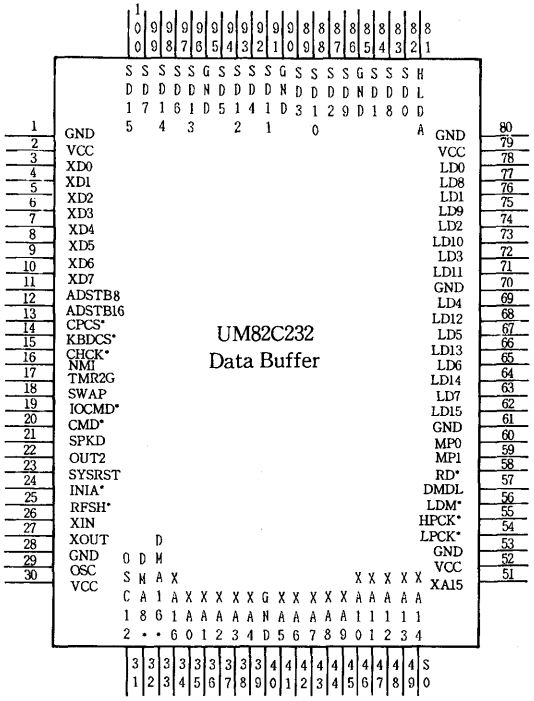
2. Features:

- 16-bit data bus buffer
- 16-bit or 8 bit data bus buffer for PC/AT bus
- 8-bit I/O port data bus buffer
- Word swap logic
- Advanced 1.2μ mCMOS Techonoloy
- 100 pin Flat Package

3. UM82C232 Block Diagram



4.UM82C232 Pin Configuration



5. Functional Description

5.1 Data Buffers and Latches

The UM82C232 provides the buffering between the CPU data bus and the AT data bus. The D(15:0) has 6ma driving capability. The SD(15:0) can drive the AT data bus directly because of 24ma driving capability. The UM82C232 also latches the read data from the SD bus during CPU AT cycles. This causes the bus conversion cycle and READ to command to terminate earlier than the CPU sampling data.

The latch enable signals for read data from SD(15:0) are controlled by the CMD* and SWAP signals.

The direction of the data buffers is determined by the RD*, LDM*, HLDA, DMA8* and DMA16* signals. Also, the D(15:0) are forced to become input when 80287 is accessed.

5.2 Bus Swapping Circuit

The UM82C232 supports data swapping when the 80286 reads from or writes to 8-bit devices. It also supports the high byte and low byte transition between SD bus during 8-bit DMA cycles.

The following table describes the bus transitions:

SWAP	LDM*	CYCLES	OPERATION
0	1	CPU	D(15:0)←→SD(15:0)
1	1	CPU	D(15:8)←→SD(7:0)
x	0	16-bit DMA or MASTER	D(15:0)←→SD(15:0)
0	0	8-bit DMA	D(15:0)←→SD(15:0)
1	0	8-bit DMA	D(15:8)←→SD(7:0)
1	1	8-bit DMA	D(15:8)←→SD(7:0)

5.3 Parity Generation and Checking

The UM82C232 generates an even parity bit for each two bytes during local DRAM write cycles.

During a local DRAM read cycle, the UM82C232 latches the read data and performs parity checking. If a parity error is detected, parity checking function is enabled and if NMI is not being masked, NMI will be activated.

5.4 Port B register

The UM82C232 contains a register as Port B designed for the PC/AT as shown in the following table.

Bit	R/W	Description
7	R	Local DRAM parity error status
6	R	AT bus channel check active status
5	R	Timer 2 out
4	R	Refresh toggle bit
3	R/W	Enable channel check function
2	R/W	Enable Local DRAM parity checking
1	R/W	Enable speaker
0	R/W	Timer 2 gate

5.5 NMI Generation

The NMI generation can be turned on or off through writing IOP 70 with data bit 7 equal to 0 or 1.

If NMI is not masked and parity checking and channel check function are enabled, a parity error or activated CHCK* will initiate NMI.

5.6 DMA address latch

By using ADSTB8 or ADSTB16 to latch XD(7:0), the 8-bit DMA's XA(15:8) or 16-bit DMA's XA(16:9) are latched and driven by the 82C232. The XA14 and XA15 have 24 ma driving capability.

5.7 Miscellaneous decode signals

The UM82C232 provides two decode signals,

- KBDCS* for keyboard controller
- CPCS* for co-processor

6. Pins Description

Pin Name	Pin Type	Pin No.	Description
XIN	I	26	14.3MHZ osc. input
XOUT	O	27	14.3MHZ osc. output
OSC	O	30	14.3818MHZ clock output
OSC/12	O	31	1.19MHZ clock output
D(15:0)	B	62, 64, 66, 68, 71, 73, 75, 77, 63, 65, 67, 69, 72,74,76, 78	Local data bus to/from CPU
SD(15:0)	B	100,98, 96, 93, 91, 88, 86, 83, 99, 97, 94, 92, 98,87, 84,82	AT data bus; these pins have 24 ma current sinking capability which attached to AT data bus directly.
XD(7:0)	B	10,9,8, 7,6, 5, 4,3	System board peripheral data bus.
INTA*	B	24	Interrupt acknowledge signal from 82C231; which is used to direct the interrupt vector data flow from 82C206 to CPU
MP(1:0)	B	59,60	Local DRAM parity bits; they are outputs for write cycle and become inputs during read cycle.
LDM*	I	56	Local memory accessed indication; used by 82C232 to control the data buffers enable.
HPCK*	I	55	High byte parity checking enable; used to determine if high byte parity checking is requited.

Pin Name	Pin Type	Pin No.	Description
LPCK*	I	54	Low byte parity checking enable; used to determine if Low byte parity checking is required.
DMDL	I	57	Local DRAM read data latch enable; used to latch the read data from DRAM for parity checking.
RD*	I	58	Read cycle status from 82C231; used to control the data flow direction.
SWAP	I	18	High byte data and low byte data control from 82C231; used to control the data flow direction.
CMD*	I	20	Read or write command during CPU AT cycle or MASTER cycle; used to enable the data latches inside the BUFFER.
IOCMD*	I	19	IO read or write command during CPU AT cycle or MASTER cycle ; used with RD* signal to access the IO registers inside the 82C232.
HLDA	I	81	Hold acknowledge signal from CPU to distiquish the CPU cycle and non-CPU cycle.
RFSH*	I	25	Refresh cycle indication.
ADSTB8	I	11	8-bit DMA transfer address strobe; used to latch the XD(7:0) and generate XA(15: 8) during 8-bit DMA cycle.
ADSTB16	I	12	16-bit DMA transfer address strobe; used to latch the XD(7: 0) and generate XA(16:9) during 16-bit DMA cycle.
DMA8*	I	32	8-bit DMA cycle indication; used to control the data flow directions.
DMA16*	I	33	16-bit DMA cycle indication; used to control the data flow directions.

Pin Name	Pin Type	Pin No.	Description
XA16	TO	34	System board peripheral address bus bit 16; this signal is enabled only during 16-bit DMA cycle.
XA(15:8)	B	51,50,49 48, 47,46 45,44	System board peripheral address bus bit 15 - bit 8; normally they are inputs and become outputs during DMA cycle.
XA(7:0)	I	43,42,41 39, 38,37 36,35	System board peripheral address bus bit 7 - bit 0.
CHCK*	I	15	Channel check signal from AT bus; an activated CHCK* monitored by 82C232, NMI will be issued.
NMI	O	16	Non-maskable interrupt to CPU; parity error for the data read from loacl DRAM or CHCK* activated by the channel adaptors will force 82C232 issue NMI if is is programmed to do so.
OUT2	I	22	Timer 2 output from 82C206; used to generate speaker data update IOP 61 contents.
TMR2G	O	17	Timer 2 gate control.
SPKD	O	21	Speaker data; to drive speaker.
KBDCS*	O	14	Keyboard controller chip select; decode through XA bus.
SYSRST	I	23	System reset from 82C231.
CPCS*	O	13	Co-processor chip select; decode through XA bus.
VCC		2,29,52 79	
GND		1, 28, 40 43, 61,70 80,85, 90 95	
Total pins		100	

7. Electrical Characteristics (Vcc=4.75~5.25V, TA=0°C-70°C)

7.1 DC Characteristics

Parameters	Symbol	Min.	Max.	Units
Input Low Voltage	Vil	-	0.8	V
Input High Voltage	Vih	2.0	-	V
Output Low Voltage	Vol	-	0.45	V
Output High Voltage	Voh	2.4V	-	V
Input Current	Iil	-	+- 10	ua
Power Supply Current	Icc	-	100-	ma
Output High-Z Current	Ioz	-	+- 10	ua
Standby Power Supply Current	Iccsb	-	1	ma

7.2 AC Characteristics

(Ta = 0 to 70 degree c, Vcc = 5V +- 5%)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Remark
t1	D(15:0) to SD(15:0) valid delay	11	21	30	ns	150PF
t2	D(15:0) to XD(7:0) valid delay	10	20	29	ns	75PF
t3	D(15:0) to P(1:0) valid delay	13	22	31	ns	75PF
t4	SD(15:0) to D(15:0) valid delay	9	18	28	ns	75PF
t5	SD(15:0) to XD(7:0) valid delay	9	18	28	ns	75PF
t6	SD(15:0) to P(1:0) valid delay	13	22	31	ns	75PF
t7	D(15: 0) setup time related to DMDL	0	3	5	ns	75PF
t8	D(15: 0) hold time related to DMDL	0	1	2	ns	75PF
t9	SD(15: 0) setup time related to CMD*	0	4	5.5	ns	150PF
t10	SD(15: 0) hold time related to CMD*	0	1	2	ns	150PF
t11	XD(7: 0) setup time related to CMD*	0	4	6	ns	75PF
t12	XD(7: 0) hold time related to CMD*	0	1	2	ns	75PF
t13	SD(7: 0) to SD(15: 8) delay after SWAP active	8	15	25	ns	150PF
t14	SD(7:0) to SD(15:8) invalid delay after SWAP inactive	3	9	18	ns	150PF
t15	P(1: 0) setup time related to DMDL	1	3	5	ns	75PF

Symbol	Parameter	Min.	Typ.	Max.	Unit	Remark
t16	P(1:0) hold time related to DMDL	0	1	2	ns	75PF
t17	CHCK* active to NMI active delay	3	10	18	ns	50PF
t18	HPCK* or LPCK* active to NMI active delay if parity error	8	15	23	ns	50PF
t19	XA valid to DBDCS* valid delay	10	21	32	ns	50PF
t20	XA valid to CPCS* valid delay	9	20	30	ns	50PF
t21	ADSTB8 or ADSTB16 active to XA valid during DMA cycle	10	18	28	ns	75PF
t22	SD, XD buses tri-stated after RD* invalid	5	10	20	ns	75PF
t23	SD, XD buses driven after RD* valid	6	11	15	ns	75PF
t24	D bus driven after RD* valid LDM* invalid	7	11	15	ns	75PF
t25	D bus tri-stated after RD* invalid	7	11	15	ns	75PF
t26	SD(15: 8) to SD(7: 0) delay after SWAP active	7	15	20	na	150PF
t27	SD(15:8) to SD(7:0) invalid delay after SWAP inactive	3	9	18	ns	150PF

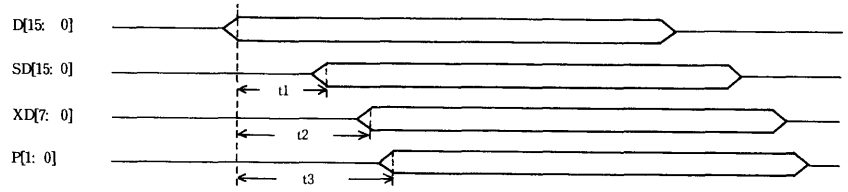


Fig.1 D[15:0] TO SD[15:0] AND P[1:0] DELAY

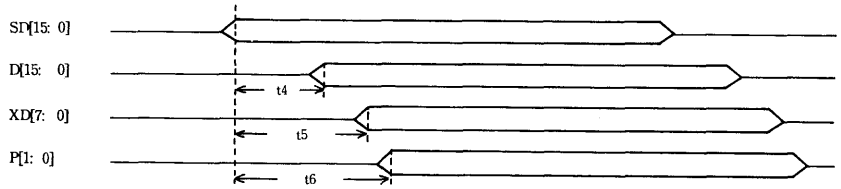


Fig.2 D[15:0] TO SD[15:0] AND P[1:0] DELAY

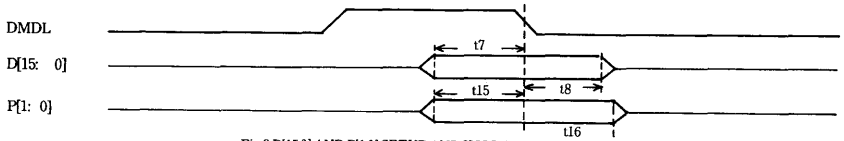


Fig.3 D[15:0] AND P[1:0] SETUP AND HOLD TIME RELATED TO DMDL

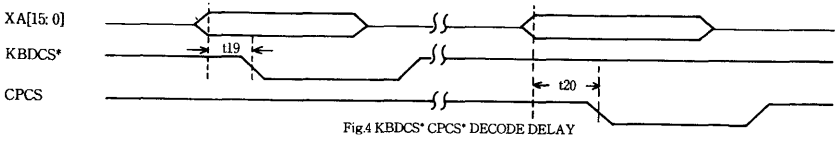


Fig.4 KBDCS* CPCS* DECODE DELAY

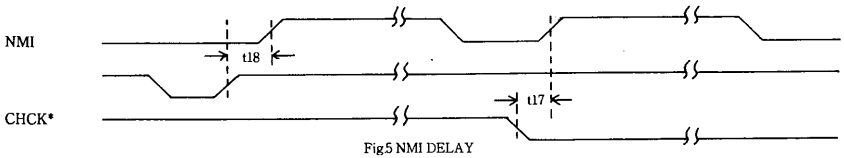


Fig.5 NMI DELAY

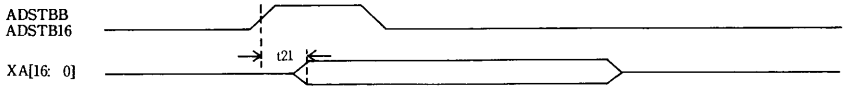


Fig.6 XA DELAY DURING DMA

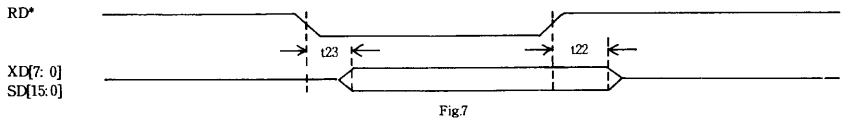


Fig.7

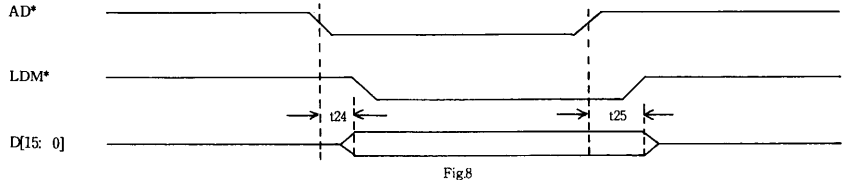


Fig.8

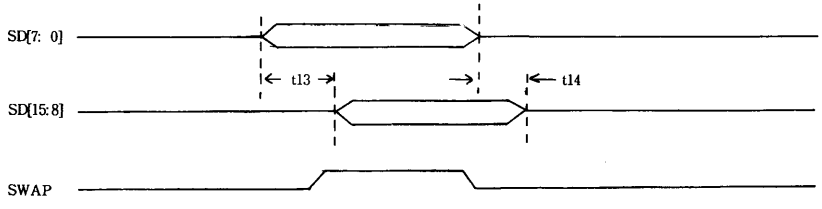


Fig. 9 BUS SWAP

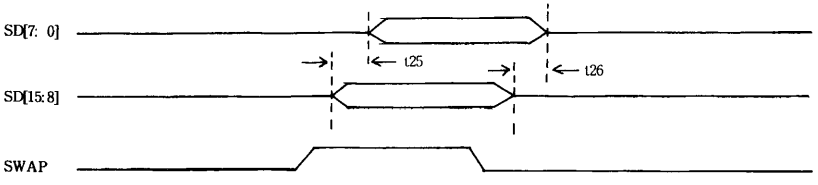


Fig. 10 BUS SWAP

I General Description

The UMC's HEAT (High End AT) Chip Set UM82C380 is a highly integrated, flexible solution for high performance 80386 PC/AT compatible systems. Fabricated using advanced 1.2μ CMOS VLSI technology, it provides high reliability, low power, low chip count features for system implementation. A commercial 25MHz/0 wait state. 12MByte main memory system with cache memory control and math-coprocessor features can be easily built in a standard baby AT size mother board (12" x 8.6") with all necessary components included.

II Features

- Highly integrated 25 MHz/0 wait state 80386 PC/AT compatible
- Supports UMC UM82152/INTEL 82385 Cache Controllers
- Easy Page/Cache mode interchange on motherboard
- 32-bit memory bus interface
- Slow DRAM 100/120 ns at 25/20 MHz 0 wait state operation
- Supports 1M/256K SIM module
- On-board memory up to 12MBytes, extendable to 32MBytes using add-on card
- Shadow RAM for system BIOS
- 8MHz I/O bus timing
- Supports 80287/80387 /3167 Math-coprocessor
- EMS 4.0 interface through software emulation
- DOS/OS2/XENIX/UNIX operation
- Commercially available BIOS (Phoenix/Award/AMI) applicable

III System Description

The UM82C380 series consists of five chips, the UM82C381 System Controller, UM82C382 Address Buffer, UM82C383 Data Buffer, UM82C384 Memory Controller and UM82C388/389 Cache Interface. Combined with UMC's UM82C206 Integrated Peripheral Controller, the chip set forms a highly integrated solution for 25MHz 80386 PC/AT systems with Page/Cache Mode options.

The UM82C380 series supports a local 32-bit CPU/MP bus, a 32-bit memory data bus, a 16-bit AT channel bus, an 8 bit I/O channel peripheral data bus and 8MHz system clock to provide the best compatibility with industry standards.

The UM82C381 is a System Controller. It provides all four bus control signals, synchronized reset for CPU and peripherals, refresh control, math-coprocessor (80287/80387) interface, address decoding logic, CLK2, BCLK and timer clock generation.

The UM82C382 is an Address Buffer. It provides address interface to processor address, system address, DMA address XA and latched XD bus. A 10-bit refresh counter is included for both 256K and 1M DRAM refresh.

The UM82C383 is a Data Buffer. It provides bus interface for CPU local data bus, system data bus and peripheral data bus. Word-swap logic is also built in to facilitate the 80386 read or write 32-bit data through PC/AT 16-bit data bus.

The UM82C384 is a Memory Controller. It provides control for 32-bit memory data bus, memory paging control for 256K and 1M DRAM, RAS and CAS control for system memory.

The UM82C388 is a Cache interface. It provides a simple DRAM controller to interface INTEL 82385 Cache controller with the system memory.

The UM82C389 is another Cache Interface. It also provides a simple DRAM Controller to interface UM82152 Cache Controller with the System Memory, it has been highly integrated for easy application.

IV System Configurations

Basically, three different 80386 PC/AT system configurations can be implemented using UM82C380 series HEAT chip set. These are Page Mode, UM82152 Cache Control Mode, and INTEL 82385 Cache Control Mode. All three mode implementations will require the four common core logic devices of HEAT chip set; UM82C381, UM82C382, UM82C383 and UM82C206. The UM82C384 will be needed for Page Mode , while UM82C389 and UM82C388 are needed for UM82152 and 82385 Cache Control Modes. The block diagrams and the required IC list for each system configuration is illustrated in Figures 1,2, and 3 .

A software driver is required to initiate the UM82152 when the system is working in UM82152 Cache Control Mode. A PAL equation is needed to implement the HEAT chip set working in INTEL 82385 Cache Control Mode. Either or both of these tools can be requested from UMC's worldwide sales offices.

V Remarks

Throughout HEAT documents,a "*" will be attached to specific pin name if it's active low, CLK2* ,for example.

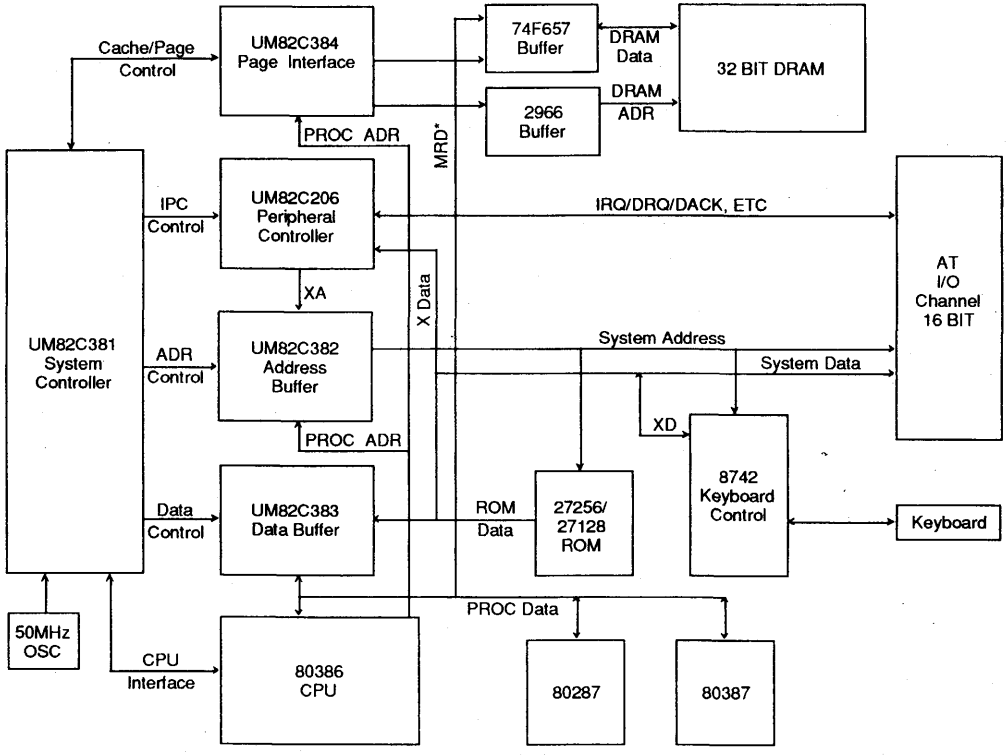


Figure 1. HEAT Chip Set System Diagram (Page Mode)

Required IC List:

80386	x1	80387	x1	
UM82C206	x1	27256	x2	
UM82C381	X1	AM2966	x4	
UM82C382	x1	74F657	x4	
UM82C383	x1	74F04	x1	
UM82C384	x1	74C04	x1	
8042	x1	7406	x1	

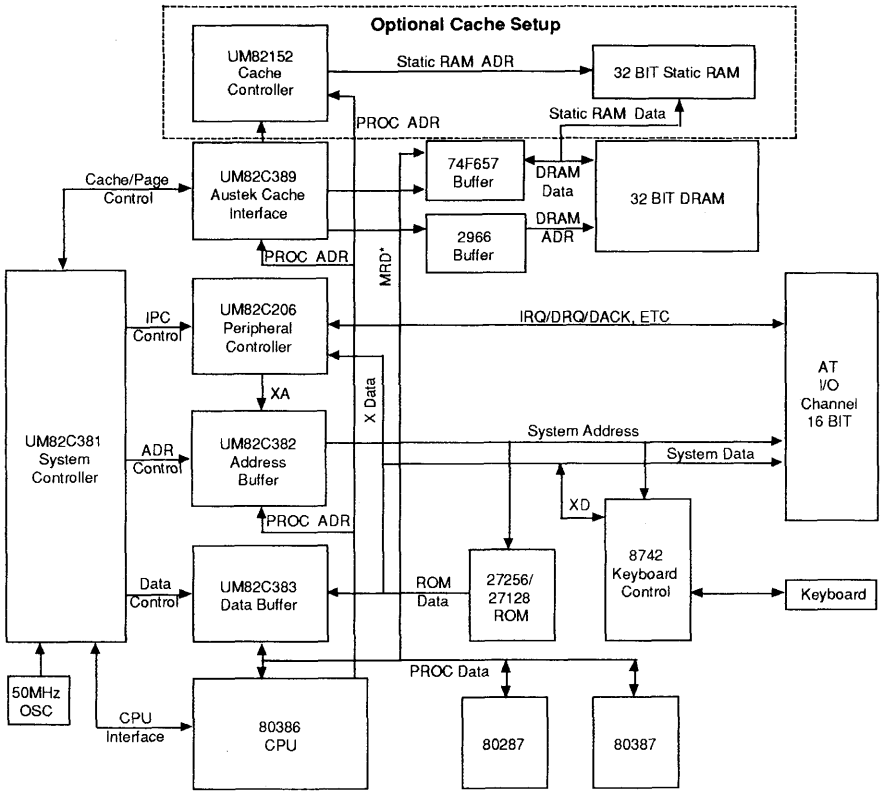


Figure 2. HEAT Chip Set System Diagram (Cache Mode with UM82152)

Required IC List:

80386	x1	UM82152	x1	74F657	
UM82C206	x1	8Kx8-25	x4	74F04	x1
UM82C381	x1	8042	x1	74C04	x1
UM82C382	x1	80387	x1	7406	x1
UM82C383	x1	27256	x2	*74F74	x1
UM82C389	x1	AM2966	x4	*74F258	x1
74F08	x1	74F74	x1		

*needed only when using 27256

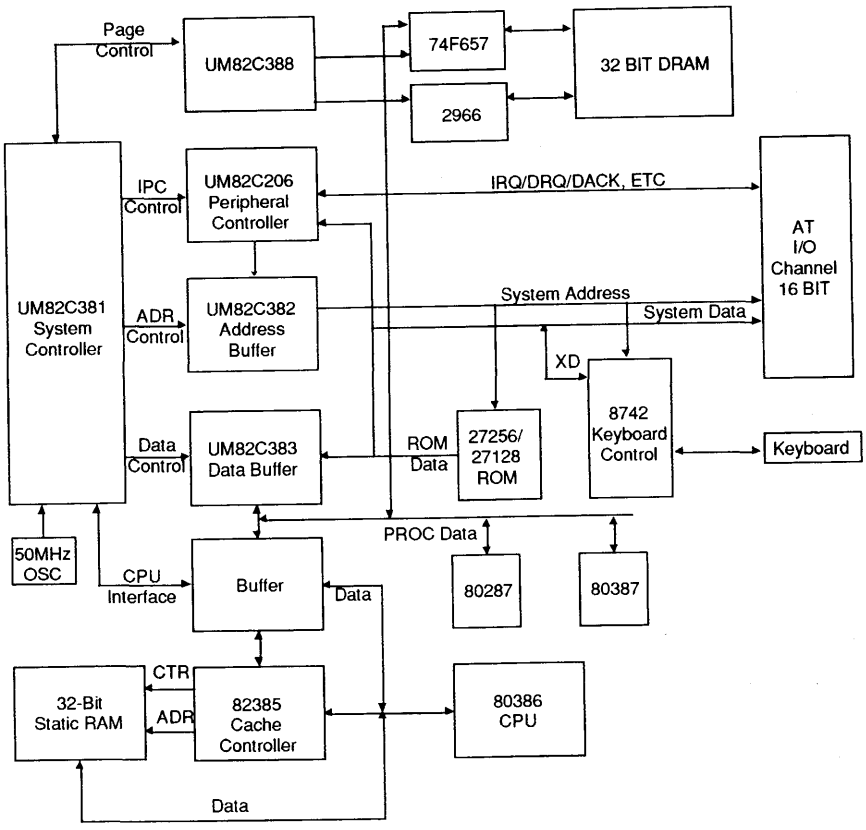


Figure 3. HEAT Chip Set System Diagram (Cache Mode with INTEL 82385)

Required IC List

80386	x1	82385	x1	74F04	x1
UM82C206	x1	4Kx4-25	x16	74C04	x1
UM82C381	x1	8042	x1	7406	x1
UM82C382	x1	27256	x2	74F74	x1
UM82C383	x1	AM2966	x4	74F646	x4
UM82C388	x1	74F657	x4	74F573	x2
74F08	x1	74F32	x1	18P8A	x1

I General Description

The UM82C381 is a system controller. It provides bus control signals to PC/AT and 32-bit memory expansion bus. It also provides synchronized reset for CPU and peripherals, refresh control, math-coprocessor (80287/80387/3167) interface, address decoding logic CLK2, CLK* and timer clock generation.

II Features

- CPU interface and bus control
- PC/AT expansion bus interface
- Clock generation
- Numerical processor 80287/80387 interface
- Peripheral chips interface
- Refresh and DMA logic
- Reset and shut down logic
- Advanced 1.2μM CMOS technology
- TTL compatible input
- 120 pin flat package

III Block Diagram

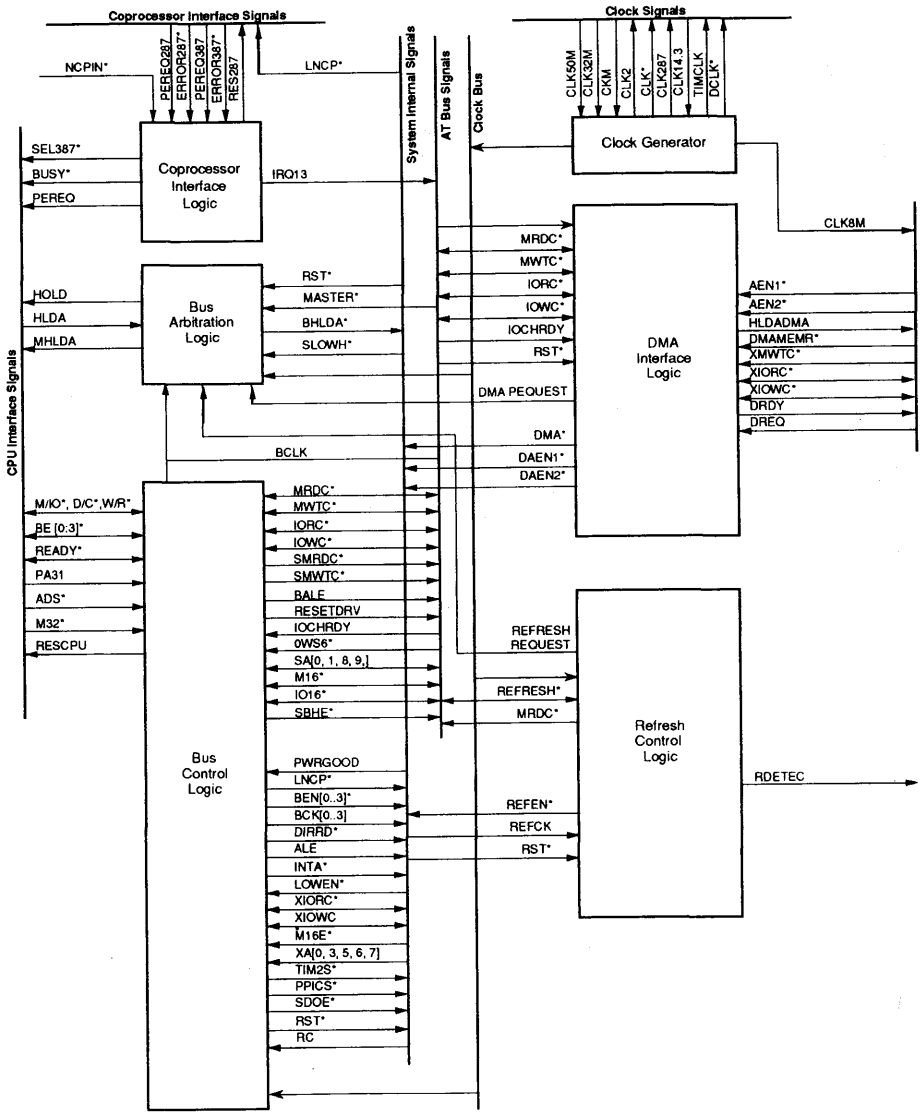


Figure 1. Block Diagram

IV Pin Configuration

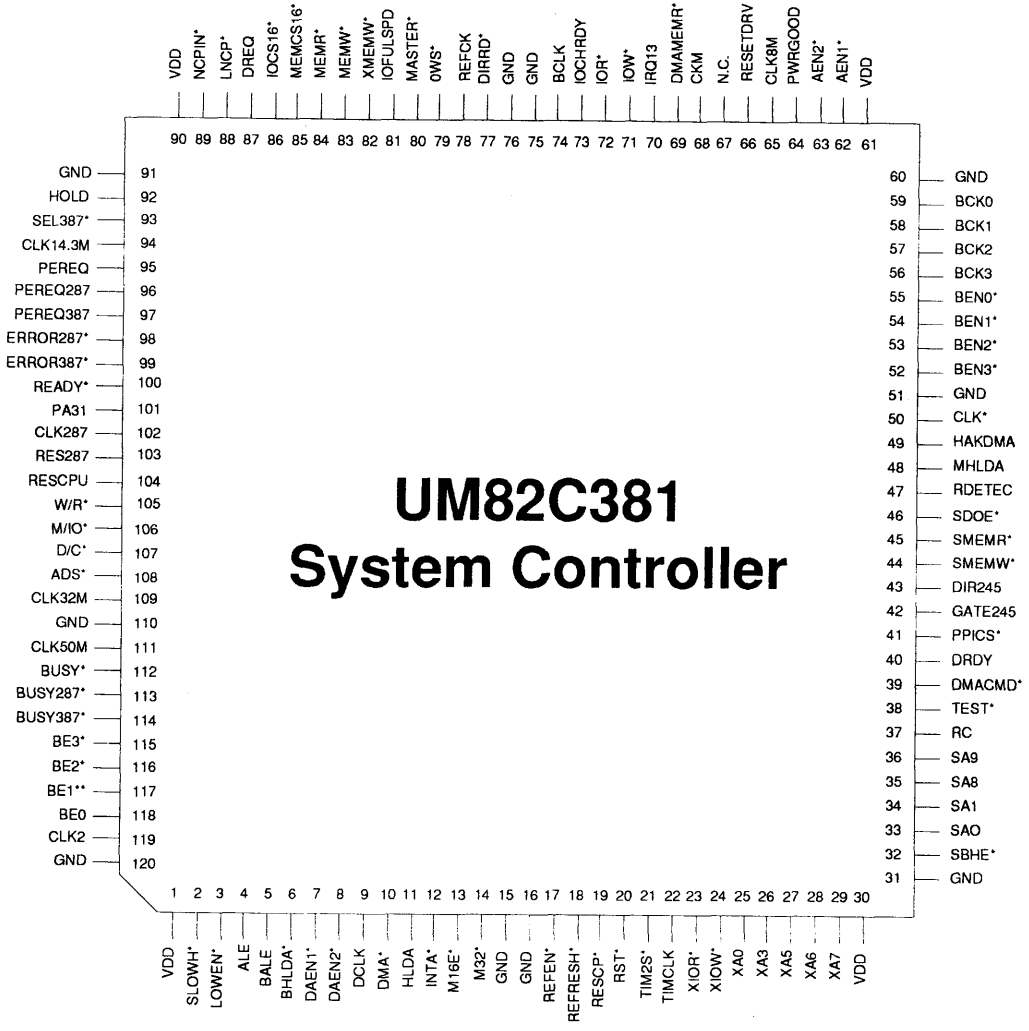


Figure 2. Pin Configuration

VI Functional Description

The function of UM82C381 can be divided into six sub-modules (see block diagram of Figure 1)

- Clock generator
- Bus control logic
- DMA interface logic
- Refresh logic
- Bus arbitration logic
- Numerical processor interface logic

6.1 Clock Generator

The clock generator may operate in both synchronous and asynchronous modes. It has two clock inputs - CK50M and CK32M, both of which are driven from a TTL crystal oscillator.

(1) When IOFULSPD is high, it operates in synchronous mode

CLK2 = CK50M
CLK* = CK50M/2
BLCK = CK50M/4

(2) When IOFULSPD is low, it operates in asynchronous mode

a. During CPU local memory cycle

CLK2 = CK50M
CLK* = CK50M/2
BCLK = CK50M/4

b. During CPU AT BUS cycle or DMA cycle

CLK2 = CK32M
CLK* = CK32M/2
BCLK = CK32M/4

If the target of system clock is 16MHz, IOFULSPD can be pulled high and CK50M is driven by 32MHz clock. In this case, CK32M does not matter for any operation. If the target of system clock is more than 16 MHz, IOFULSPD must be pulled low, CK50M is driven by double frequency of system clock and CK32M is driven by 32MHz clock in order to provide 8 MHz AT bus timing during non-local bus operation.

6.2 Bus Control Logic

a. Reset operation

The UM82C381 provides two reset inputs, PWRGOOD and RC. PWRGOOD is the power good signal from the power supply. When PWRGOOD is inactive (low), UM82C381 asserts RESCPU and RESETDRV for a system reset. RC is generated from the keyboard controller when a "warm reset" is required. The warm reset activates RESCPU to reset the 80386 CPU. RESCPU is also activated by the UM82C381 after a shutdown condition is detected, and held high for at least 16 CLK2 cycles and then deasserted. RESCPU is synchronous with CLK2, ensuring proper CPU operation. RESCP* is used to disable RTC during CPU reset period.

b. Bus status definitions

During CPU memory cycle (ADS* low and M/IO* high), if M32* is sampled low, it means current cycle is CPU local memory cycle, otherwise, it is an AT bus cycle.

The bus control logic gains control when M32* is detected high or M/IO* is low under ADS* active. It will perform the necessary synchronization of control and status signals between the AT bus and the processor. The UM82C381 supports 8 and 16 bit transfers between the processor and 8 or 16 bit memory or I/O devices located on the AT bus.

The data conversion definitions between CPU status signals and AT 8- and 16-bit bus are shown in Table 1.

IO16*/ M16*	BE3*	BE2*	BE1*	BE0*	SA1	SA0	BHE*	Cycle Type
X	1	1	1	0	0	0	1	Low byte on 8 or 16 bit bus
1	1	1	0	1	0	1	0	High byte on 8 bit bus
0	1	1	0	1	0	1	0	High byte on 16 bit bus
X	1	0	1	1	1	0	1	Low byte on 8 or 16 bit bus
1	0	1	1	1	1	1	0	High byte on 8 bit bus
0	0	1	1	1	1	1	0	High byte on 16 bit bus
0	1	1	0	0	0	0	0	Word on 16 bit bus
1	1	1	0	0	0	0	0	Word on 8 bit bus
					0	1	0	
0	1	0	0	1	1	0	1	2 bytes split on 16 bit bus
1	1	0	0	1	0	1	0	2 bytes split on 8 bit bus
					1	0	1	
0	0	0	1	1	1	0	0	Word on 16 bit bus
1	0	0	1	1	1	0	0	Word on 8 bit bus
					1	1	0	
0	1	0	0	0	0	0	0	3 bytes on16-bit bus
					1	0	1	
1	1	0	0	0	0	0	0	3 bytes on 8 bit bus
					0	1	0	
					1	0	1	
0	0	0	0	1	0	1	0	3 bytes on 16 bit bus
					1	0	0	
1	0	0	0	1	0	1	0	3 bytes on 8 bit bus
					1	0	0	
					1	1	0	
0	0	0	0	0	0	0	0	4 bytes on 16 bit bus
					1	0	0	
1	0	0	0	0	0	0	0	4 bytes on 8 bit bus
					0	1	0	
					1	0	0	
					1	1	0	

Notes: 1. I/O16* signal during I/O cycle
2. M16* signal during memory cycle
3. X means that the value of this signal doesn't matter for that cycle

Table 1. Data conversion definitions

c.Bus timing

The UM82C381 provides control signals to emulate the 8MHz AT bus signals. The number of AT bus cycles for CPU operation is shown in Table 2. For slow I/O devices, IOCHRDY is used to extend command cycle.

Operation	Bus Size	Number of Cycles Required	
		0 W.S.	Normal W.S.
memory read	16 bit	4	6
memory read	8 bit	6	12
memory write	16 bit	4	6
memory write	8 bit	6	12
I/O read	16 bit	6	6
I/O read	8 bit	6	12
I/O write	16 bit	6	6
I/O write	8 bit	6	12

Note: A normal wait state occurs if the device being accessed does not specify the number of wait states that should be generated by the system.

Table 2. Number of AT Bus Cycles

6.3 DMA Interface Logic

Essentially, DMA operation is controlled by UM82C206. During DMA cycle, UM82C381 provides interface among UM82C206, local bus and AT bus. It provides command signals to AT bus and generates bus cycle status signal to local bus for memory operation. The DMA operation is memory to I/O only and its bus size can be 8 or 16 bits.

The bus cycle status definitions for the non-CPU cycle are shown in Table 3:

BHDLA	M/IO	D/C	W/R	Cycle Time
1	0	0	0	Invalid cycle time
1	0	0	1	Non-CPU refresh read
1	0	1	0	Non-CPU memory write
1	0	1	1	Non-CPU memory read(*)
1	1	0	0	Invalid cycle type
1	1	0	1	Non-CPU refresh cycle
1	1	1	0	Non-CPU cycle (*)
1	1	1	1	Non-CPU, no cycle in progress

* This cycle can occur during the transition to and from memory write cycles.

Table 3. Non-CPU cycle status definitions

6.4 Refresh Logic

The refresh control logic is triggered by REFCK, witch generates the refresh control signals to the AT bus cycle. MEMR* is asserted low during a refresh cycle and the refresh address A0-A9 is provided by UM82C382 when REFEN* is active. It also provides the bus cycle status to the local bus for memory refresh operation.
Its definitions during the refresh cycle are shown in Table 3.

6.5 Bus Arbitration Logic

The UM82C381 controls all bus activity and provides arbitration between the CPU, DMA, DRAM refresh and Master device and SLOWH*. SLOWH* comes from UM82C382 and is used to control the system speed. The UM82C381 generates HOLD request to the CPU and arbitrates those requests in a non-preemptive manner. The CPU relinquishes the bus by issuing HLDA. During a refresh cycle, the refresh logic has control of the bus until REFRESH* goes inactive. During a DMA cycle, the DMA controller has control of the bus until DREQ (HRQ of UM82C206) goes inactive.

6.6 Numerical Processor Interface Logic

The UM82C381 provides signals to interface between CPU and coprocessor. The coprocessor can be either UM80287 or UM80387. If NCPIN* is low, it means that UM80287 or UM80387 is installed; otherwise, no coprocessor is present.

Since 80386 samples its ERROR* input during initialization to determine the type of coprocessor present, SEL387* is low after RESCPU goes low and before execution of the first instruction, this pin can be used to seperate 80387 or 80287 present.

If 80387 is present, 82C381 handles BUSY387*, PEREQ387* and ERROR387* signals from the 80387 to the CPU and generates IRQ13 for error handling. During executing a task, 80387 issues a BUSY387* signal to the 82C381. Under normal operation, it is passed out to the CPU as BUSY*. If during this busy period, a coprocessor error occurs, ERROR387* input to the 82C381 becomes active resulting in latching of the BUSY* output and assertion of IRQ13. BUSY* stays active until cleared by I/O write cycle to address 0F0(H).

If 80287 is present, 82C381 provides the decoding required for selecting and resetting the 80287, handling BUSY287*, PEREQ287 and ERROR287* signals from the 80287 to the CPU and generates IRQ13 for error handling. The 80287 chip select LNCP* is active for I/O address OF8(H)-OFF(H) and PA31 is high. During execution of a task, 80287 issues a BUSY287* signal to the 82C381. Under normal operation , it is passed out to the CPU as BUSY*. If during this busy period, a coprocessor error occurs, ERROR287* input to the 82C381 becomes active, resulting in latching of the BUSY* output and assertion of IRQ13. BUSY* stays active until cleared by I/O write cycle to address 0F0(H) or 0F1(H).

The clock signal to 80287 is also provided by 82C381. If CKM is low, CLK287 is a 16 MHz clock signal with 50% duty cycle and 80287 is running at 5.4MHz. If CKM is high, CLK287 is a 10.67MHz clock signal with 33% duty cycle and 80287 is running at 10.67 MHz.

I General Description

The UM82C382 Address Buffer is in UMC's 82C380 series High End AT (HEAT) Chip Set. It provides address interface to processor address, system address, DMA address XA and Latched Bus. A 10-bit refresh counter is built in for both 256K and 1M DRAM refresh. Two address decoders are included for ROM space and on-board I/O port.

II Features

- 24 bit address line buffer
- Supports 256Kx1 and 1Mx1 DRAM refresh
- Advanced 1.2μ CMOS Technology
- 120 pin flat package

III Block Diagram

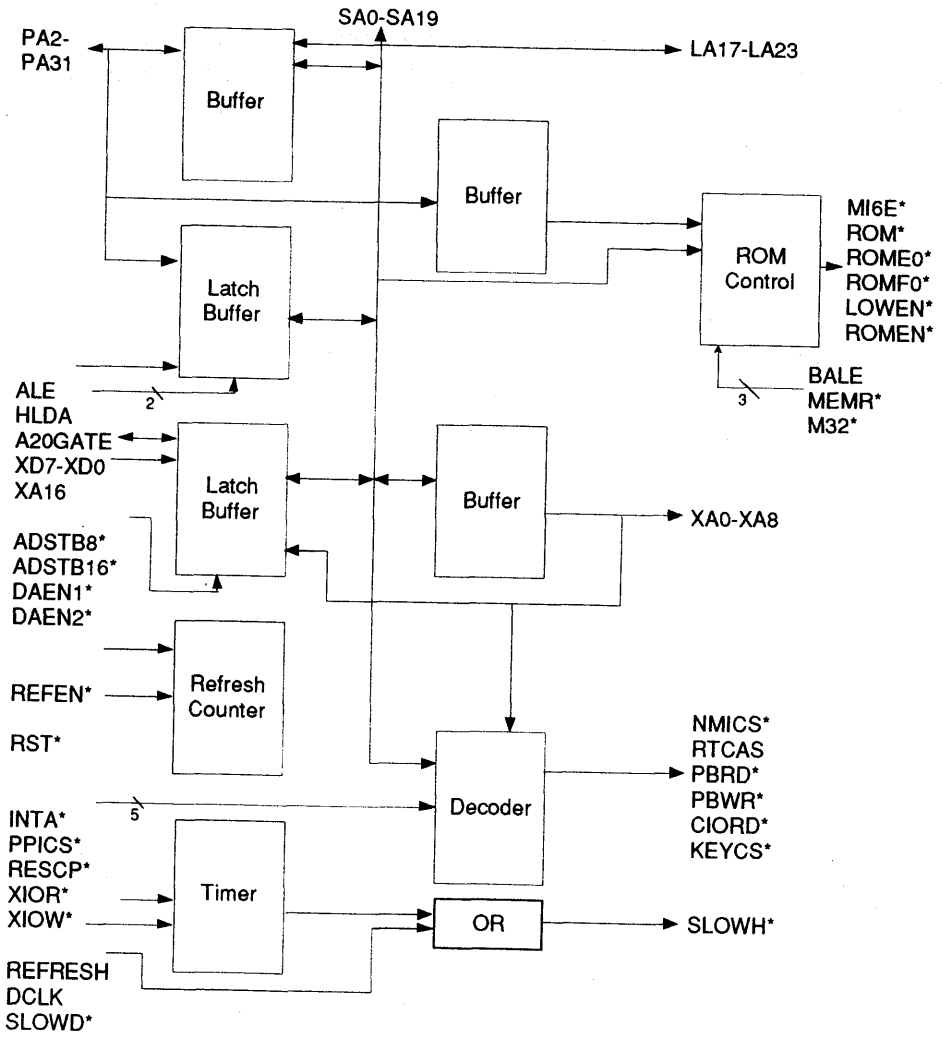


Figure 1. UM82C382 Block Diagram

IV Pin Configuration

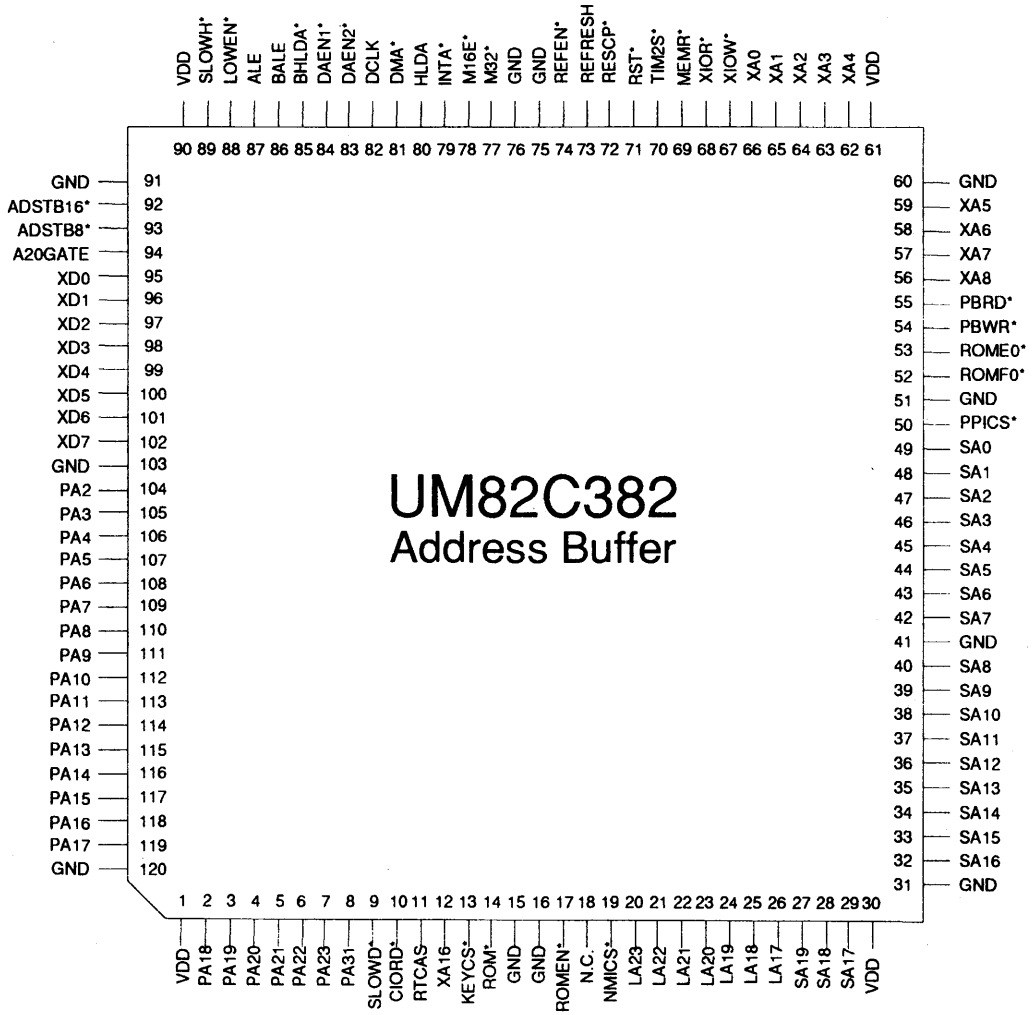


Figure 2. Pin Configuration

VI Functional Description

The UM82C382 is an address interface between processor bus, system bus and peripheral bus (X-bus).

During the CPU cycle, address PA2-PA19 from CPU bus will be linked to system bus and X-bus, while PA17-PA23 will be linked to LA17-LA23 of the system bus. If the ROM address space is selected during this period, the ROM control unit will generate the signals to access the ROM address, the decoder will also generate signals to access I/O port data.

During the DMA cycle, address LA17-LA23 from the system bus will be linked to PA17-PA23 of CPU bus, and SA2-SA19 will be linked to PA2-PA19. During this cycle, system address is generated from DMA controller or refresh counter. When REFEN* is active, the refresh counter will issue refresh address to the system bus. The refresh counter will be incremented by one automatically after the refresh cycle.

The DMA controller will dominate the system bus during the DMA cycle, both 8-bit and 16-bit data transfer types can be generated as DMA transfer. For 8-bit data transfer, with the negative transition of ADSTB8*, XA0-XA7 will be linked to SA0-SA7, XD7-XD0 will be linked to SA15-SA8, while the contents of SA15-SA8 will be latched in the latch buffer. For 16-bit data transfer, with the negative transition of ADSTB16*, XA8-XA0 will be linked to SA8-SA0, XD7-XD0 will be linked to SA16-SA9, while the contents of SA16-SA9 will be latched in the latch buffer.

A timer is also designed in UM82C382 to provide the necessary clock timing to be compatible with standard PC/AT 8-MHz bus. The user is able to slow down the system speed by enabling SLOWD* to keep the system timing compatible with PC/AT.

I General Description

The UM82C383 Data Buffer is one of UMC's High End AT (HEAT) Chip Set, It is an interface between 32-bit processor data bus, 16-bit system data bus and 8-bit peripheral data bus.

II Features

- 32-bit data bus buffer
- 16-bit or 8-bit data-bus buffer for PC/AT bus
- 8-bit I/O port data bus buffer
- Word swap logic
- Advanced 1.2μ CMOS Technology
- 120 Pin Flat Package

III Block Diagram

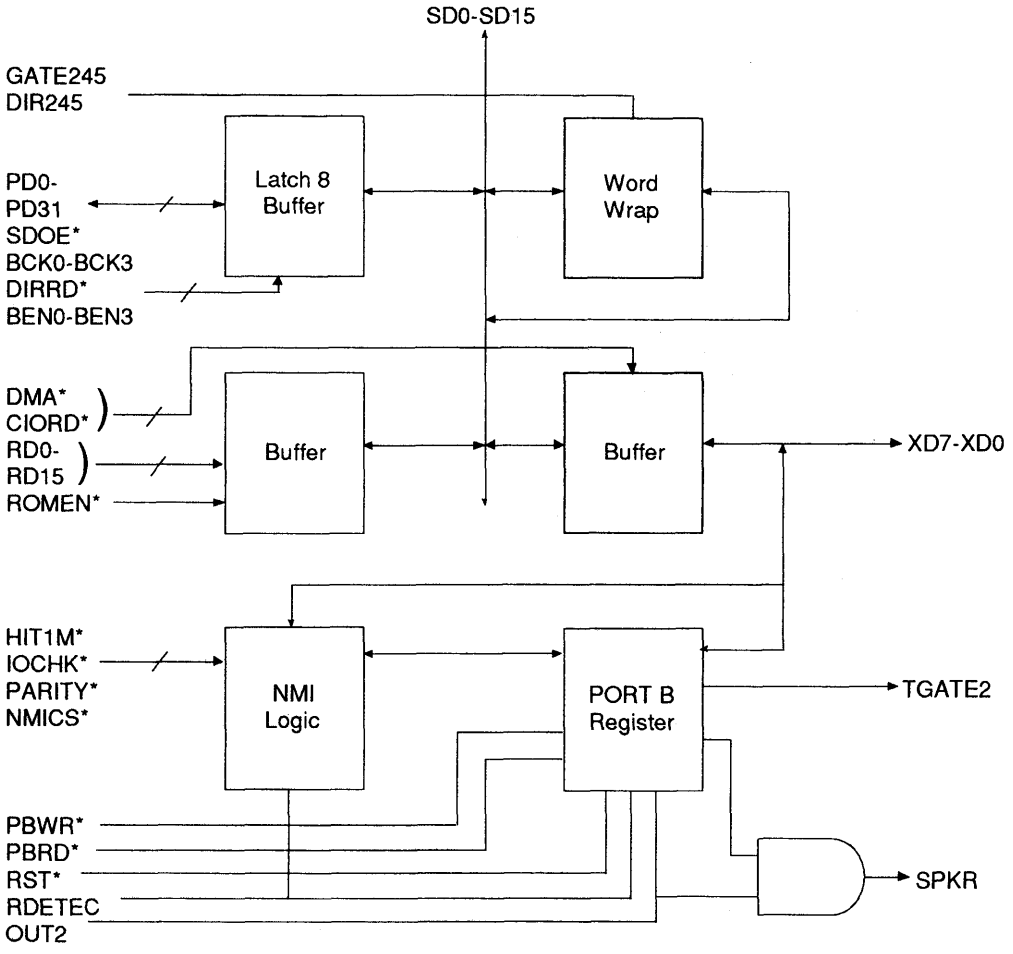


Figure 1. UM82C383 Block Diagram

IV Pin Configuration

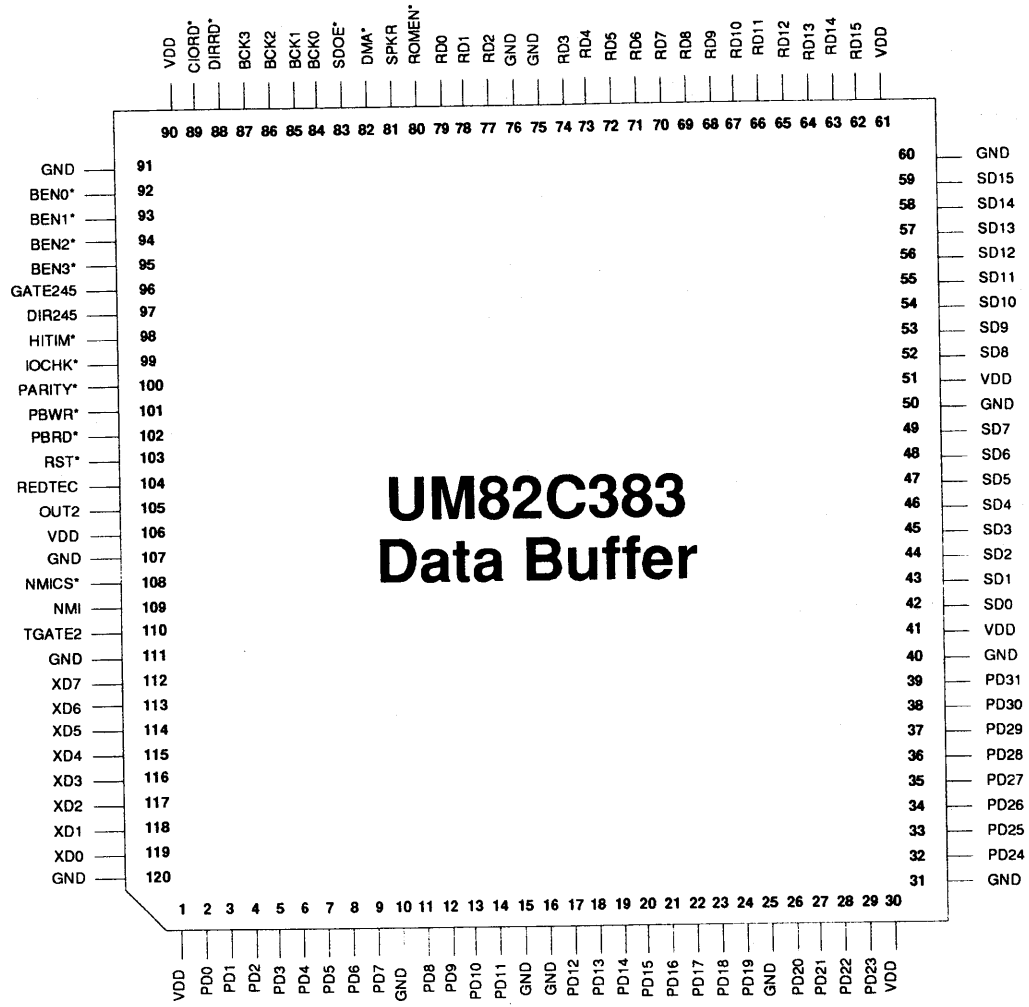


Figure 2. Pin Configuration

VI Functional Description

The UM82C383 Data Buffer contains a 32-bit 80386 data bus buffer, 16-bit PC/AT slot data buffer, 8-bit I/O port data bus buffer, and one internal port 61H. A word-swap logic circuit is also built to facilitate 80386 read or write 32-bit data through PC/AT 16-bit data bus.

During the CPU read cycle, the system bus data can be latched by controlling the signals BCK0-BCK3 and SDOE*. During the CPU write cycle, the processor data can be written to the system bus through data buffer by controlling the signals DIRRD* ,BEN0*-BEN3*. The GATE245 and DIR245 should be asserted to initiate the word wrap circuit to transfer 32-bit data into 8-bit data.

During the DMA cycle, the data transfer between processor bus and system bus is controlled by asserted DIRRD*, BEN0*-BEN3* signals. When the DIRRD* is low, the system bus will be transferred to processor bus. When the DIRRD* is high, the processor bus will be transferred to system bus. The signals GATE245, DIR245 should be asserted to initiate the word wrap circuit if the data transfer is 8-bit only.

UM82C383 also generates NMI signals, which can be enabled by Port B Bit 7. Whenever IOCHK* or PARITY* is low, an NMI error signal will be generated, and can be checked by reading Port B, Bit 6. When a positive transition occurs in HITIM*, NMI will be forced High, which can be checked by reading Port B,Bit 7.

The register descriptions are illustrated as follows:

WRITE PORT B:

BIT 7		: Not defined
BIT 6		: Not defined
BIT 5		: Not defined
BIT 4		: Not defined
BIT 3	-->1	: Clear hit timer register
BIT 2	-->1	: Clear parity check error
BIT 1	-->1	: Enable speaker output
BIT 0		: Trigger 8254 timer 2

READ PORT B:

BIT 7	: Hit timer register status
BIT 6	: Parity check status
BIT 5	: 8254 timer 2 output
BIT 4	: Read RDETEC input to check if refresh counter is active
BIT 3	: Read back written data
BIT 2	: Read back written data
BIT 1	: Read back written data
BIT 0	: Read back written data

I General Description

The UM82C384 is one of UMC's High End AT (HEAT) Chip Set. It provides memory control functions which facilitate wide ranges of DRAM and CPU speed selections for 80386 AT system design.

II Features

- Supports 16MHz, 20MHz and 25MHz Intel 80386
- Supports DRAM speed range from 60ns up to 120ns
- Supports 256K and 1M DRAM
- Supports up to 12M Bytes on board memory
- Using page mode DRAM to reduce wait states for same page memory access (hit)
- Relocates BIOS to high speed DRAM for very fast BIOS function calls
- 1.2μ CMOS technology

III Block Diagram

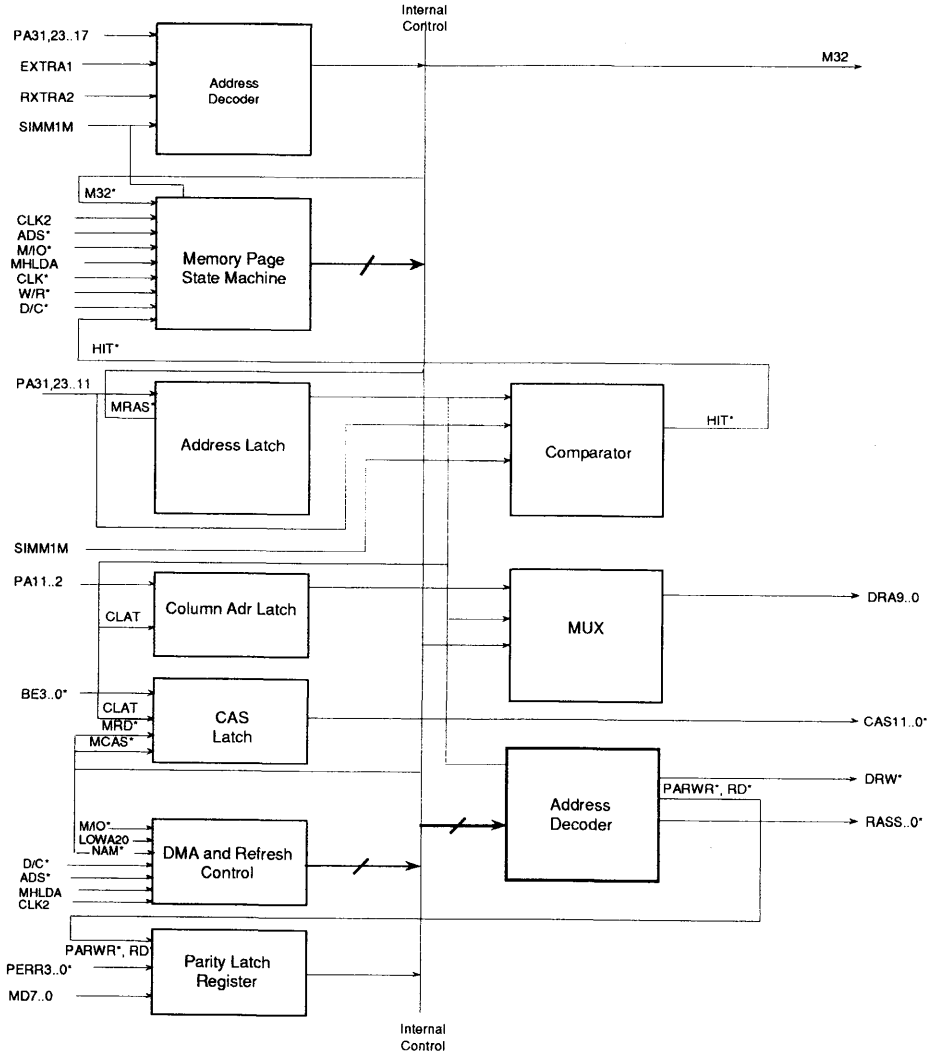


Figure 1. UM82C384 Block Diagram

IV Pin Configuration

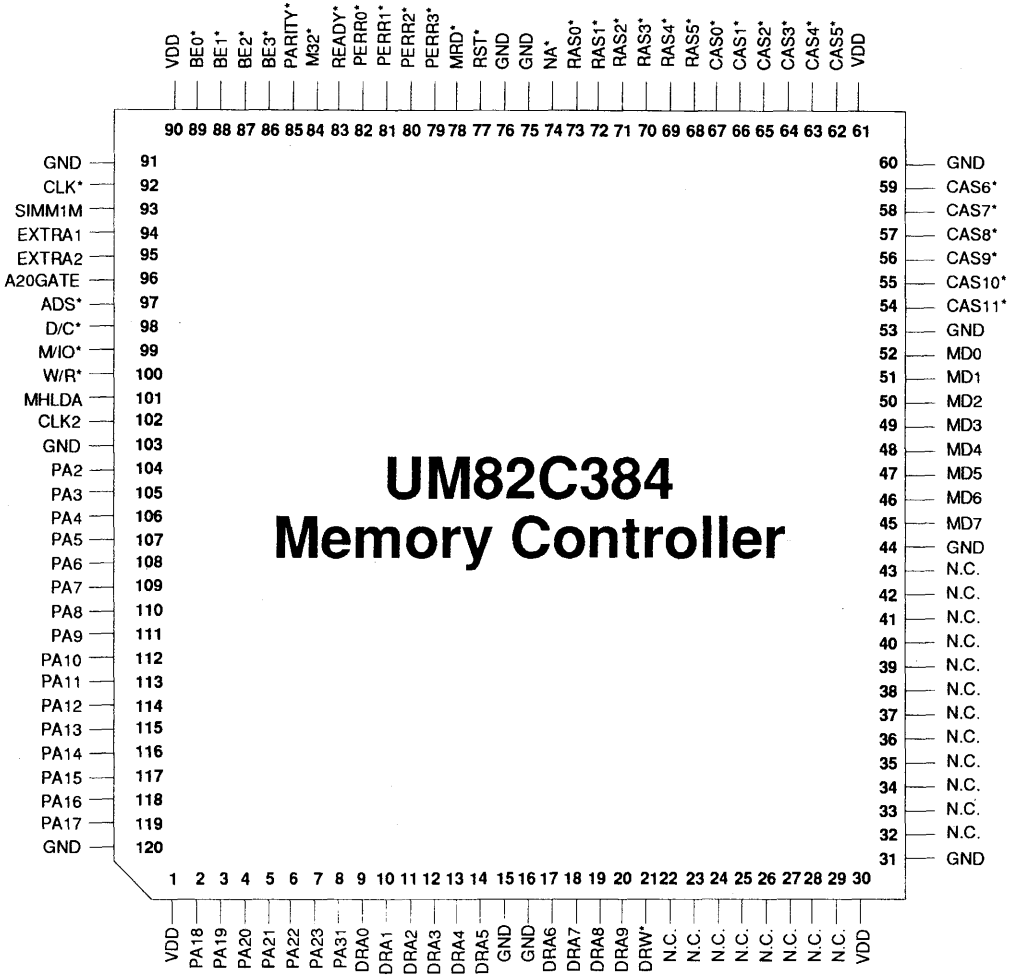


Figure 2. Pin Configuration

VI Functional Description

(a) Memory Mapping:

The memory mapping of UMC 386PC/AT chip set is shown in Figures 3 and 4. The 640 KB of base memory can execute existing MS-DOS applications developed for 80286-based product. On top of the base memory is 128KB video RAM, 64KB LIM pages and 128KB system BIOS. The extended memory can be 1M, 2M, 3M, 7M, and 11M bytes. The size of the memory is determined by SIMM1M, EXTRA1, and EXTRA2 as listed in table 2.

SIMM1M	EXTRA1	EXTRA2	System Memory	DRAM Type
0	0	0	1M	
0	1	0	2M	256K
0	1	1	3M	
1	0	0	4M	
1	1	0	8M	1M
1	1	1	12M	
0	0	1	*Illegal	
1	0	1		

Table 2

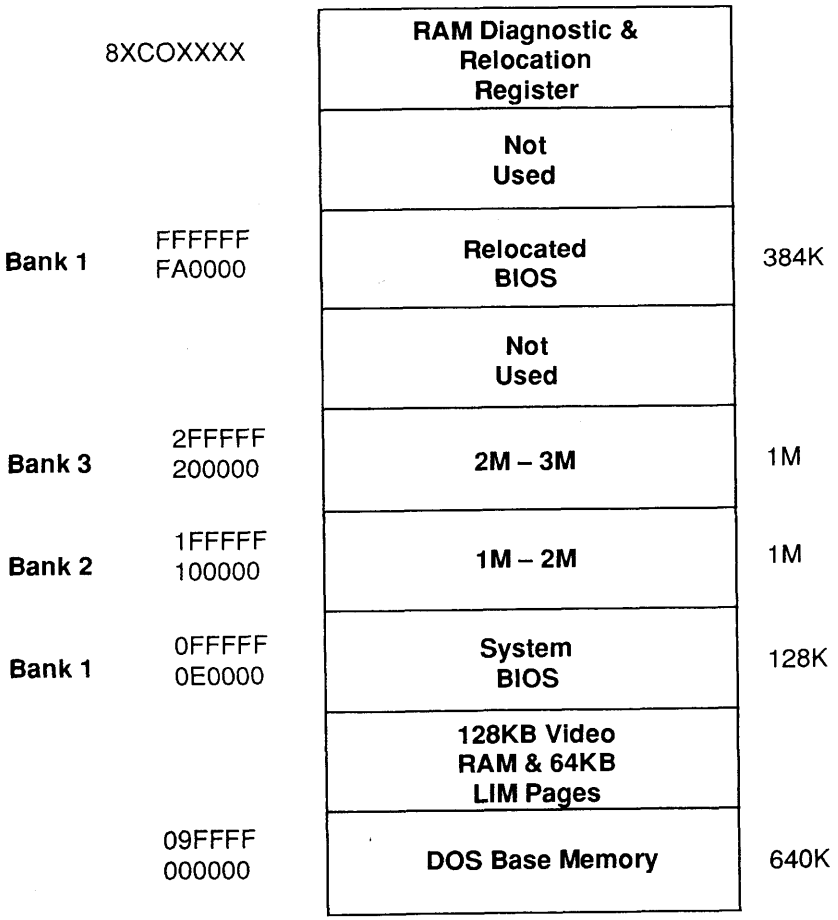


Figure 3. Memory Mapping when using 256K DRAM. M32* is active in all regions except in regions marked "not used" and video RAM and LIM pages.

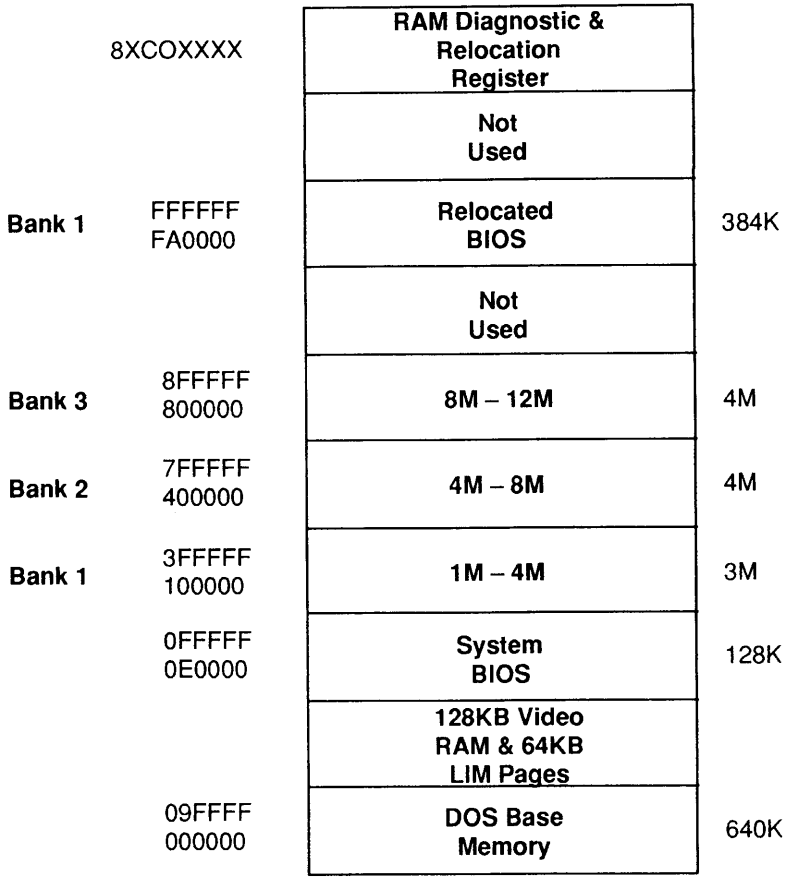


Figure 4. Memory Mapping when using 1M DRAM. M32* is active in all regions except in regions marked "not used" and video RAM and LIM pages.

(b) ROM Mapping:

Of the 384KB of memory addressed on top of the 16MB address space, the last 128KB has a special addressing feature. This 128-KB block, starting at address FE0000, can be relocated (mapped) via special hardware map registers to the system BIOS (0E0000 - 0FFFFF). When mapped, the 128-KB RAM block normally located at FE0000 can be addressed at either FE0000 or 0E0000. The ROM devices are not accessible while the RAM is mapped to the address space normally occupied by the ROMs.

In addition to this relocation capability, the 128KB block of RAM beginning at address FE0000 can be write-protected by special hardware registers on the system memory board. The relocation and write-protection capabilities allow the system ROM to be replaced by high-speed RAM having the same contents (Shadow RAM).

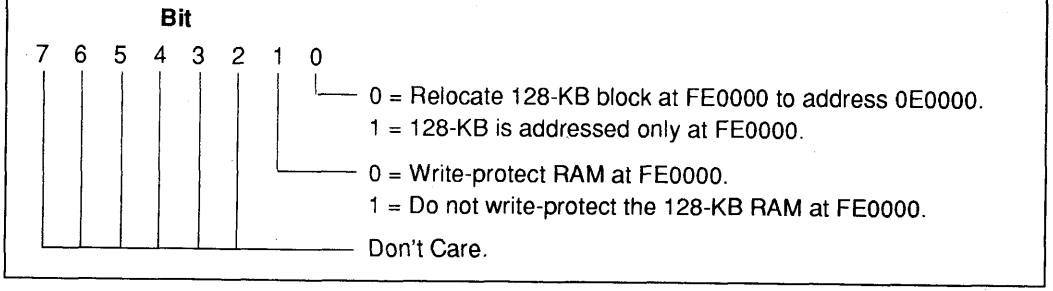
(c) Memory Mapped Registers:

UM82C384 has two memory-mapped registers: one is used in RAM relocation, the other is for RAM diagnostics

RAM relocation:

The address and contents of the special memory-mapped hardware register used in the RAM relocation is shown in the following bit map. This register is a write-only register:

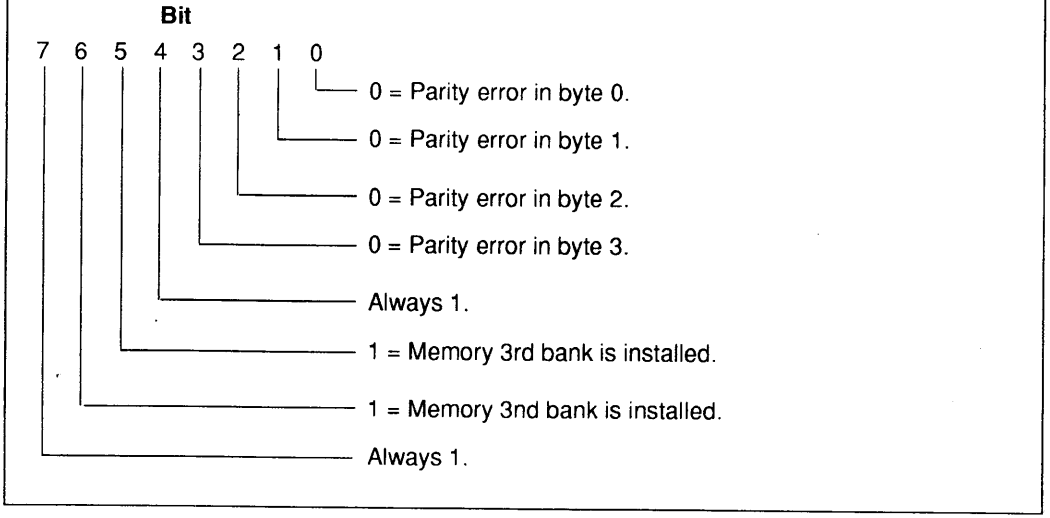
RAM Relocation --> Memory-Mapped Address 80C00000 (write only)



RAM Diagnostics:

The RAM diagnostics register helps test the memory subsystems. This register allows a diagnostics program to read the state of memory configuration jumpers on the system memory board. The register also contains the status of the parity bits for each of the four bytes of a 32-bit memory access. RAMs can be tested very quickly, because they are performed by reading and writing 32-bit data patterns. When a parity error is detected, a diagnostics program uses the RAM diagnostics register to determine which byte in the 32-bit double-word caused the error. The address and contents of the memory-mapped diagnostics register are shown in the following bit map. This register is a read-only register. Writing to this register affects the contents of the RAM relocation register since they share the same memory location.

RAM Relocation --> Memory-Mapped Address 80C00000 (write only)



(d) Bus Cycle Status Definitions

Table 3 gives the bus cycle status definition for the MHLDA, M/IO* D/C*, and W/R* signals:

MHLDA	M/IO*	D/C*	W/R*	Cycle Type
0	0	0	0	CPU Interrupt Acknowledge
0	0	0	1	Invalid Cycle Type
0	0	1	0	CPU I/O Read
0	0	1	1	CPU I/O Write
0	1	0	0	CPU Memory Instruction Prefetch Read
0	1	0	1	CPU Halt or Shutdown
0	1	1	0	CPU Memory Data Read
0	1	1	1	CPU Memory Data Write
1	0	0	0	Invalid Cycle type
1	0	0	1	DRAM Refresh - 3 (see note)
1	0	1	0	DMA Memory Write
1	0	1	1	DMA Memory Read
1	1	0	0	Invalid Cycle Type
1	1	0	1	DRAM Refresh - 2 (see note)
1	1	1	0	Non-CPU Cycle - Transition State
1	1	1	1	DRAM Refresh - 1 (see note)

Note: DRAM Refresh Cycles follow the following sequence:
1 → 2 → 3 → 2 → 1

Table 3

(e) RAS, CAS signals and DRAM Module

In order to reduce loading for RAS and CAS signals, six RAS signals and twelve CAS signals are generated to drive three banks of DRAMs. The following tables illustrate the connection of RAS and CAS signals to different banks of DRAMs.

Bank 1	RAS0*,	RAS1*,	CAS0* - CAS3*
Bank 2	RAS2*,	RAS3*,	CAS4* - CAS7*
Bank 3	RAS4*,	RAS5*,	CAS8* - CAS11*

Bit#	31 - 24	23 - 16	15 - 8	7 - 0
Bank 1	CAS3*	CAS2*	CAS1*	CAS0*
Bank 2	CAS7*	CAS6*	CAS5*	CAS4*
Bank 3	CAS11*	CAS10*	CAS9*	CAS8*

Bank 1	RAS1*	RAS0*
Bank 2	RAS3*	RAS2*
Bank 3	RAS5*	RAS4*

(f) DRAM Address corresponding to CPU Address

The following table illustrates the DRAM address corresponding to the CPU address when using 256K or 1M DRAM.

	256K DRAM		1M DRAM	
DRAM Address	**Column**	**Row**	**Column**	**Row**
- DRA0	PA2	PA12	PA2	PA12
- DRA1	PA3	PA13	PA3	PA13
- DRA2	PA4	PA14	PA4	PA14
- DRA3	PA5	PA15	PA5	PA15
- DRA4	PA6	PA16	PA6	PA16
- DRA5	PA7	PA17	PA7	PA17
- DRA6	PA8	PA18	PA8	PA18
- DRA7	PA9	PA19	PA9	PA19
DRA8	PA10	PA11	PA10	PA20
DRA9	0	0	PA11	PA21

Note: DRA0 - DRA7 are in opposite phase with the real CPU address.

I General Description

The UM82C388 is one of the UMC High End AT (HEAT) Chip Set. It provides memory control functions which facilitate wide ranges of DRAM and CPU speed selections for UM80386 AT system design.A summary of DRAM and CPU speed options is listed in Table 1 for quick reference.

II Features

- Supports 16MHz, 20MHz and 25MHz Intel 80386
- Supports 25MHz 80386 with 82385 cache controller
- Supports DRAM speed range from 60ns to 120ns
- Supports 256K and 1M DRAMs
- 1.2μ CMOS technology
- 120 pin flat package

SIMM1M	SW2	SW3	DRAM Type	(MHz)	WH	RH	WM	RM
X	0	0	80ns, 256K, 1M 100ns, 256K, 1M	25(1) 25(1)	3	3	3	3
0	0	1	60ns, 256K 80ns, 256K 100ns, 256K (2)	25 20 16	1	0	2	2
0	1	0	100ns, 256K 120ns, 256K	20 16	1	1	2	2
X	1	1	80ns, 256K (3) 80ns, 1M 100ns, 1M 120ns, 1M	25 25 20 16	0	0	2	3
1	1	0	60ns, 1M 80ns, 1M	25 20	0	0	2	2

Table 1. DRAM and CPU speed options

Notes:
1. For switch position = 0 0 1, CAS precharge time is 30ns at 16MHz. Most 100ns, 256K DRAMs need 40ns CAS precharge time. At least, Hitachi, NMB, Micron will meet this spec.
2. For switch position = x 1 1 (x=don't care), CAS pulse width is 20ns at 25MHz. Almost all the 80ns, 1M DRAMs meet this spec. But for 80ns, 256K DRAM, only the one with fast page mode can meet this spec. At least Hitachi and NMB have 80ns, 256K fast page mode DRAMs.
3. WH = Write Hit, RH = Read Hit, WM = Write Miss, RM = Read Miss

III Block Diagram

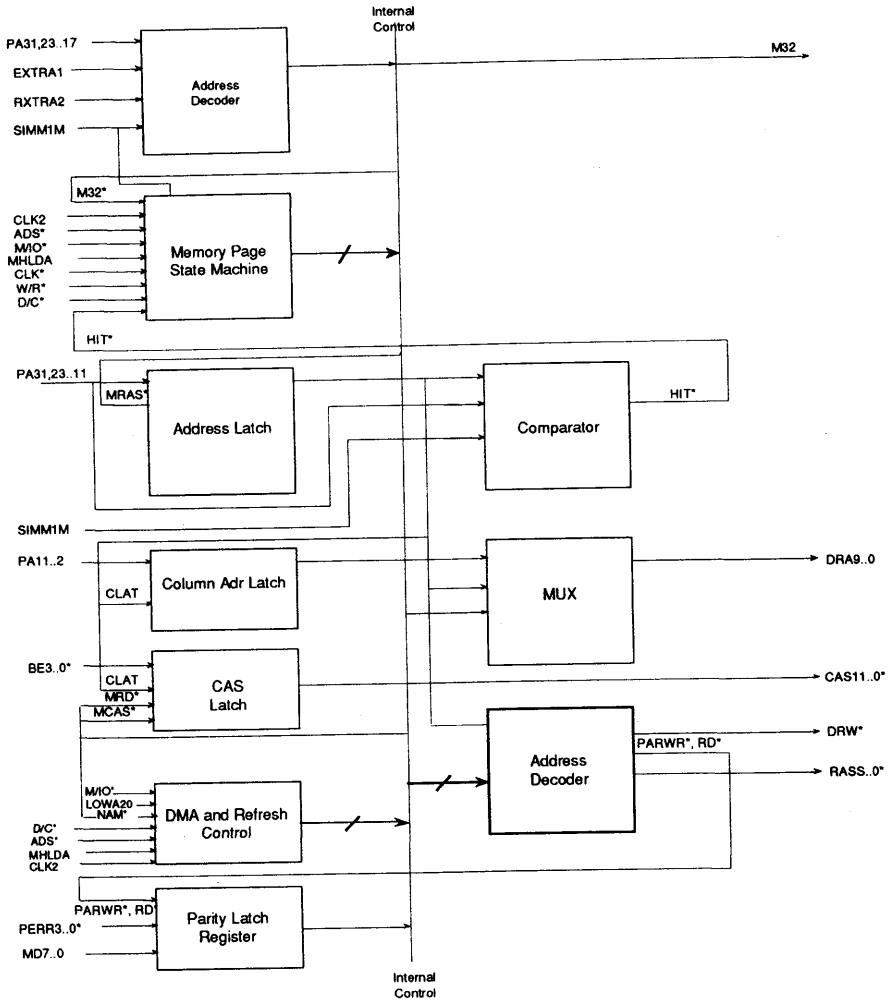


Figure 1. UM82C388 Block Diagram

IV Pin Configuration

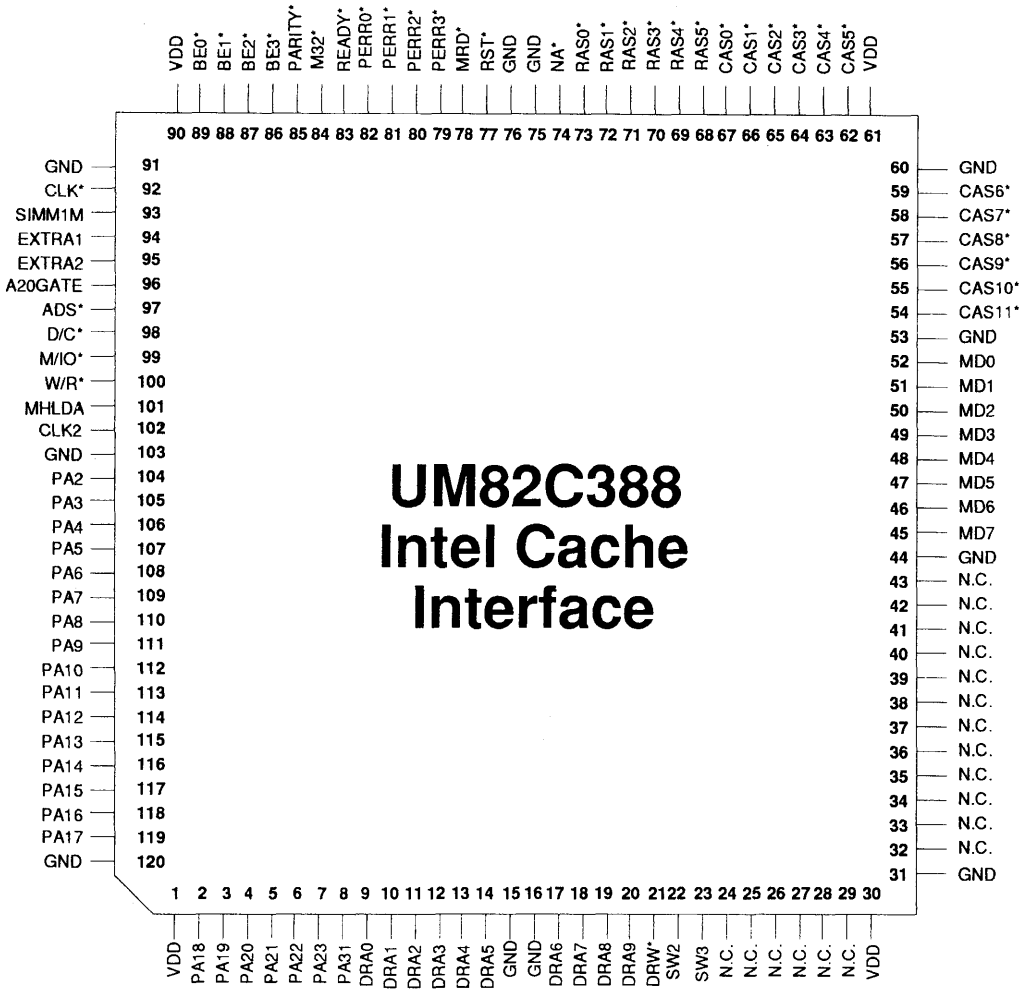


Figure 2. Pin Configuration

VI Functional Description

(a) Memory Mapping:

The memory mapping of UMC 386PC/AT chip set is shown in Figures 3 and 4. The 640 KB of base memory can execute existing MS-DOS applications developed for 80286-based product. On top of the base memory is 128KB video RAM, 64KB LIM pages and 128KB system BIOS. The extended memory can be 1M, 2M, 3M, 7M, and 11M bytes. The size of the memory is determined by SIMM1M, EXTRA1, and EXTRA2 as listed in table 2.

SIMM1M	EXTRA1	EXTRA2	System Memory	DRAM Type
0	0	0	1M	
0	1	0	2M	256K
0	1	1	3M	
1	0	0	4M	
1	1	0	8M	1M
1	1	1	12M	
0	0	1	*Illegal	
1	0	1		

Table 2

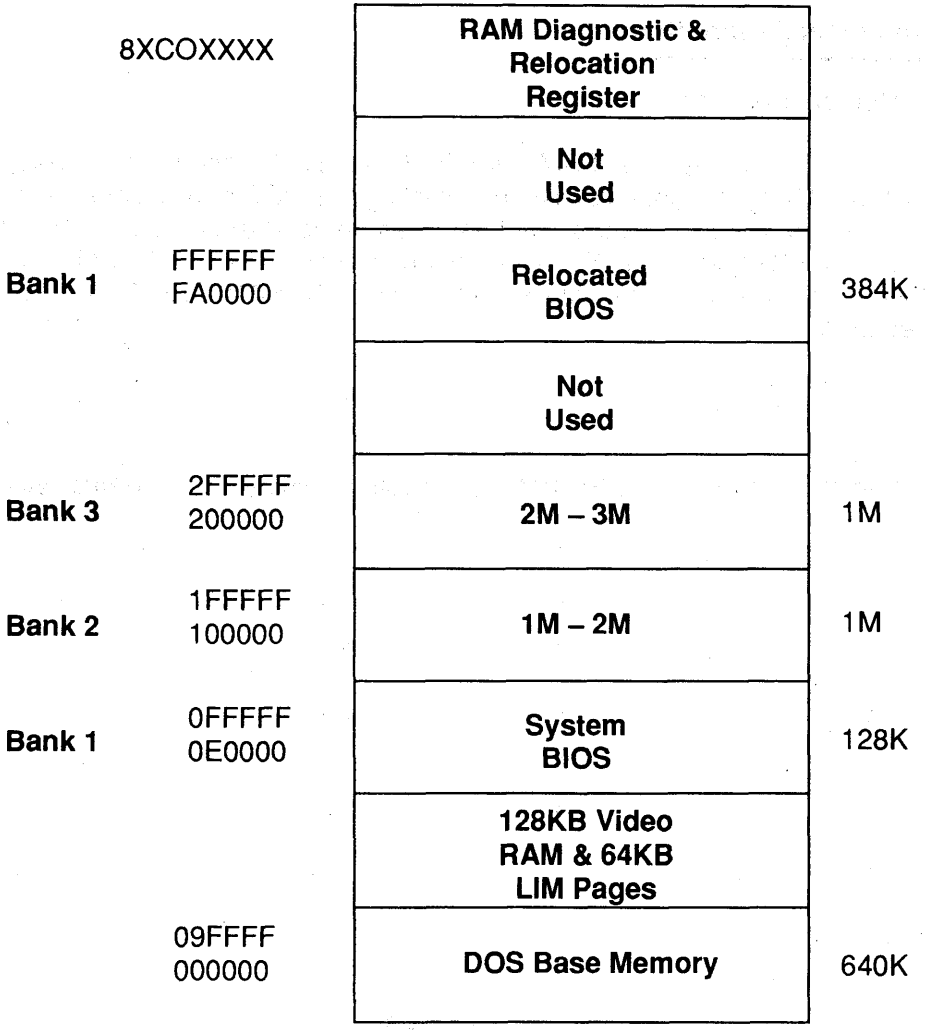


Figure 3. Memory Mapping when using 256K DRAM. M32* is active in all regions except in regions marked "not used" and video RAM and LIM pages.

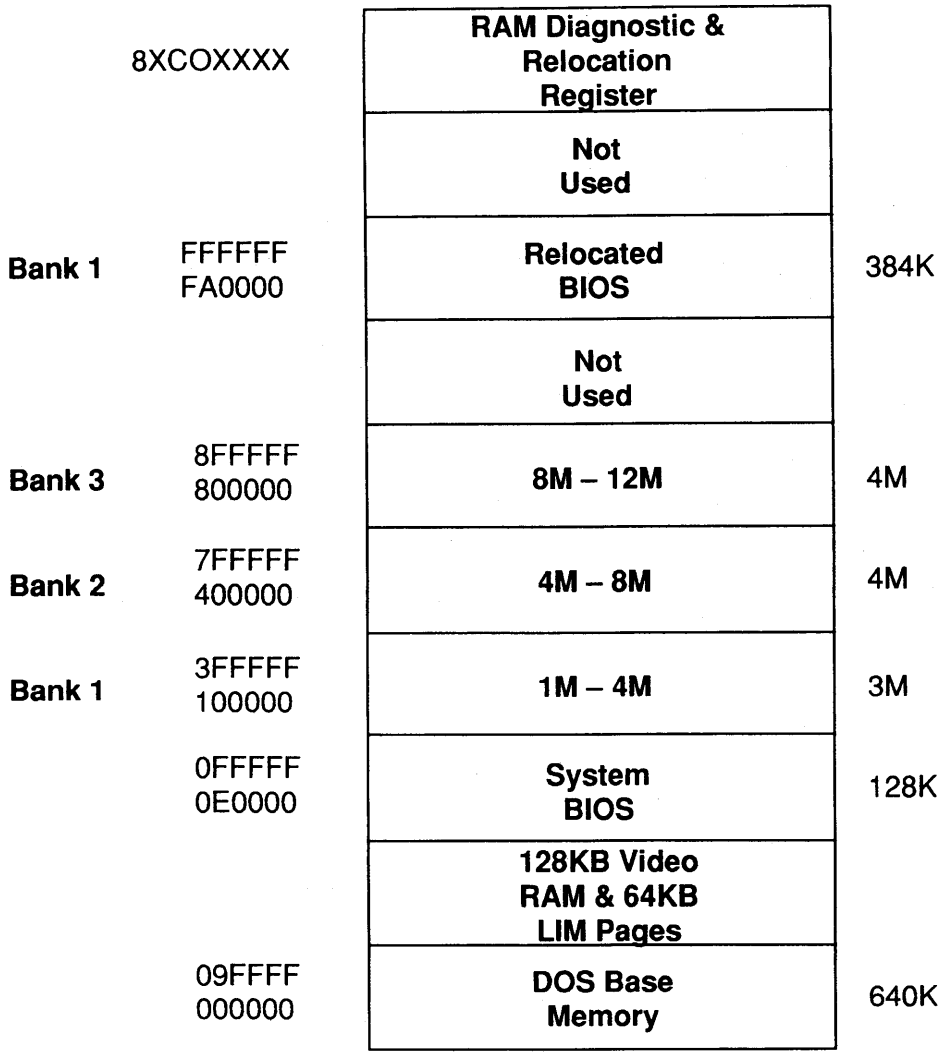


Figure 4. Memory Mapping when using 1M DRAM. M32* is active in all regions except in regions marked "not used" and video RAM and LIM pages.

(b) ROM Mapping:

Of the 384KB of memory addressed on top of the 16MB address space, the last 128KB has a special addressing feature. This 128-KB block, starting at address FE0000, can be relocated (mapped) via special hardware map registers to the system BIOS (0E0000 - 0FFFFF). When mapped, the 128-KB RAM block normally located at FE0000 can be addressed at either FE0000 or 0E0000. The ROM devices are not accessible while the RAM is mapped to the address space normally occupied by the ROMs.

In addition to this relocation capability, the 128KB block of RAM beginning at address FE0000 can be write-protected by special hardware registers on the system memory board. The relocation and write-protection capabilities allow the system ROM to be replaced by high-speed RAMs having the same contents (Shadow RAMs).

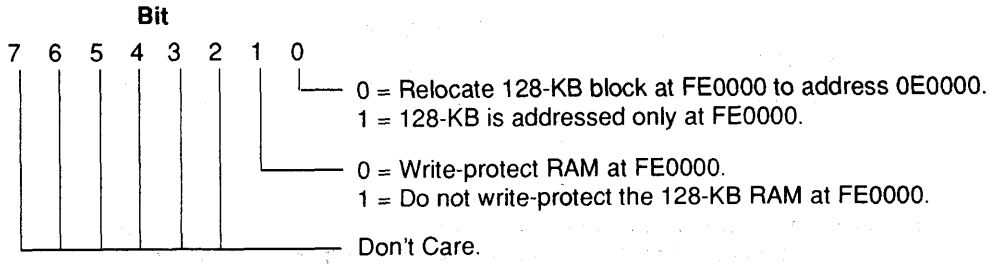
(c) Memory Mapped Registers:

UM82C388 has two memory-mapped registers: one is used in RAM relocation, the other is for RAM diagnostics

RAM relocation:

The address and contents of the special memory-mapped hardware register used in the RAM relocation are shown in the following bit map. This register is a write-only register:

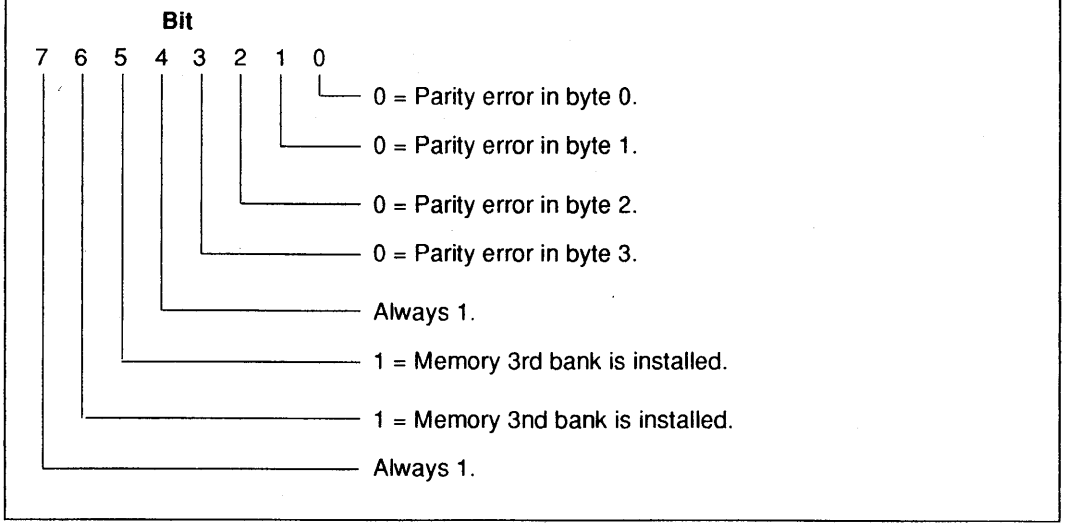
RAM Relocation --> Memory-Mapped Address 80C00000 (write only)



RAM Diagnostics:

The RAM diagnostics register helps test memory subsystems. This register allows a diagnostics program to read the state of memory configuration jumpers on the system memory board. The register also contains the status of the parity bits for each of the four bytes of a 32-bit memory access. RAMs can be tested very quickly, because they are performed by reading and writing 32-bit data patterns. When a parity error is detected, a diagnostics program uses the RAM diagnostics register to determine which byte in the 32-bit double-word caused the error. The address and contents of the memory-mapped diagnostics register are shown in the following bit map. This register is a read-only register. Writing to this register affects the contents of the RAM relocation register since they share the same memory location.

RAM Relocation --> Memory-Mapped Address 80C00000 (write only)



(d) Bus Cycle Status Definitions

Table 3 gives the bus cycle status definition for the MHLDA, M/IO* D/C*, and W/R* signals:

MHLDA	M/IO*	D/C*	W/R*	Cycle Type
0	0	0	0	CPU Interrupt Acknowledge
0	0	0	1	Invalid Cycle Type
0	0	1	0	CPU I/O Read
0	0	1	1	CPU I/O Write
0	1	0	0	CPU Memory Instruction Prefetch Read
0	1	0	1	CPU Halt or Shutdown
0	1	1	0	CPU Memory Data Read
0	1	1	1	CPU Memory Data Write
1	0	0	0	Invalid Cycle type
1	0	0	1	DRAM Refresh - 3 (see note)
1	0	1	0	DMA Memory Write
1	0	1	1	DMA Memory Read
1	1	0	0	Invalid Cycle Type
1	1	0	1	DRAM Refresh - 2 (see note)
1	1	1	0	Non-CPU Cycle - Transition State
1	1	1	1	DRAM Refresh - 1 (see note)

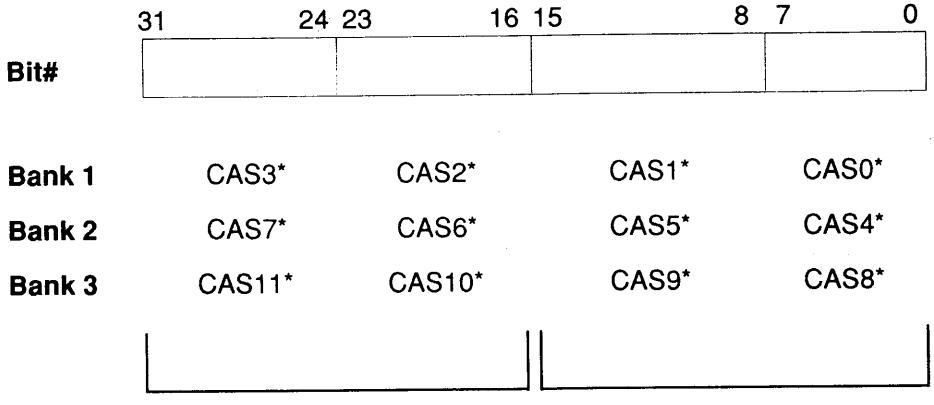
Note: DRAM Refresh Cycles follow the following sequence:
1 → 2 → 3 → 2 → 1

Table 3

(e) RAS, CAS signals and DRAM Module

In order to reduce loading for RAS and CAS signals, six RAS signals and twelve CAS signals are generated to drive three banks of DRAMs. The following tables illustrate the connection of RAS and CAS signals to different banks of DRAMs.

Bank 1	RAS0*,	RAS1*,	CAS0* - CAS3*
Bank 2	RAS2*,	RAS3*,	CAS4* - CAS7*
Bank 3	RAS4*,	RAS5*,	CAS8* - CAS11*



(f) DRAM Address corresponding to CPU Address

The following table illustrates the DRAM address corresponding to the CPU address when using 256K or 1M DRAMs.

	256K DRAM		1M DRAM	
DRAM Address	**Column**	**Row**	**Column**	**Row**
- DRA0	PA2	PA12	PA2	PA12
- DRA1	PA3	PA13	PA3	PA13
- DRA2	PA4	PA14	PA4	PA14
- DRA3	PA5	PA15	PA5	PA15
- DRA4	PA6	PA16	PA6	PA16
- DRA5	PA7	PA17	PA7	PA17
- DRA6	PA8	PA18	PA8	PA18
- DRA7	PA9	PA19	PA9	PA19
DRA8	PA10	PA11	PA10	PA20
DRA9	0	0	PA11	PA21

Note: DRA0 - DRA7 are in opposite phase with the real CPU address.

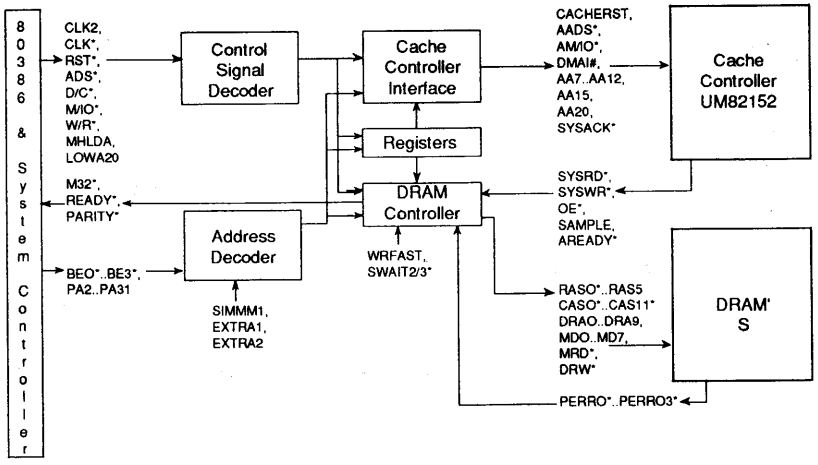
I General Description

The UM82C389 Cache Interface Chip is one of the UMC UM82C380 series High End AT (HEAT) chip set. As a DRAM controller, UM82C389 works in tandem with UM82152 Cache Controller to form an efficient cache memory subsystem. This highly integrated Cache Interface chip contains all necessary glue logic components to interface UM82152 directly to UM80386 CPU. It is also carefully tailored to be directly pin replaceable with the UM82C384 Page Memory Controller: one motherboard is sufficient for both Page/Cache modes.

II Features

- Supports a flexible system memory configuration:
  a) 1M, 2M or 3M using 256Kx1 DRAM
  b) 4M, 8M or 12M using 1Mx1 DRAM
- Uses normal page DRAM (Static column is unnecessary)
- Handles 80ns/100ns DRAM speed at 25MHz system speed
- Accepts short precharge time DRAM to boost system performance
- 120 pin flat package in 1.2μ CMOS technology

III Block Diagram



IV Pin Configuration

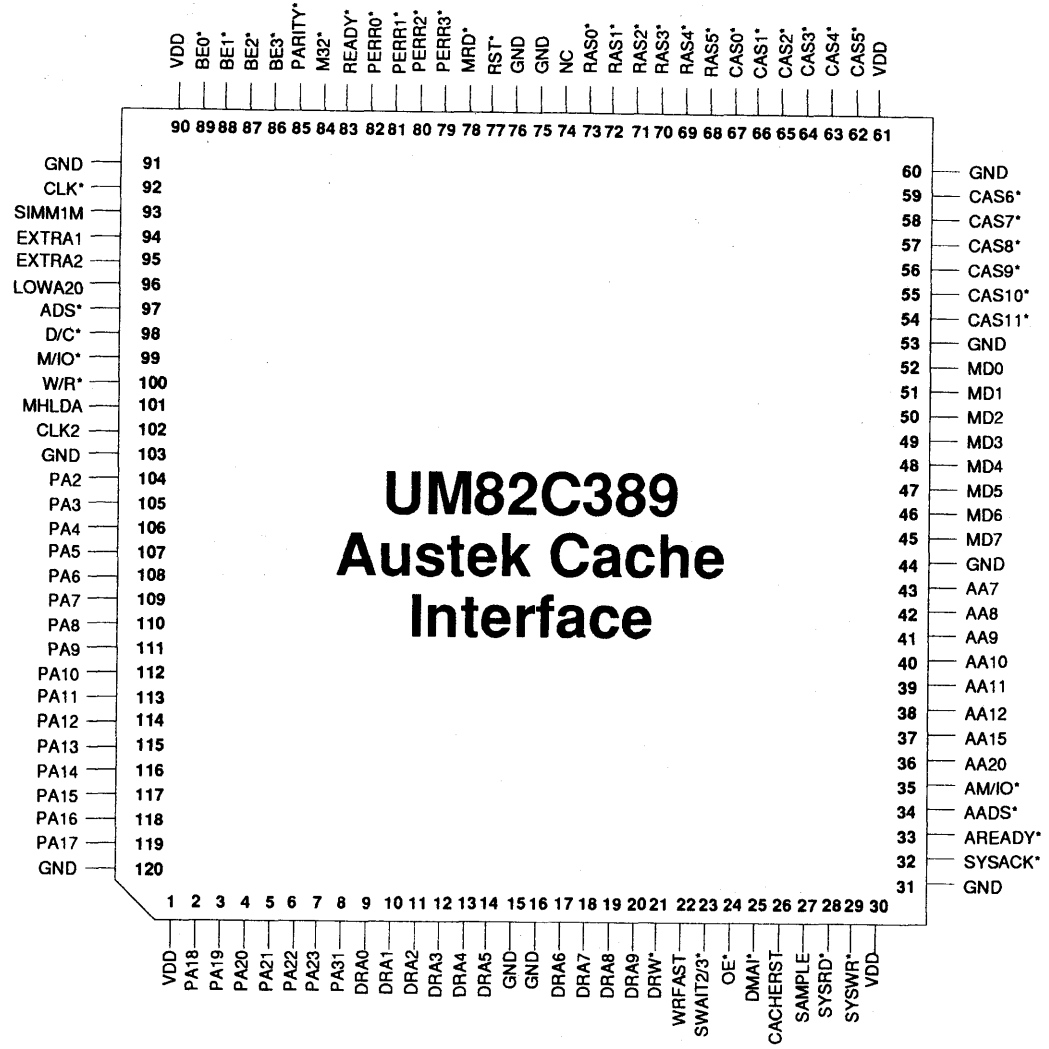


Figure 1. Pin Configuration

VI Functional Description

The Cache Interface has two major functions:

1) Intercepting and modifying all control signals between UM80386 CPU and the Cache Controller UM82152 for different bus cycles (Reset, Memory, I/O, DMA)

2) Working as DRAM controller underneath the Cache Controller

Following is the operation of Cache Interface in different bus cycles:

1) Reset: upon receiving active RST*, Cache Interface generates CACHERST signal correctly synchronized with CLK* for the Cache Controller.
The internal flip-flops of Cache Interface are also forced to initial known states.

2) I/O: Cache Interface converts all I/O cycles from UM80386 to memory cycles to Cache Controller.

3) Memory:

   a) Normal Memory: all control signals are passed directly to Cache Controller. If a miss occurs, DRAM Controller will be activated to transfer data from DRAM's to UM80386.
   b) Memory-Mapped I/O: only 2 devices are mapped; they are the Cache Controller and the Register of Cache Interface.
   c) Non-Existing Memory Locations: these cycles will be terminated and the corresponding entries in tag RAM will be invalidated to avoid data stalling.

4) D(irect) M(emory) A(ccess): during the DMA read cycles (i.e. data coming from DRAM), Cache controller is forced idle. However, during the DMA Write cycles, Cache Controller will watch over the address bus; if anyaddresses match any entries of tag RAM, the corresponding entries will be invalidated.

Cache Interface can be divided into 5 logic blocks: Control Signal Decoder, Address Decoder, Registers, Cache Controller Interface and DRAM Controller.

1) Control Signal Decoder: decodes all incoming control signals from 80386 to activate either Cache Controller or DRAM Controller depending on bus cycle (Reset, Memory, I/O, or DMA bus cycles).

2) Address Decoder: maps all incoming addresses to actual physical on board memory; activates M32* if existing memory locations are referred to.

3) Registers: store various options to program the Cache Controller Interface as well as the DRAM Controller.

4) Cache Controller Interface: provides all necessary signals to control Cache Controller.

5) DRAM Controller: generates all necessary signals to control DRAM such as R(ow) A(ddress) S(elect) C(olumn) A(dress) S(elect), transceiver direction control, parity generation & detection.

Memory Configurations

Because 24 bit address is used, only 16MB can be addressed. The minimum memory requirement is 1MB. This first 1MB is mapped into two regions: 640KB of base memory and 384KB located at the high end of the 16M address place. More memory can be added incrementally provided the following jumpers are setup correctly

SIMM1M	EXTRA 1	EXTRA 2	System Memory	DRAM Type
0	0	0	1M	
0	1	0	2M	256K
0	1	1	3M	
1	0	0	4M	
1	1	0	8M	1M
1	1	1	12M	
0	0	1	*Illegal	
1	0	1		

Figure 2. Memory Configuration Set Up

Different Memory Configurations are illustrated by Figures 3 & 4.

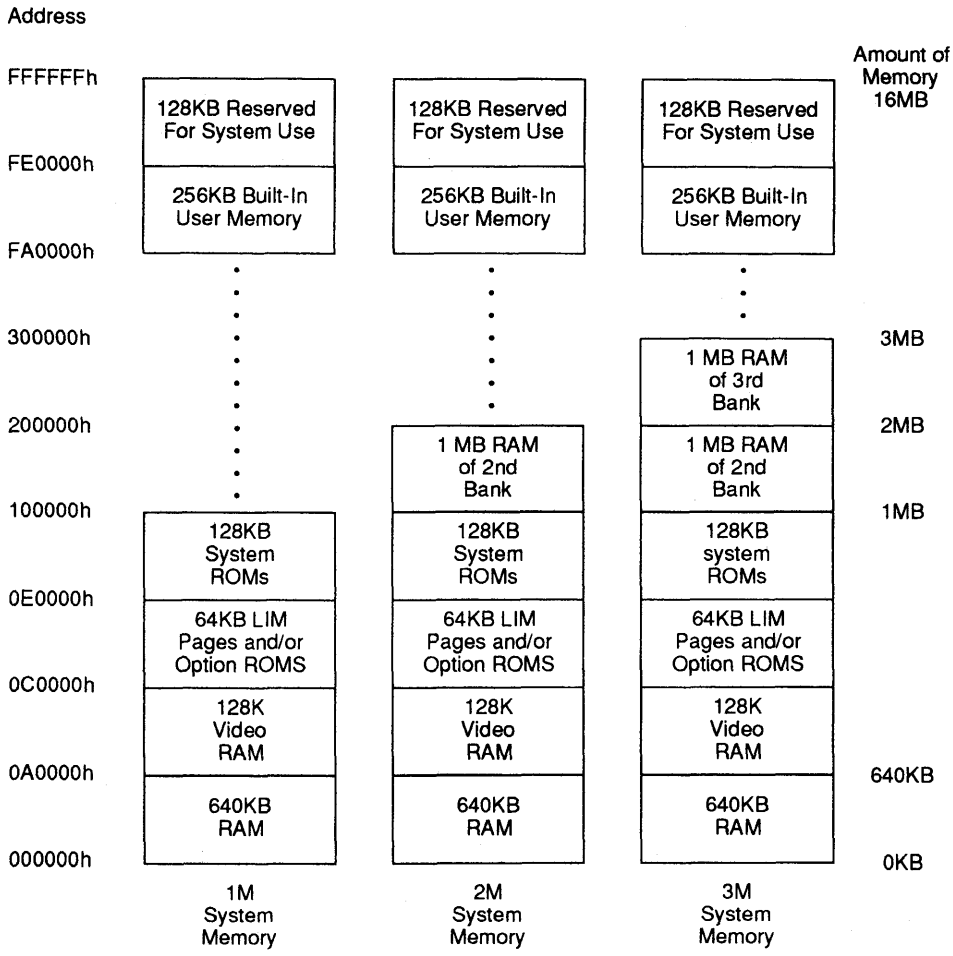


Figure 3. Memory Configuration Using 256Kx1 DRAM

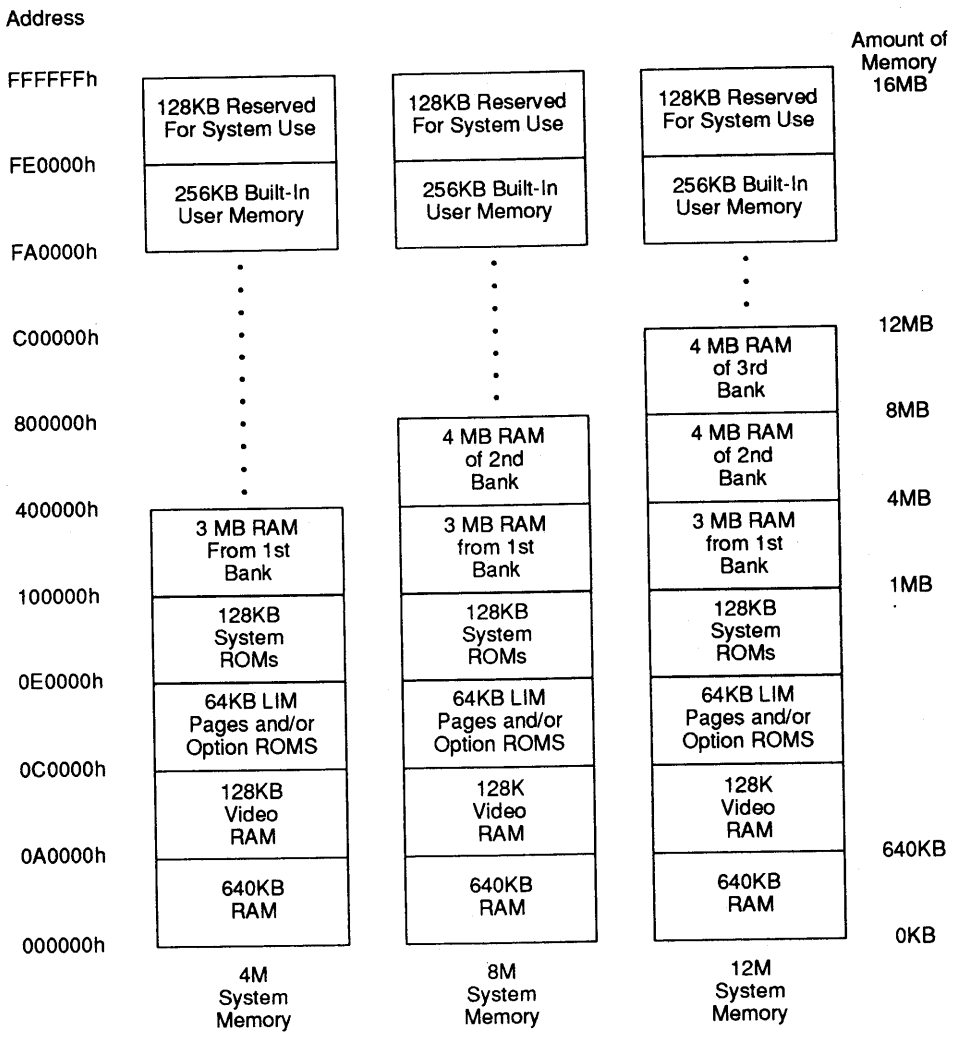


Figure 4. Memory Configuration Using 1Mx1 DRAM

ROM Mapping

Of the 384KB memory located at the end of the 16M address space, the bottom 128KB starting at FE0000h is called Shadow RAM. The Shadow RAM has 2 special features:

- Write-protected by controlling a special hardware register named CONTROL.
- Relocated via hardware register CONTROL to the system ROM's location (0E0000h - OFFFFFh); when mapped, this Shadow RAM can be addressed at locations FE0000h - FFFFFFh or 0E0000h - 0FFFh. The system ROM cannot be accessed any longer.

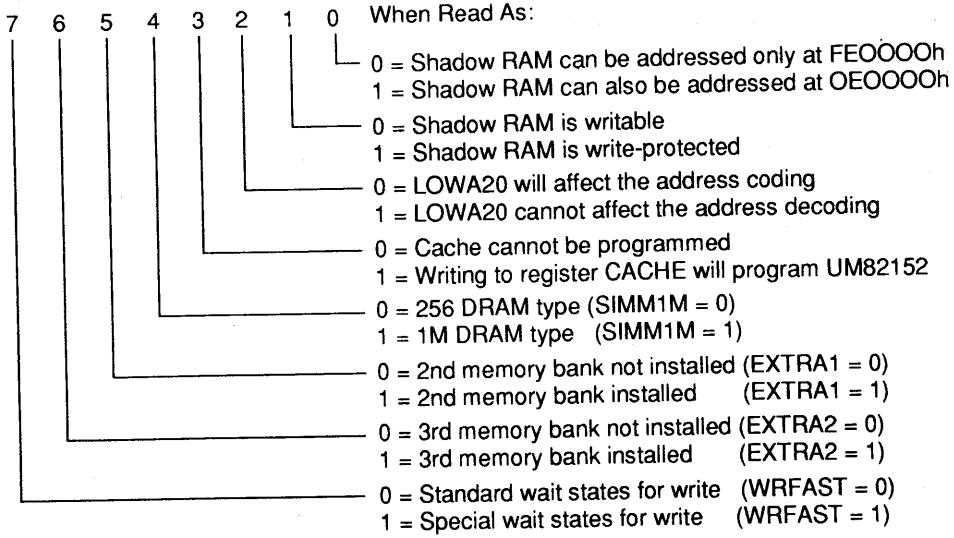
The relocation and write-protected capabilities allow the system ROM to be replaced with high speed RAM having the same contents (Shadow RAM)

Memory-Mapped Hardware Registers

There are 2 registers: CONTROL for diagnostics and control, CACHE for programming the cache controller.

- CONTROL register (address 80C00000h): is partitioned into 2 segments: low nibble is read/write while the high nibble is read only.

IMPORTANT: When writing to CONTROL register, all the bits of low nibble will be complemented (i.e. writing 1 will be read later as 0 and vice versa)



- CACHE register (address 8030xxxxh): actually spreads out 64K memory block starting at 80300000h. When bit 3 of CONTROL register is 1, writing to these locations will be interpreted by the UM82152 as a programming command (check UM82152 data sheet)

Operation

Because the UM82152 always tries to operate the CPU in pipeline mode, the actual length of a bus cycle varies. Here is the summary of wait states for different configurations and situations:

SWAIT 2/3#	WRFAST	Read/ Write	Hit/ Miss	Single/ Pipeline	Wait States	Number of CLK2 Cycles	Notes:
0/1	0/1	Read	Hit	Single	0	6	
0	0/1	Read	Miss	Single	3	12	
0	0	Write	Hit/Miss	Single	3	12	
0	1	Write	Hit/Miss	Single	3/2	12/10	10 if previous cycle is read
1	0/1	Read	Miss	Single	2	10	
1	0	Write	Hit/Miss	Single	2	10	
1	1	Write	Hit/Miss	Single	2/1	10/8	8 if previous cycle is read

Note: For pipeline mode, subtract 2 from the number of CLK2 cycles of the corresponding bus cycle since ADS# is hidden from previous bus cycle (i.e., Read Hit in pipeline mode is 0 wait states and lasts 4 CLK2 cycles).

Figure 5. Wait State Summary

General Information

Description	Page
Guide to MOS Handling	B-3
Quality/Reliability	B-4
Packaging Information	B-6
International Representatives & Distributors	B-33

UMC

Guide To MOS Handling

We at UMC are constantly looking for more effective ways to provide protection for MOS devices. Present configurations of protective devices are the result of years of research and review of field problems.

Even though oxide breakdown may happen far beyond the voltage levels encountered in normal operation, excessive voltages can cause permanent damage. Though we have evolved the best-designed protective devices currently possible, we recognize that they are not 100-percent effective. What is?

A large number of failed returns have been due to misapplication of biases. In particular, forward bias conditions cause excessive current through the protective devices, which in turn will vaporize metal lines to the inputs. Careful inspection of the device date sheets and proper pin designation should help reduce such failures.

Gate ruptures caused by static discharge have also accounted for a large percentage of device failures in customers' manufacturing areas. Precautions should be taken to minimize the possibility of static charges during handling and assembly of MOS circuits.

The following guidelines for handling MOS devices are offered to assist our customers in reducing the hazards which may be detrimental to MOS circuits. Precautions listed herein are used at UMC.

A. Cover all benches used for assembly or test of MOS circuits with conductive sheets. Warning: Never expose an operator directly to a hard electrical ground. For safety reasons the operator must have a resistance of at least 100K Ohms between himself and hard electrical ground.

B. Have grounding plates on doors and/or floors of all entrances to work areas. These must be contacted by people entering the areas.

C. Have employees wear conductive straps inside and outside their shoes so that body charges are grounded when entering the work area.

D. Have employees wear anti-static neutralized smocks to eliminate the possibility of static charges being generated by the friction of normal wear.

E. Have employees wear cotton gloves while handling parts. Nylon gloves and rubber finger cots are not allowed.

F. To help reduce generation of static voltages, humidity should be controlled at a minimum of 35 percent.

G. Transport all parts in conductive trays. Do not use plastic containers. Store axial leaded parts in conductive foam, e.g. Velofoam #7611.

H. All equipment used in the assembly area must be thoroughly grounded. Attention should be given to equipment that may be inductively coupled and generate stray voltages. Soldering irons must have grounded tips. Grounding must also be provided for solder pots, reflow soldering equipment, etc.

I. It is advisable to place a grounding clip across the finger of the board to ground all leads and lines on the board during insertion of ICs to printed circuit boards.

J. Use of carpets is discouraged in work areas, but in other areas, carpets may be treated with anti-static solution to reduce static generation.

K. Handle MOS parts on conductive surfaces. The handler must touch the conductive surface first before touching the parts.

L. No power should be applied to the socket or board when the MOS device is being inserted. This permits any static charge accumulated on the MOS device to be safely removed before power is applied.

M. Do not handle MOS by their leads unless absolutely necessary. Handle MOS devices by their packages as much as possible.

N. In general, materials prone to static charge accumulation should not come in contact with MOS devices.

Observe these precautions even when an MOS device is suspected of being defective. The real cause of failure cannot be accurately determined if the device is damaged because of static charge build-up.

IMPORTANT REMINDER: EVEN THE MOST ELABORATE PHYSICAL PREVENTION TECHNIQUES WILL NOT ELIMINATE DEVICE FAILURE IF PERSONNEL ARE NOT FULLY TRAINED IN PROPER HANDLING OF MOS DEVICES.

For further information, please contact Quality Assurance/ Reliability Department

United Microelectronics Corp.
No. 10, Innovation First Road,
Science-Based Industrial Park
Hsinchu City, Taiwan, Republic of China

UMC

Quality/Reliability

Design Reliability

Before a new design is approved for production, UMC takes into consideration factors which may affect reliability such as circuit layout, element structures and characteristics, final application, process requirements and assembly, and packaging specs. These aspects are reviewed in the light of quality and reliability standards. Initially, all factors are evaluated on a worst case basis and results are monitored at all stages of the development cycle. These include product planning, layout, mask design, pilot production, testing and packaging. Only when established quality and reliability standards are met in consecutive pilot runs is the product released for production start-up.

Reliability Qualification Tests

The reliability tests include life testing, environmental testing and mechanical testing. These tests are performed in accordance with MIL-STD-883C as the prime standard and with EIAJ-IC-121, where applicable. When a new technique or product is introduced, the UMC reliability engineering department conducts approval and any new process or product is approved only if it meets specified reliability standards and acceptance limits of related tests. Table 1. gives the typical conditions for reliability testing.

Quality Conformance Test

After initial product evaluations are successfully completed, regular testing of volume production is performed on a 100% basis so that test specifications are met in all respects. Additionally, production lots must pass the sampling quality conformance test. Prior to this, the appropriate screening tests are performed on each lot of product.

Engineering Change Control

Engineering approval testing determines the practicality and usability of a process or product.

Production approval is given only if reliability evaluations are successfully met. No device or process change at UMC can be implemented unless full customer notification and approval is received and the change is verified acceptable by the reliability engineering department.

Table 1. Reliability Test Items & Conditions

	Test Items	Test Conditions	Reference Standard	Sample Size	Acc. / Rej.	LTPD
Life Test	Operating Life	T_A=125°C, 1000 hours	MIL-STD-883C 1005.7	55	1/2	7%
	Bias Life	T_A=125°C, 1000 hours	MIL-STD-883C 1005.7	55	1/2	7%
	Temperature Humidity with Bias	T_A=85°C, 85% R.H (rated voltage applied), 1000 hours	EIAJ-IC-121 17	55	1/2	7%

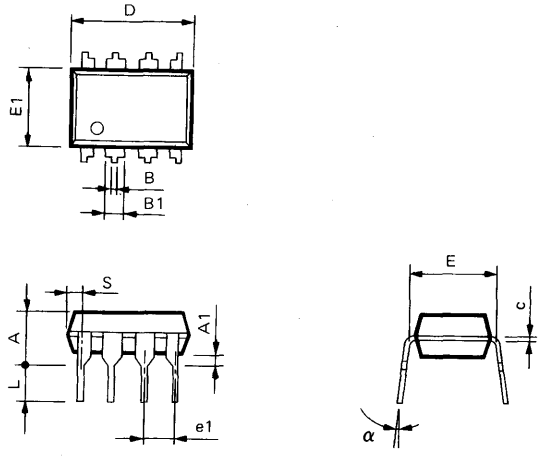
Table 1. Reliability Test Items & Conditions (Continued)

	Test Items	Test Conditions	Reference Standard	Sample Size	Acc./Rej.	LTPD
Environmental Test	High Temperature Storage	T_A=150°C, 1000 hours	MIL-STD-883C 1008.2	55	1/2	7%
	Low Temperature Storage	T_A=−65°C, 1000 hours	EIAJ-IC-121 16	55	1/2	7%
	Thermal Shock	−65°C ⇌ 150°C 5 min within 10 sec 5 min 100 Cycles	MIL-STD-883C 1011.8	38	1/2	10%
	Temperature Cycling	−65°C ⇌ 150°C 10 min 10 min 200 Cycles	MIL-STD-883C 1010.7	38	1/2	10%
	Pressure Cooker	121°C, 15 psig (2 atm) 100% R.H. 216 hours	EIAJ-IC-121 18	38	1/2	10%
	Salt Atmosphere	35°C, 5% NaCl 24 hours	MIL-STD-883C 1009.8	38	1/2	10%
	Resistance To Soldering Heat	260°C, 10 seconds (Solder Bath)	EIAJ-IC-121 11	15	0/1	15%
Mechanical Test	Lead Fatigue	Bend 90°, 0.229±0.014kg 3 Cycles	MIL-STD-883C 2004.5	15	0/1	15%
	Solderability	230°C + 5°C, 5 seconds Flux used	EIAJ-IC-121 02	15	0/1	15%
	Vibration	100-2000HZ, 20G 4 min/cycle, X.Y.Z Direction	MIL-STD-883C 2007.1	15	0/1	15%
	Mechanical Shock	1500G, 0.5 ms X.Y.Z Direction	MIL-STD-883C 2002.2	15	0/1	15%
	Constant Acceleration	3000G, 60 sec	MIL-STD-883C 2001.2	15	0/1	15%

UMC

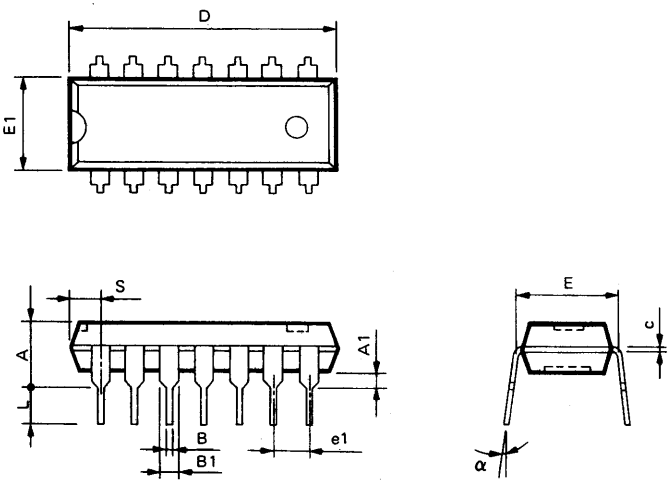
PACKAGING INFORMATION

P- DIP 8L Outline Dimension



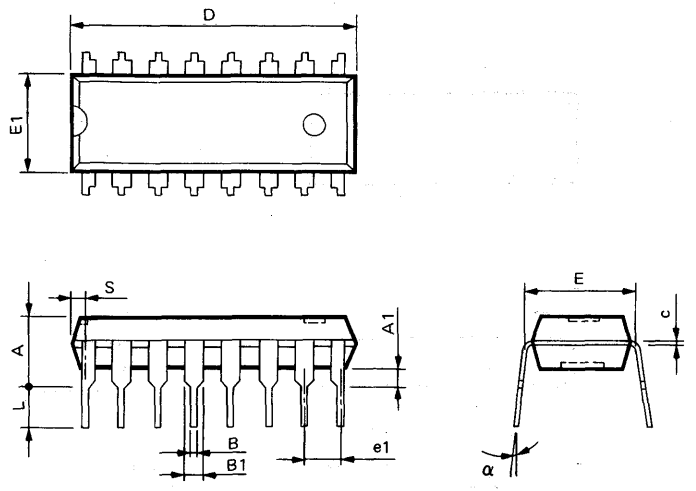
Symbol	Dimensions in inch	Dimensions in mm
A	0.175 Max.	4.445 Max.
A1	0.010 Min.	0.254 Min.
B	$0.018^{+\ 0.004}_{-\ 0.002}$	$0.457^{+\ 0.102}_{-\ 0.051}$
B1	$0.060^{+\ 0.004}_{-\ 0.002}$	$1.524^{+\ 0.102}_{-\ 0.051}$
c	$0.010^{+\ 0.004}_{-\ 0.002}$	$0.254^{+\ 0.102}_{-\ 0.051}$
D	0.360 (0.370 Max.)	9.144 (9.398 Max.)
E	0.300 ± 0.010	7.620 ± 0.254
E1	0.250 (0.275 Max.)	6.350 (6.985 Max.)
e1	0.100 ± 0.010	2.540 ± 0.254
L	0.130 ± 0.010	3.302 ± 0.254
α	0° ~ 15°	0° ~ 15°
S	0.040 Max.	1.016 Max.

P- DIP 14L Outline Dimension



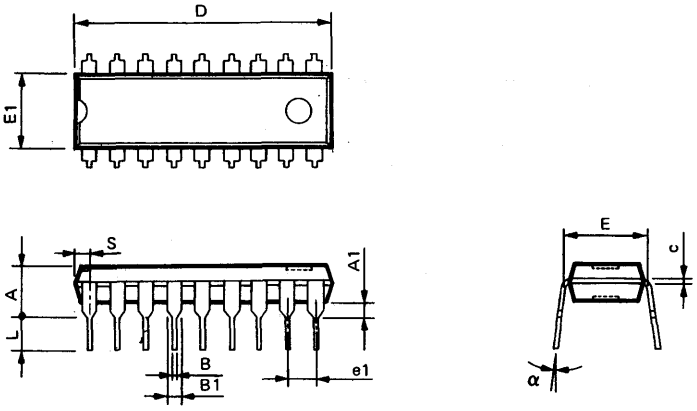
Symbol	Dimensions in inch	Dimensions in mm
A	0.175 Max.	4.445 Max.
A1	0.010 Min.	0.254 Min.
B	$0.018^{+0.004}_{-0.002}$	$0.457^{+0.102}_{-0.051}$
B1	$0.060^{+0.004}_{-0.002}$	$1.524^{+0.102}_{-0.051}$
c	$0.010^{+0.004}_{-0.002}$	$0.254^{+0.102}_{-0.051}$
D	0.750 (0.770 Max.)	19.050 (19.558 Max.)
E	0.300 ± 0.010	7.620 ± 0.254
E1	0.250 (0.275 Max.)	6.350 (6.985 Max.)
e1	0.100 ± 0.010	2.540 ± 0.254
L	0.130 ± 0.010	3.302 ± 0.254
α	0° ~ 15°	0° ~ 15°
S	0.090 Max.	2.286 Max.

P- DIP 16L Outline Dimension



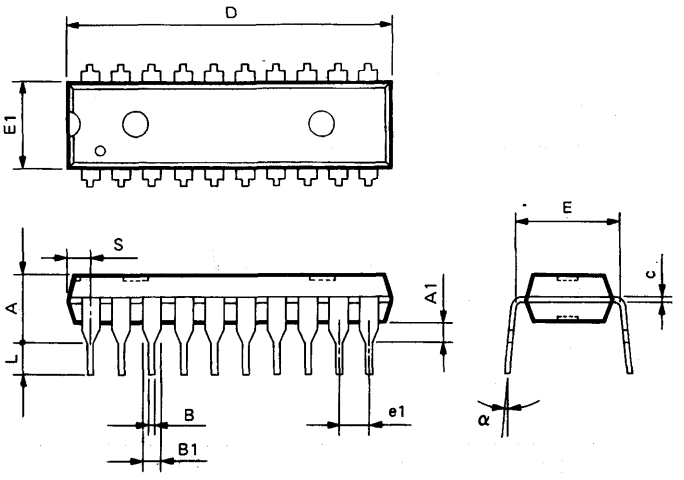
Symbol	Dimensions in inch	Dimensions in mm
A	0.175 Max.	4.445 Max.
A1	0.010 Min.	0.254 Min.
B	$0.018^{+0.004}_{-0.002}$	$0.457^{+0.102}_{-0.051}$
B1	$0.060^{+0.004}_{-0.002}$	$1.524^{+0.102}_{-0.051}$
c	$0.010^{+0.004}_{-0.002}$	$0.254^{+0.102}_{-0.051}$
D	0.750 (0.770 Max.)	19.050 (19.558 Max.)
E	0.300 ± 0.010	7.620 ± 0.254
E1	0.250 (0.275 Max.)	6.350 (6.985 Max.)
e1	0.100 ± 0.010	2.540 ± 0.254
L	0.130 ± 0.010	3.302 ± 0.254
α	0° ~ 15°	0° ~ 15°
S	0.040 Max.	1.016 Max.

P- DIP 18L Outline Dimension



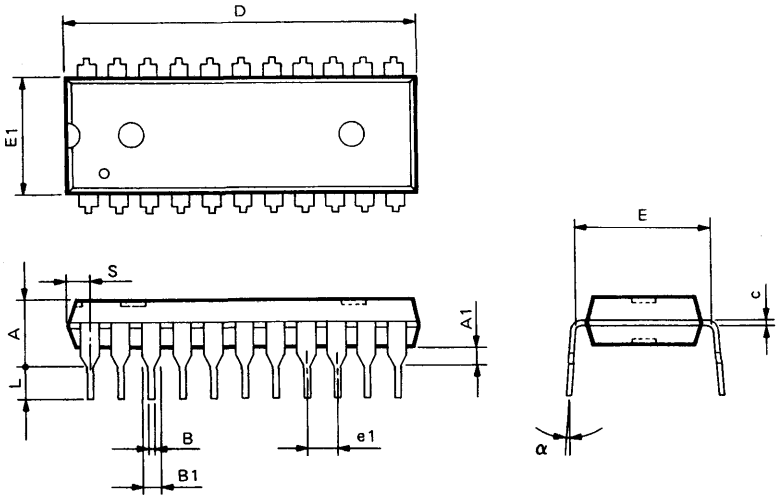
Symbol	Dimensions in inch	Dimensions in mm
A	0.175 Max.	4.445 Max.
A1	0.010 Min.	0.254 Min.
B	$0.018^{+0.004}_{-0.002}$	$0.457^{+0.102}_{-0.051}$
B1	$0.060^{+0.004}_{-0.002}$	$1.524^{+0.102}_{-0.051}$
c	$0.010^{+0.004}_{-0.002}$	$0.254^{+0.102}_{-0.051}$
D	0.900 (0.910 Max.)	22.860 (23.114 Max.)
E	0.300 ± 0.010	7.620 ± 0.254
E1	0.250 (0.275 Max.)	6.350 (6.985 Max.)
e1	0.100 ± 0.010	2.540 ± 0.254
L	0.130 ± 0.010	3.302 ± 0.254
α	0° ~ 15°	0° ~ 15°
S	0.060 Max.	1.524 Max.

P-DIP 20L Outline Dimension



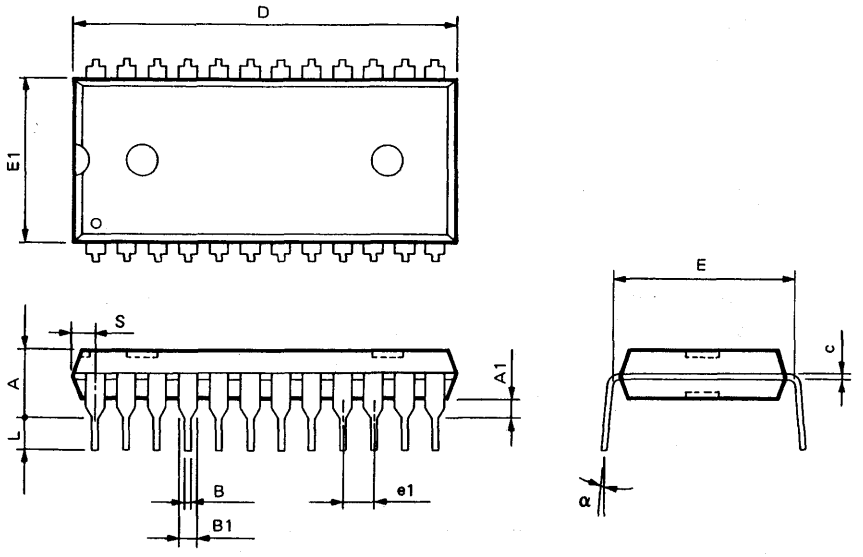
Symbol	Dimensions in inch	Dimensions in mm
A	0.175 Max.	4.445 Max.
A1	0.010 Min.	0.254 Min.
B	$0.018^{+\ 0.004}_{-\ 0.002}$	$0.457^{+\ 0.102}_{-\ 0.051}$
B1	$0.060^{+\ 0.004}_{-\ 0.002}$	$1.524^{+\ 0.102}_{-\ 0.051}$
c	$0.010^{+\ 0.004}_{-\ 0.002}$	$0.254^{+\ 0.102}_{-\ 0.051}$
D	1.026 (1.040 Max.)	26.060 (26.416 Max.)
E	0.300 ± 0.010	7.620 ± 0.254
E1	0.250 (0.275 Max.)	6.350 (6.985 Max.)
e1	0.100 ± 0.010	2.540 ± 0.254
L	0.130 ± 0.010	3.302 ± 0.254
α	0° ~ 15°	0° ~ 15°
S	0.075 Max.	1.905 Max.

P-DIP 22L Outline Dimension



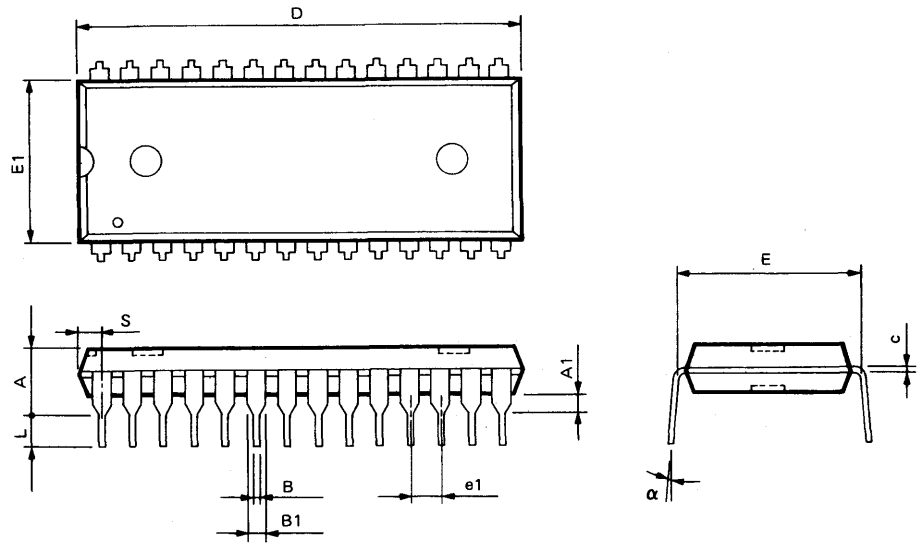
Symbol	Dimensions in inch	Dimensions in mm
A	0.190 max.	4.826 Max.
A1	0.020 Min.	0.508 Min.
B	$0.018^{+\ 0.004}_{-\ 0.002}$	$0.457^{+\ 0.102}_{-\ 0.051}$
B1	$0.060^{+\ 0.004}_{-\ 0.002}$	$1.524^{+\ 0.102}_{-\ 0.051}$
c	$0.010^{+\ 0.004}_{-\ 0.002}$	$0.254^{+\ 0.102}_{-\ 0.051}$
D	1.090 (1.120 Max.)	27.686 (28.448 Max.)
E	0.400 ± 0.010	10.160 ± 0.254
E1	0.350 (0.375 Max.)	8.890 (9.525 Max.)
e1	0.100 ± 0.010	2.540 ± 0.254
L	0.130 ± 0.010	3.302 ± 0.254
α	0° ~ 15°	0° ~ 15°
S	0.065 Max.	1.651 Max.

P-DIP 24L Outline Dimension



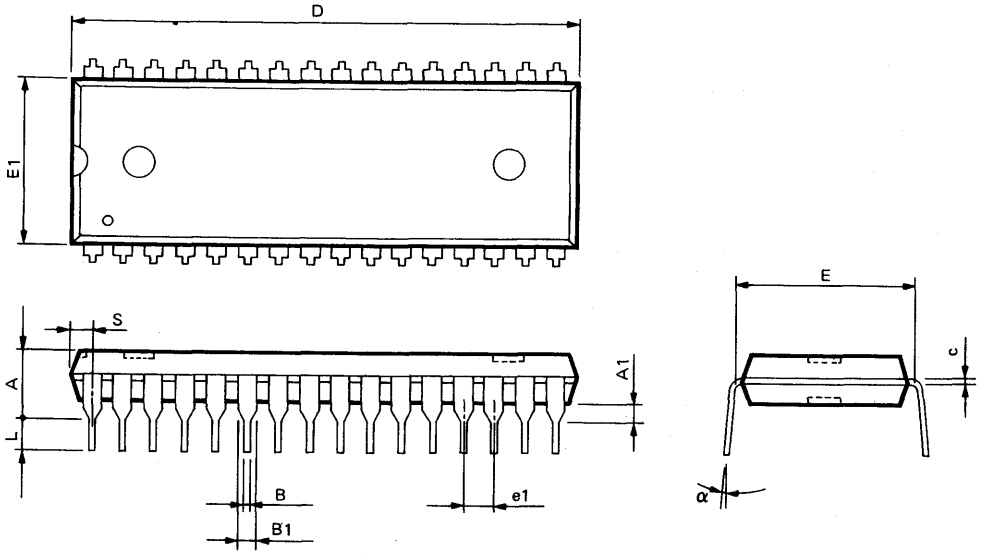
Symbol	Dimensions in inch	Dimensions in mm
A	0.210 Max.	5.334 Max.
A1	0.010 Min.	0.254 Min.
B	$0.018^{+0.004}_{-0.002}$	$0.457^{+0.102}_{-0.051}$
B1	$0.060^{+0.004}_{-0.002}$	$1.524^{+0.102}_{-0.051}$
c	$0.010^{+0.004}_{-0.002}$	$0.254^{+0.102}_{-0.051}$
D	1.250 (1.260 Max.)	31.750 (32.004 Max.)
E	0.600 ± 0.010	15.240 ± 0.254
E1	0.550 (0.575 Max.)	13.970 (14.605 Max.)
e1	0.100 ± 0.010	2.540 ± 0.254
L	0.130 ± 0.010	3.302 ± 0.254
α	0° ~ 15°	0° ~ 15°
S	0.085 Max.	2.159 Max.

P- DIP 28L Outline Dimension



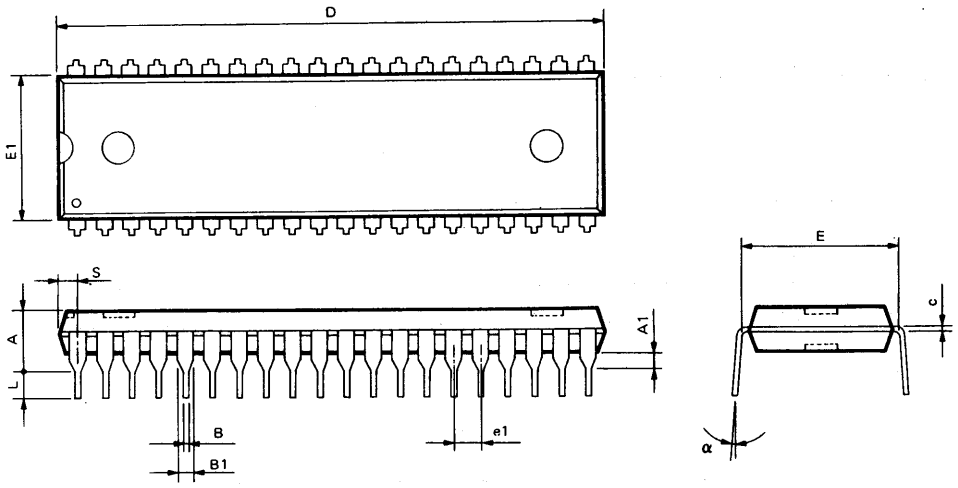
Symbol	Dimensions in inch	Dimensions in mm
A	0.210 Max.	5.334 Max.
A1	0.010 Min.	0.254 Min.
B	$0.018^{+0.004}_{-0.002}$	$0.457^{+0.102}_{-0.051}$
B1	$0.060^{+0.004}_{-0.002}$	$1.524^{+0.102}_{-0.051}$
c	$0.010^{+0.004}_{-0.002}$	$0.254^{+0.102}_{-0.051}$
D	1.460 (1.470 Max.)	37.084 (37.338 Max.)
E	0.600 ± 0.010	15.240 ± 0.254
E1	0.545 (0.575 Max.)	13.843 (14.605 Max.)
e1	0.100 ± 0.010	2.540 ± 0.254
L	0.130 ± 0.010	3.302 ± 0.254
α	0° ~ 15°	0° ~ 15°
S	0.090 Max.	2.286 Max.

P- DIP 32L Outline Dimension



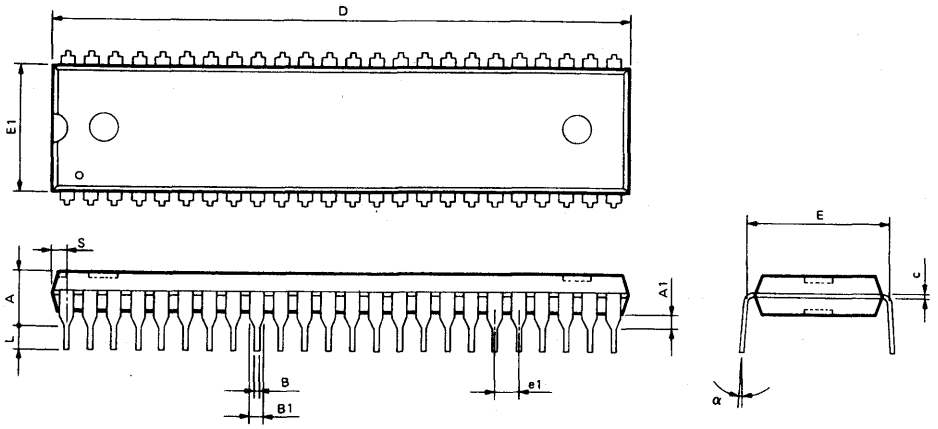
Symbol	Dimensions in inch	Dimensions in mm
A	0.210 Max.	5.334 Max.
A1	0.010 Min.	0.254 Min.
B	$0.018^{+0.004}_{-0.002}$	$0.457^{+0.102}_{-0.051}$
B1	$0.050^{+0.004}_{-0.002}$	$1.270^{+0.102}_{-0.051}$
c	$0.010^{+0.004}_{-0.002}$	$0.254^{+0.102}_{-0.051}$
D	1.650 (1.660 Max.)	41.910 (42.164 Max.)
E	0.600 ± 0.010	15.240 ± 0.254
E1	0.550 (0.575 Max.)	13.970 (14.605 Max.)
e1	0.100 ± 0.010	2.540 ± 0.254
L	0.130 ± 0.010	3.302 ± 0.254
α	0° ~ 15°	0° ~ 15°
S	0.085 Max.	2.159 Max.

P-DIP 40L Outline Dimension



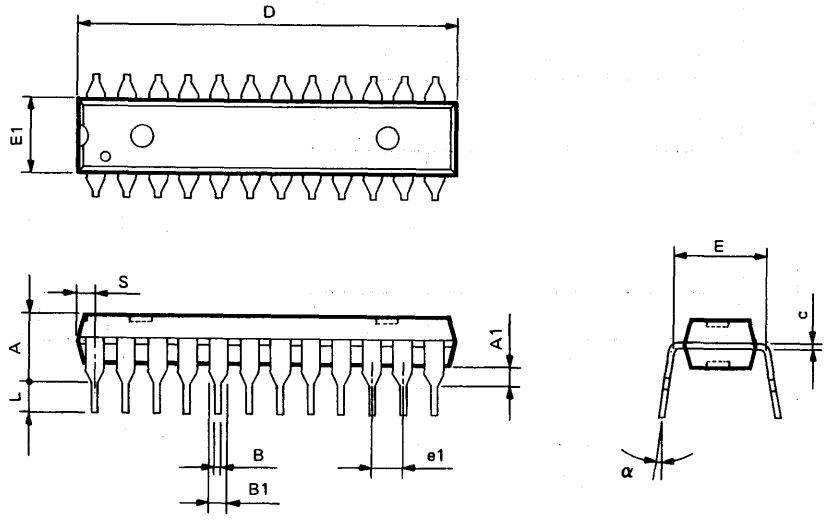
Symbol	Dimensions in inch	Dimensions in mm
A	0.210 Max.	5.334 Max.
A1	0.010 Min.	0.254 Min.
B	$0.018^{+\ 0.004}_{-\ 0.002}$	$0.457^{+\ 0.102}_{-\ 0.051}$
B1	$0.050^{+\ 0.004}_{-\ 0.002}$	$1.270^{+\ 0.102}_{-\ 0.051}$
c	$0.010^{+\ 0.004}_{-\ 0.002}$	$0.254^{+\ 0.102}_{-\ 0.051}$
D	2.055 (2.070 Max.)	52.197 (52.578 Max.)
E	0.600 ± 0.010	15.240 ± 0.254
E1	0.550 (0.575 Max.)	13.970 (14.605 Max.)
e1	0.100 ± 0.010	2.540 ± 0.254
L	0.130 ± 0.010	3.302 ± 0.254
α	0° ~ 15°	0° ~ 15°
S	0.090 Max.	2.286 Max.

P-DIP 48L Outline Dimension



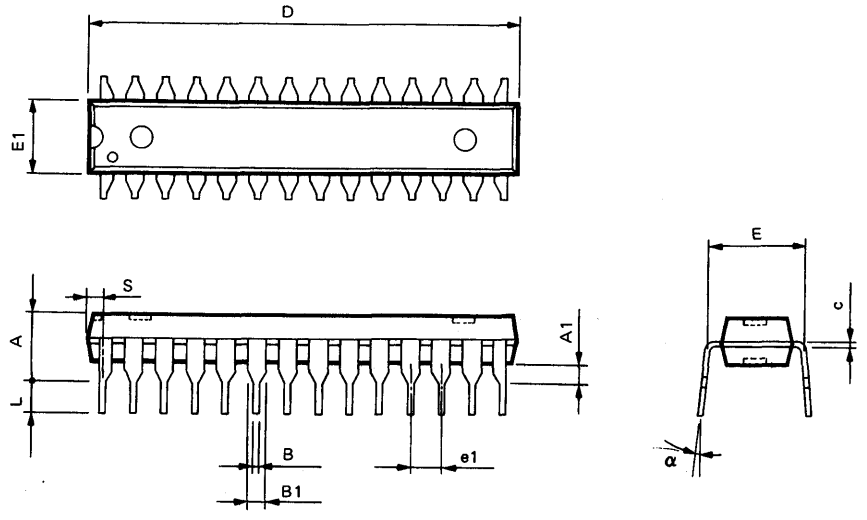
Symbol	Dimensions in inch	Dimensions in mm
A	0.210 Max.	5.334 Max.
A1	0.010 Min.	0.254 Min.
B	$0.018^{+0.004}_{-0.002}$	$0.457^{+0.102}_{-0.051}$
B1	$0.050^{+0.004}_{-0.002}$	$1.270^{+0.102}_{-0.051}$
c	$0.010^{+0.004}_{-0.002}$	$0.254^{+0.102}_{-0.051}$
D	2.450 (2.460 Max.)	62.230 (62.484 Max.)
E	0.600 ± 0.010	15.240 ± 0.254
E1	0.550 (0.575 Max.)	13.970 (14.605 Max.)
e1	0.100 ± 0.010	2.540 ± 0.254
L	0.130 ± 0.010	3.302 ± 0.254
α	0° ~ 15°	0° ~ 15°
S	0.085 Max.	2.159 Max.

Skinny 24L Outline Dimension



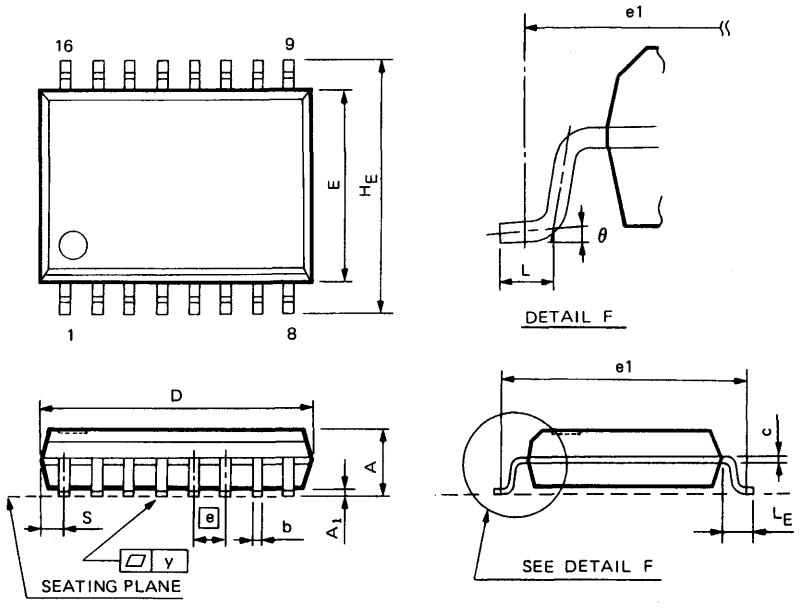
Symbol	Dimensions in inch	Dimensions in mm
A	0.175 Max.	4.445 Max.
A1	0.010 Min.	0.254 Min.
B	$0.018^{+0.004}_{-0.002}$	$0.457^{+0.102}_{-0.051}$
B1	$0.060^{+0.004}_{-0.002}$	$1.524^{+0.102}_{-0.051}$
c	$0.010^{+0.004}_{-0.002}$	$0.254^{+0.102}_{-0.051}$
D	1.256 (1.266 Max.)	31.902 (32.156 Max.)
E	0.300 ± 0.010	7.620 ± 0.254
E1	0.258 (0.285 Max.)	6.553 (7.239 Max.)
e1	0.100 ± 0.010	2.540 ± 0.254
L	0.130 ± 0.010	3.302 ± 0.254
α	0° ~ 15°	0° ~ 15°
S	0.088 Max.	2.235 Max.

Skinny 28L Outline Dimension



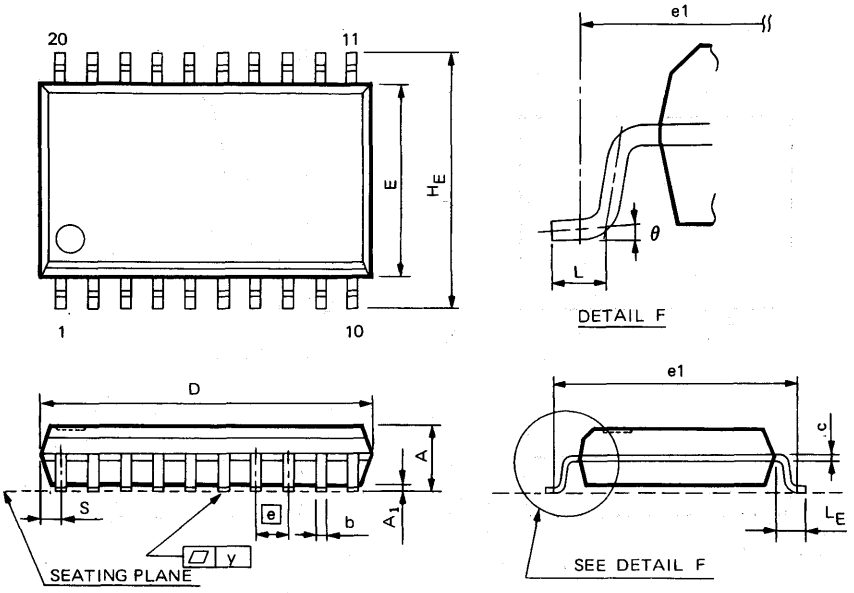
Symbol	Dimensions in inch	Dimensions in mm
A	0.175 Max.	4.445 Max.
A1	0.010 Min.	0.254 Min.
B	$0.018^{+0.004}_{-0.002}$	$0.457^{+0.102}_{-0.051}$
B1	$0.060^{+0.004}_{-0.002}$	$1.524^{+0.102}_{-0.051}$
c	$0.010^{+0.004}_{-0.002}$	$0.254^{+0.102}_{-0.051}$
D	1.388 (1.400 Max.)	35.255 (35.560 Max.)
E	0.310 ± 0.010	7.874 ± 0.254
E1	0.288 (0.310 Max.)	7.315 (7.874 Max.)
e1	0.100 ± 0.010	2.540 ± 0.254
L	0.130 ± 0.010	3.302 ± 0.254
α	0° ~ 15	0° ~ 15°
S	0.055 Max.	1.397 Max.

SO 16L Outline Dimension



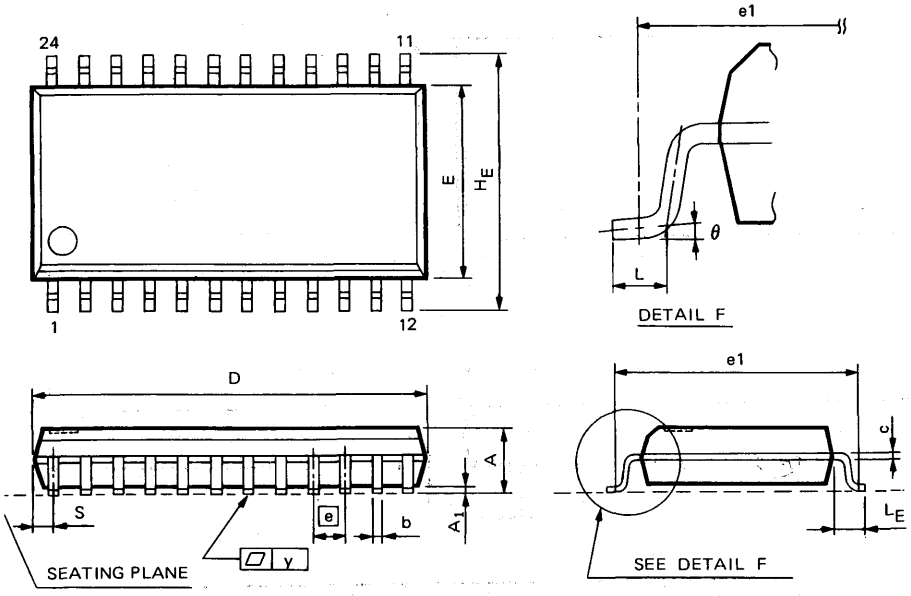
Symbol	Dimensions in inch	Dimensions in mm
A	0.106 Max.	2.692 Max.
A1	0.004 Min.	0.102 Min.
b	$0.016^{+\ 0.004}_{-\ 0.002}$	$0.406^{+\ 0.102}_{-\ 0.051}$
c	$0.010^{+\ 0.004}_{-\ 0.002}$	$0.254^{+\ 0.102}_{-\ 0.051}$
D	0.405 (0.425 Max.)	10.287 (10.795 Max.)
E	0.295 (0.320 Max.)	7.493 (8.128 Max.)
e	0.050 ± 0.006	1.270 ± 0.152
e1	0.374 Nor.	9.50 Nor.
H_E	0.406 ± 0.010	10.312 ± 0.254
L	0.032 ± 0.008	0.813 ± 0.203
L_E	0.055 ± 0.008	1.397 ± 0.203
S	0.043 Max.	1.092 Max.
y	0.006 Max.	0.152 Max.
θ	0° ~ 8°	0° ~ 8°

SO 20L Outline Dimension



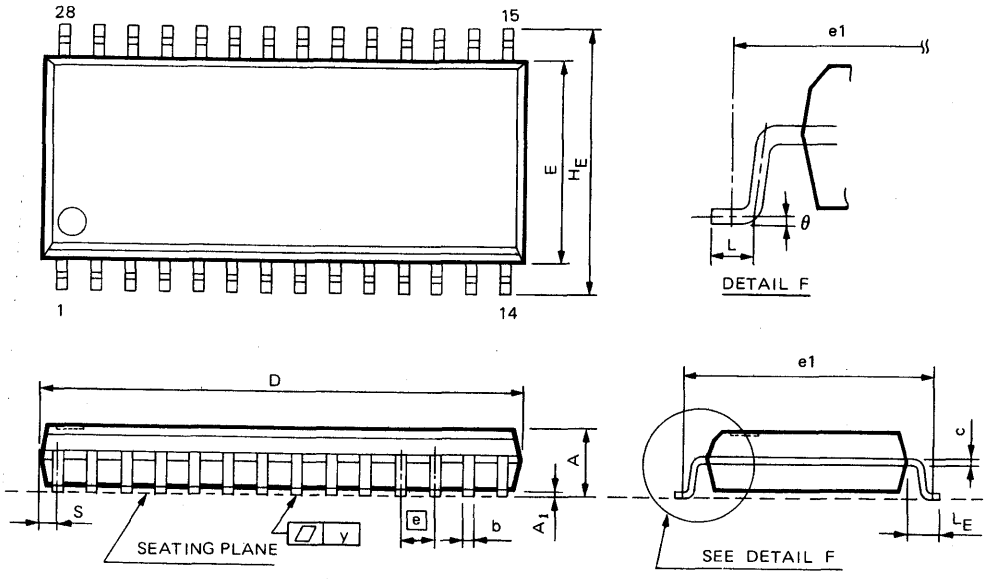
Symbol	Dimensions in inch	Dimensions in mm
A	0.106 Max.	2.692 Max.
A1	0.004 Min.	0.102 Min.
b	$0.016^{+\ 0.004}_{-\ 0.002}$	$0.406^{+\ 0.102}_{-\ 0.051}$
c	$0.010^{+\ 0.004}_{-\ 0.002}$	$0.254^{+\ 0.102}_{-\ 0.051}$
D	0.504 (0.524 Max.)	12.802 (13.310 Max.)
E	0.295 (0.320 Max.)	7.493 (8.128 Max.)
[e]	0.050 ± 0.006	1.270 ± 0.152
e1	0.374 Nor.	9.50 Nor.
H_E	0.406 ± 0.010	10.312 ± 0.254
L	0.032 ± 0.008	0.813 ± 0.203
L_E	0.055 ± 0.008	1.397 ± 0.203
S	0.042 Max.	1.067 Max.
y	0.006 Max.	0.152 Max.
θ	0° ~ 8°	0° ~ 8°

SO 24L Outline Dimension



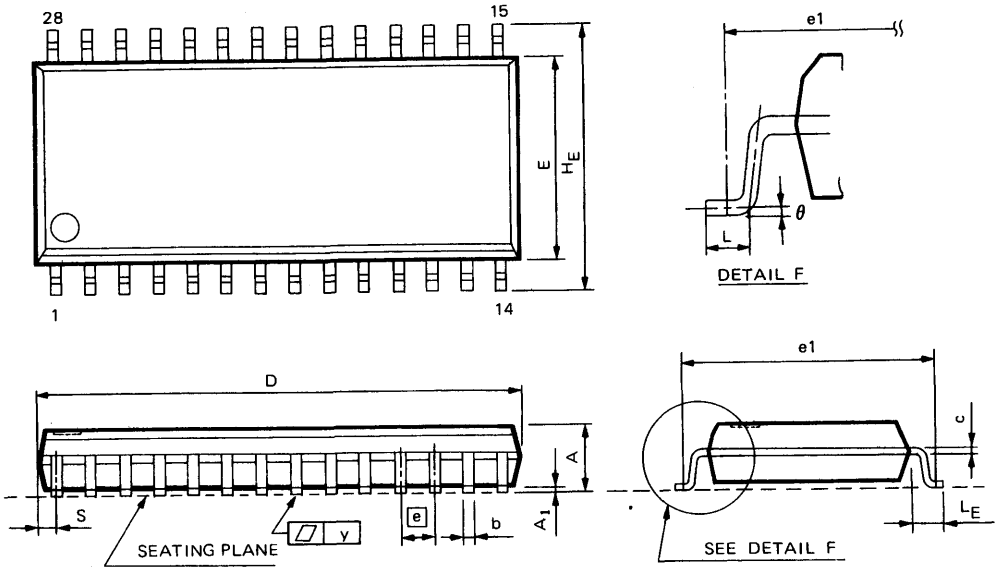
Symbol	Dimensions in inch	Dimensions in mm
A	0.106 Max.	2.692 Max.
A1	0.004 Min.	0.102 Min.
b	$0.016^{+\ 0.004}_{-\ 0.002}$	$0.406^{+\ 0.102}_{-\ 0.051}$
c	$0.006^{+\ 0.004}_{-\ 0.002}$	$0.152^{+\ 0.102}_{-\ 0.051}$
D	0.606 (0.611 Max.)	15.392 (15.520 Max.)
E	0.295 (0.320 Max.)	7.493 (8.128 Max.)
e	0.050 ± 0.006	1.270 ± 0.152
e1	0.370 Nor.	9.40 Nor.
H_E	0.406 ± 0.010	10.312 ± 0.254
L	0.036 ± 0.008	0.914 ± 0.203
L_E	0.055 ± 0.008	1.397 ± 0.203
S	0.035 Max.	0.889 Max.
y	0.006 Max.	0.152 Max.
θ	0° ~ 8°	0° ~ 8°

SO 28L Outline Dimension (300 mil)



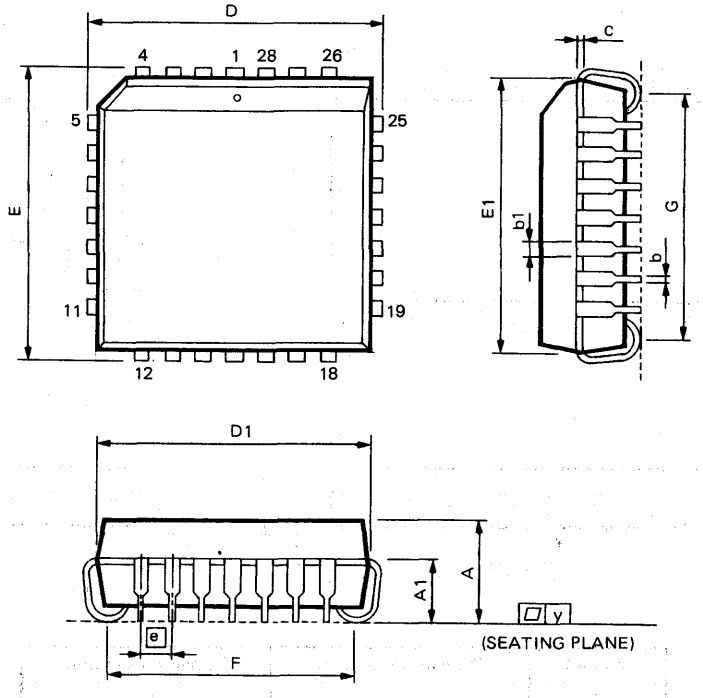
Symbol	Dimensions in inch	Dimensions in mm
A	0.106 Max.	2.692 Max.
A1	0.004 Min.	0.102 Min.
b	$0.016^{+\ 0.004}_{-\ 0.002}$	$0.406^{+\ 0.102}_{-\ 0.051}$
c	$0.010^{+\ 0.004}_{-\ 0.002}$	$0.254^{+\ 0.102}_{-\ 0.051}$
D	0.705 (0.730 Max.)	17.907 (18.540 Max.)
E	0.295 (0.320 Max.)	7.493 (8.128 Max.)
[e]	0.050 ± 0.006	1.270 ± 0.152
e1	0.370 Nor.	9.40 Nor.
H_E	0.406 ± 0.010	10.312 ± 0.254
L	0.036 ± 0.008	0.914 ± 0.203
L_E	0.055 ± 0.008	1.397 ± 0.203
S	0.045 Max.	1.143 Max.
y	0.006 Max.	0.152 Max.
θ	0° ~ 8°	0° ~ 8°

SO 28L Outline Dimension (330 mil)



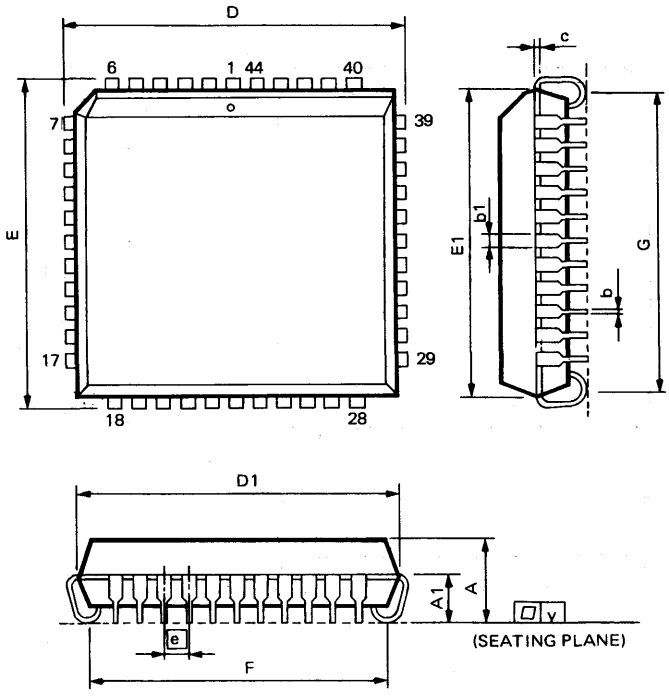
Symbol	Dimensions in inch	Dimensions in mm
A	0.112 Max.	2.845 Max.
A1	0.004 Min.	0.102 Min.
b	$0.016^{+\ 0.004}_{-\ 0.002}$	$0.406^{+\ 0.102}_{-\ 0.051}$
c	$0.010^{+\ 0.004}_{-\ 0.002}$	$0.254^{+\ 0.102}_{-\ 0.051}$
D	0.713 (0.736 Max.)	18.110 (18.694 Max.)
E	0.331 (0.356 Max.)	8.407 (9.042 Max.)
[e]	0.050 ± 0.006	1.270 ± 0.152
e1	0.429 Nor.	10.90 Nor.
H_E	0.465 ± 0.010	11.811 ± 0.254
L	0.036 ± 0.008	0.914 ± 0.203
L_E	0.067 ± 0.008	1.702 ± 0.203
S	0.048 Max.	1.219 Max.
y	0.006 Max.	0.152 Max.
θ	0° ~ 8°	0° ~ 8°

PLCC 28L Outline Dimension



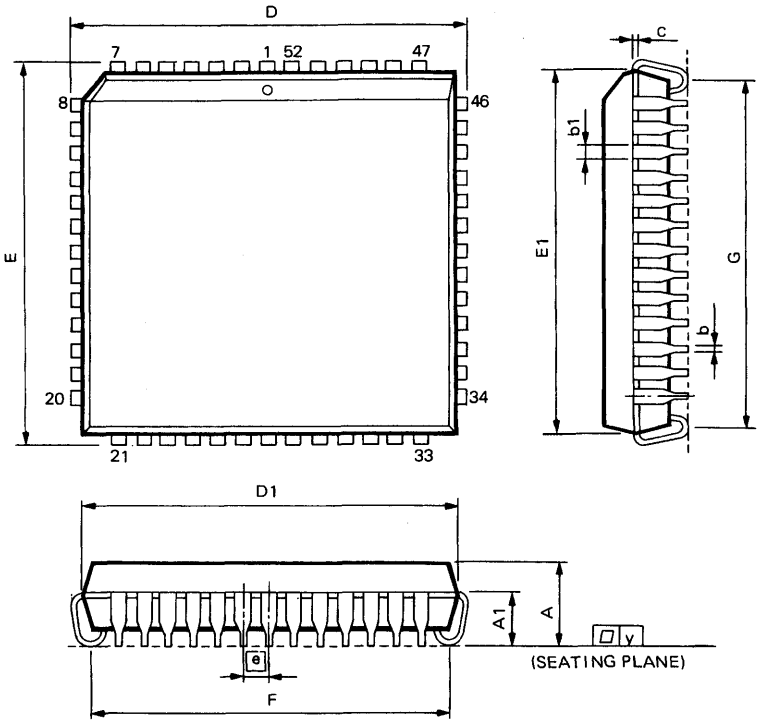
Symbol	Dimensions in inch	Dimensions in mm
A	0.172 ± 0.008	4.369 ± 0.203
A1	0.100 ± 0.008	2.540 ± 0.203
b	$0.018^{+0.004}_{-0.002}$	$0.457^{+0.102}_{-0.051}$
b1	$0.028^{+0.004}_{-0.002}$	$0.711^{+0.102}_{-0.051}$
c	$0.010^{+0.004}_{-0.002}$	$0.254^{+0.102}_{-0.051}$
D	0.490 ± 0.005	12.446 ± 0.127
D1	0.453 (0.485 Max.)	11.506 (12.319 Max.)
e	0.050 ± 0.006	1.270 ± 0.152
E	0.490 ± 0.005	12.446 ± 0.127
E1	0.453 (0.485 Max.)	11.506 (12.319 Max.)
F	0.410 ± 0.020	10.414 ± 0.508
G	0.410 ± 0.020	10.414 ± 0.508
y	0.006 Max.	0.152 Max.

PLCC 44L Outline Dimension



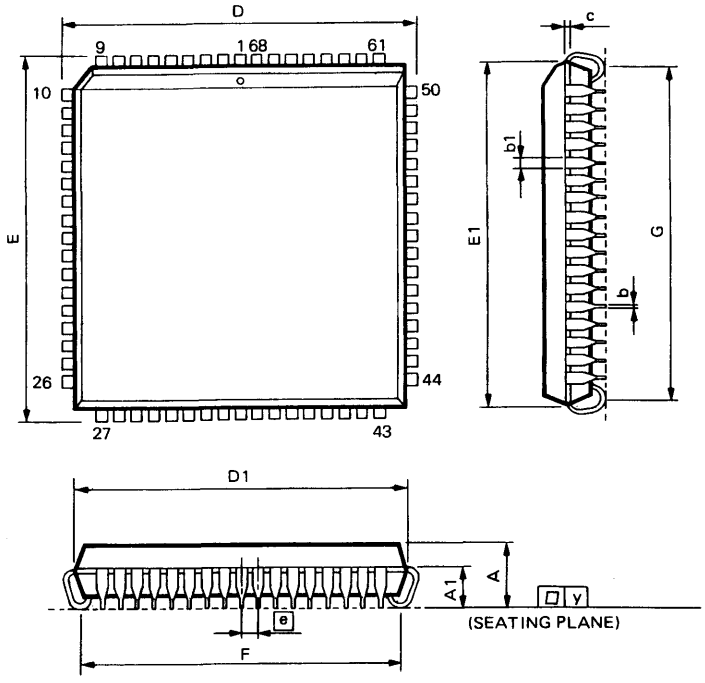
Symbol	Dimensions in inch	Dimensions in mm
A	0.172 ± 0.008	4.369 ± 0.203
A1	0.100 ± 0.008	2.540 ± 0.203
b	0.018 $^{+\ 0.004}_{-\ 0.002}$	0.457 $^{+\ 0.102}_{-\ 0.051}$
b1	0.028 $^{+\ 0.004}_{-\ 0.002}$	0.711 $^{+\ 0.102}_{-\ 0.051}$
c	0.010 $^{+\ 0.004}_{-\ 0.002}$	0.254 $^{+\ 0.102}_{-\ 0.051}$
D	0.690 ± 0.005	17.526 ± 0.127
D1	0.653 (0.685 Max.)	16.586 (17.399 Max.)
e	0.050 ± 0.006	1.270 ± 0.152
E	0.690 ± 0.005	17.526 ± 0.127
E1	0.653 (0.685 Max.)	16.586 (17.399 Max.)
F	0.615 ± 0.020	15.621 ± 0.508
G	0.615 ± 0.020	15.621 ± 0.508
y	0.006 Max.	0.152 Max.

PLCC 52L Outline Dimension



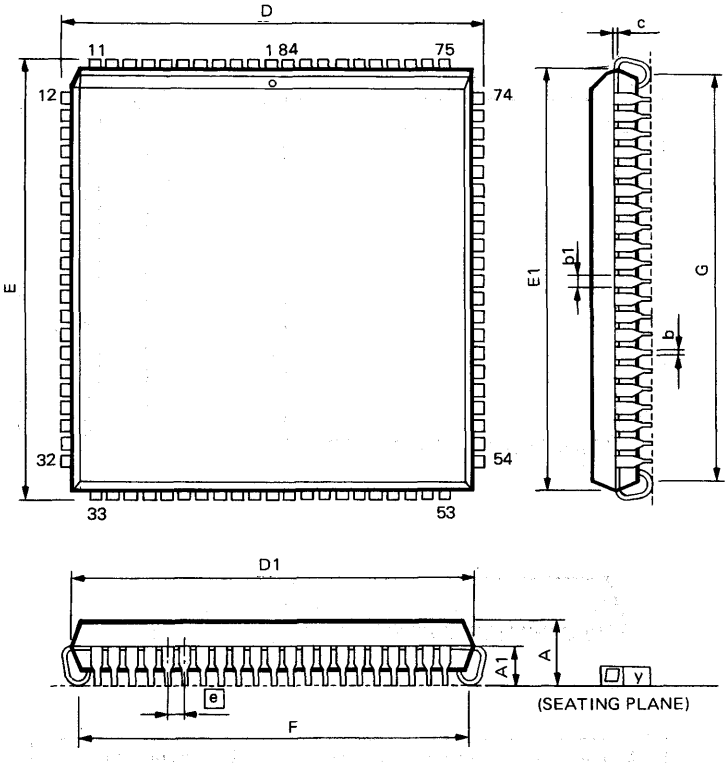
Symbol	Dimensions in inch	Dimensions in mm
A	0.172 ± 0.008	4.369 ± 0.203
A1	0.100 ± 0.008	2.540 ± 0.203
b	0.018 $^{+\ 0.004}_{-\ 0.002}$	0.457 $^{+\ 0.102}_{-\ 0.051}$
b1	0.028 $^{+\ 0.004}_{-\ 0.002}$	0.711 $^{+\ 0.102}_{-\ 0.051}$
c	0.010 $^{+\ 0.004}_{-\ 0.002}$	0.254 $^{+\ 0.102}_{-\ 0.051}$
D	0.790 ± 0.005	20.066 ± 0.127
D1	0.753 (0.785 Max.)	19.126 (19.939 Max.)
e	0.050 ± 0.006	1.270 ± 0.152
E	0.790 ± 0.005	20.066 ± 0.127
E1	0.753 (0.785 Max.)	19.126 (19.939 Max.)
F	0.710 ± 0.020	18.034 ± 0.508
G	0.710 ± 0.020	18.034 ± 0.508
y	0.006 Max.	0.152 Max.

PLCC 68L Outline Dimension



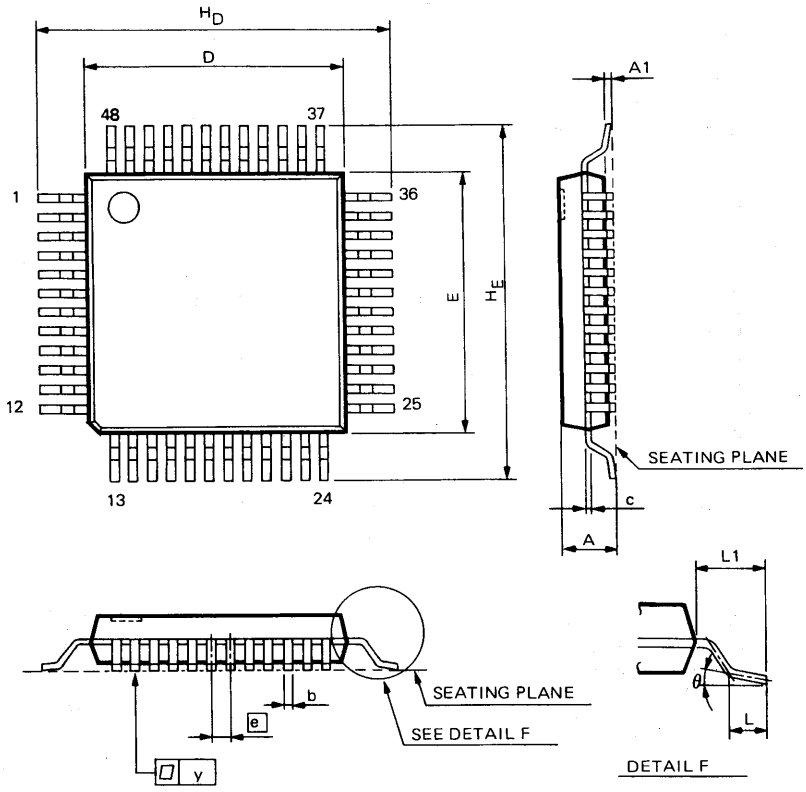
Symbol	Dimensions in inch	Dimensions in mm
A	0.170 ± 0.008	4.318 ± 0.203
A1	0.100 ± 0.008	2.540 ± 0.203
b	0.018 $^{+\ 0.004}_{-\ 0.002}$	0.457 $^{+\ 0.102}_{-\ 0.051}$
b1	0.028 $^{+\ 0.004}_{-\ 0.002}$	0.711 $^{+\ 0.102}_{-\ 0.051}$
c	0.008 $^{+\ 0.004}_{-\ 0.002}$	0.203 $^{+\ 0.102}_{-\ 0.051}$
D	0.990 ± 0.005	25.146 ± 0.127
D1	0.954 (0.985 Max.)	24.232 (25.019 Max.)
e	0.050 ± 0.006	1.275 ± 0.152
E	0.990 ± 0.005	25.146 ± 0.127
E1	0.954 (0.985 Max.)	24.232 (25.019 Max.)
F	0.917 ± 0.020	23.292 ± 0.508
G	0.917 ± 0.020	23.292 ± 0.508
y	0.006 Max.	0.152 Max.

PLCC 84L Outline Dimension



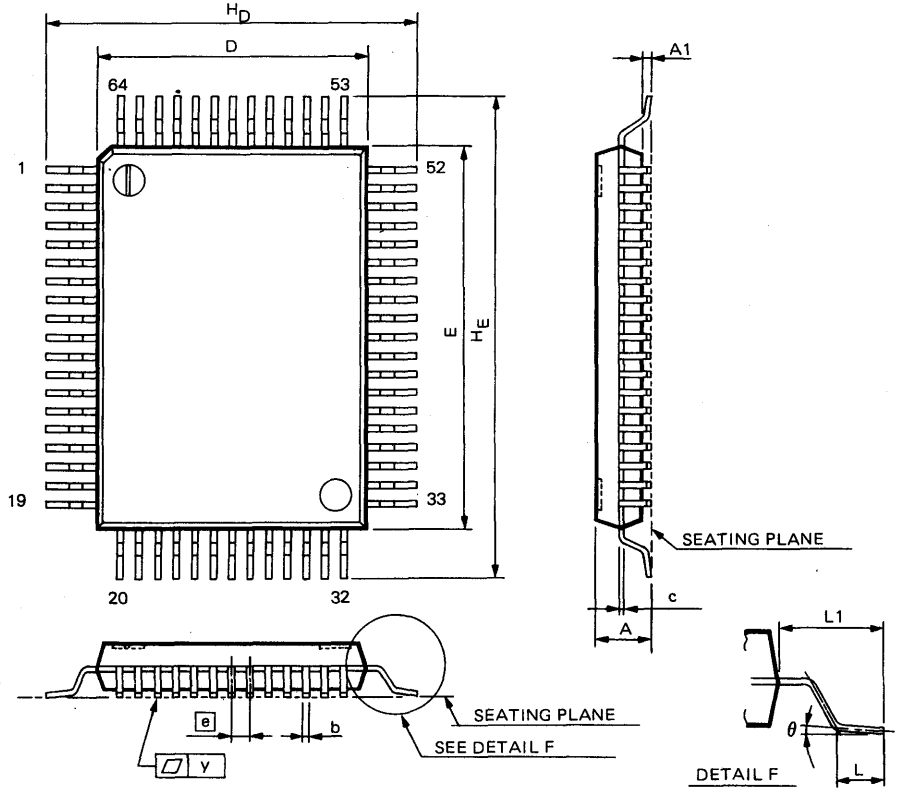
Symbol	Dimensions in inch	Dimensions in mm
A	0.170 ± 0.008	4.318 ± 0.203
A1	0.100 ± 0.008	2.540 ± 0.203
b	0.018 $^{+\ 0.004}_{-\ 0.002}$	0.457 $^{+\ 0.102}_{-\ 0.051}$
b1	0.028 $^{+\ 0.004}_{-\ 0.002}$	0.711 $^{+\ 0.102}_{-\ 0.051}$
c	0.008 $^{+\ 0.004}_{-\ 0.002}$	0.203 $^{+\ 0.102}_{-\ 0.051}$
D	1.190 ± 0.005	30.226 ± 0.127
D1	1.153 (1.185 Max.)	29.286 (30.099 Max.)
e	0.050 ± 0.006	1.270 ± 0.152
E	1.190 ± 0.005	30.226 ± 0.127
E1	1.163 (1.185 Max.)	29.286 (30.099 Max.)
F	1.117 ± 0.020	28.372 ± 0.508
G	1.117 ± 0.020	28.372 ± 0.508
y	0.006 Max.	0.152 Max.

QFP 48L Outline Dimension



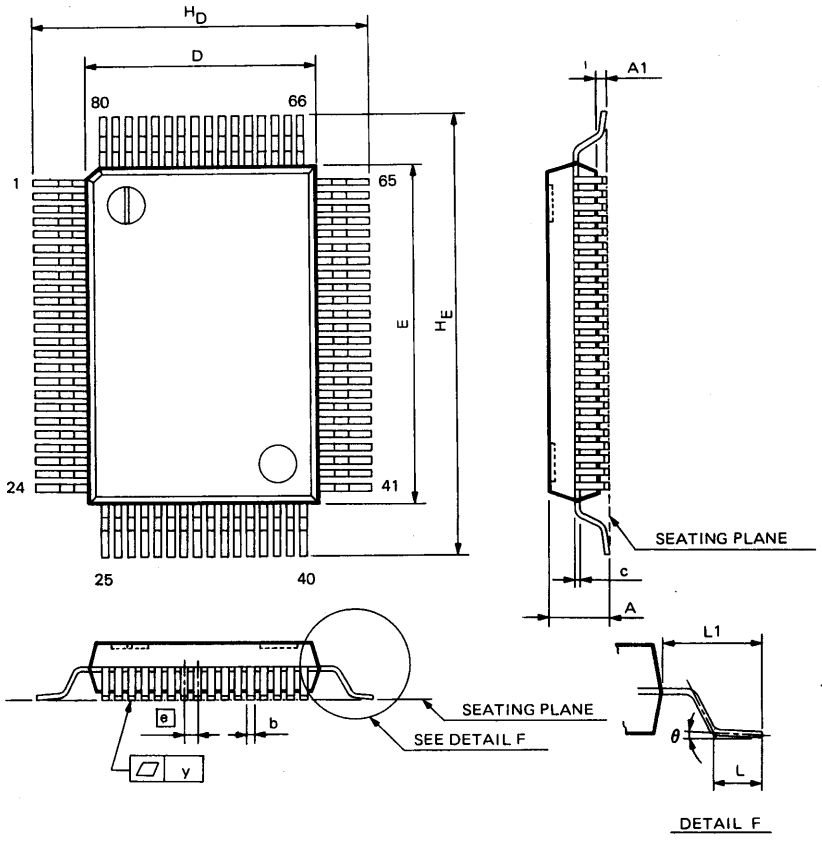
Symbol	Dimensions in inch	Dimensions in mm
A	0.063 ± 0.012	1.600 ± 0.305
A1	0.006 ± 0.004	0.152 ± 0.102
b	$0.013^{+0.004}_{-0.002}$	$0.330^{+0.102}_{-0.051}$
c	$0.006^{+0.004}_{-0.002}$	$0.152^{+0.102}_{-0.051}$
D	0.394 (0.420 Max.)	10.000 (10.668 Max.)
E	0.394 (0.420 Max.)	10.000 (10.668 Max.)
e	0.030 ± 0.006	0.762 ± 0.152
H_D	0.630 ± 0.014	16.000 ± 0.356
H_E	0.630 ± 0.014	16.000 ± 0.356
L	0.075 ± 0.012	1.905 ± 0.305
L1	0.118 ± 0.012	2.997 ± 0.305
y	0.006 Max.	0.152 Max.
θ	0° ~ 8°	0° ~ 8°

QFP 64L Outline Dimension



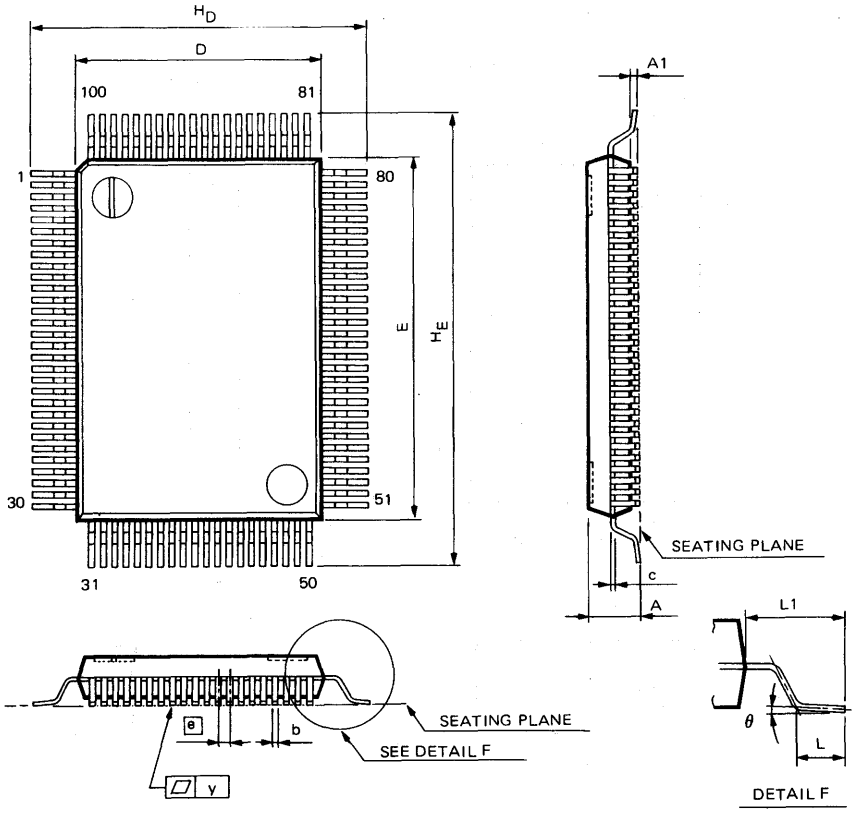
Symbol	Dimensions in inch	Dimensions in mm
A	0.120 ± 0.010	3.048 ± 0.254
A1	0.008 ± 0.004	0.203 ± 0.102
b	$0.016^{+0.004}_{-0.002}$	$0.400^{+0.102}_{-0.051}$
c	$0.006^{+0.004}_{-0.002}$	$0.152^{+0.102}_{-0.051}$
D	0.551 (0.576 Max.)	14.000 (14.630 Max.)
E	0.787 (0.812 Max.)	20.000 (20.625 Max.)
e	0.039 ± 0.006	1.000 ± 0.152
H_D	0.740 ± 0.012	18.796 ± 0.305
H_E	0.976 ± 0.012	24.790 ± 0.305
L	0.047 ± 0.012	1.194 ± 0.305
L1	0.095 ± 0.012	2.413 ± 0.305
y	0.006 Max.	0.152 Max.
θ	0° ~ 8°	0° ~ 8°

QFP 80L Outline Dimension



Symbol	Dimensions in inch	Dimensions in mm
A	0.120 ± 0.010	3.048 ± 0.254
A1	0.008 ± 0.004	0.203 ± 0.102
b	$0.014^{+0.004}_{-0.002}$	$0.351^{+0.102}_{-0.051}$
c	$0.006^{+0.004}_{-0.002}$	$0.152^{+0.102}_{-0.051}$
D	0.551 (0.576 Max.)	14.000 (14.630 Max.)
E	0.787 (0.812 Max.)	20.000 (20.625 Max.)
e	0.032 ± 0.006	0.800 ± 0.152
H_D	0.740 ± 0.012	18.796 ± 0.305
H_E	0.976 ± 0.012	24.790 ± 0.305
L	0.047 ± 0.012	1.194 ± 0.305
L1	0.095 ± 0.012	2.413 ± 0.305
y	0.006 Max.	0.152 Max.
θ	0° ~ 8°	0° ~ 8°

QFP 100L Outline Dimension



Symbol	Dimensions in inch	Dimensions in mm
A	0.120 ± 0.010	3.048 ± 0.254
A1	0.008 ± 0.004	0.203 ± 0.102
b	$0.012^{+0.004}_{-0.002}$	$0.305^{+0.102}_{-0.051}$
c	$0.006^{+0.004}_{-0.002}$	$0.152^{+0.102}_{-0.051}$
D	0.551 (0.576 Max.)	14.000 (14.630 Max.)
E	0.787 (0.812 Max.)	20.000 (20.625 Max.)
e	0.026 ± 0.006	0.650 ± 0.152
H_D	0.740 ± 0.012	18.796 ± 0.305
H_E	0.976 ± 0.012	24.790 ± 0.305
L	0.047 ± 0.012	1.194 ± 0.305
L1	0.095 ± 0.012	2.413 ± 0.305
y	0.006 Max.	0.152 Max.
θ	0° ~ 8°	0° ~ 8°

UMC

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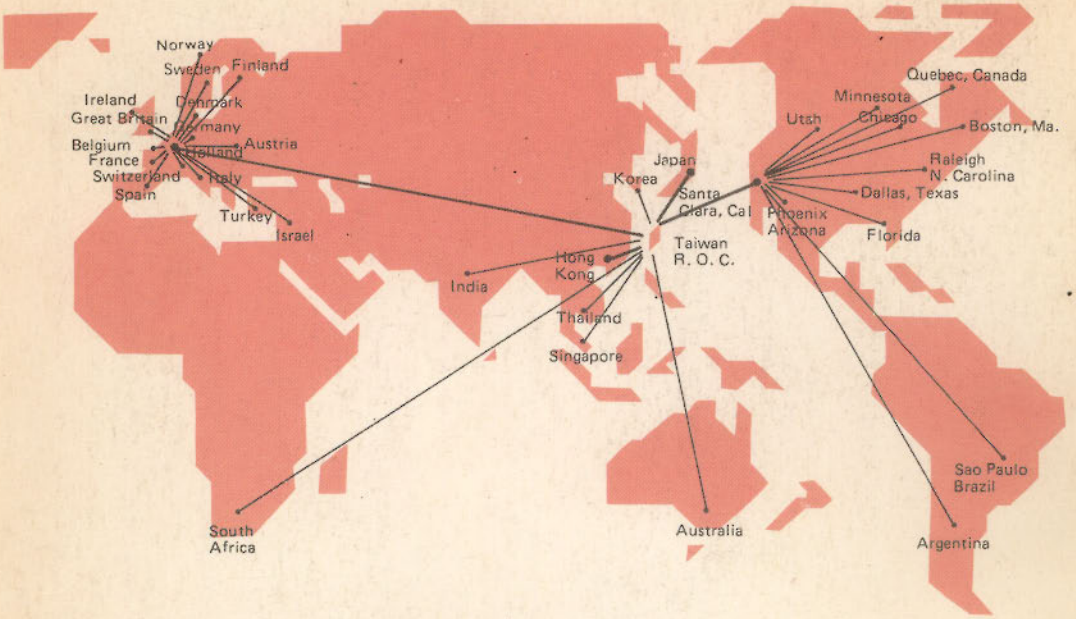

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Printed in Taiwan, R.O.C.
August 1990

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